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Implementation of a 32-bit High Speed Phase Accumulator for Direct Digital Frequency Synthesizer

^{1,2}Salah Hasan Ibrahim, ²Sawal Hamid Md. Ali and ³Shabiul Islam

¹Faculty of Engineering, Diyala University, Republic of Iraq

²Department of Electrical, Electronics and System Engineering,

³Institute of Microengineering and Nanoelectronics, Universiti Kebangsaan Malaysia, 43600, UKM, Bangi, Malaysia

Corresponding Author: Salah Hasan Ibrahim, Faculty of Engineering, Diyala University, Republic of Iraq

ABSTRACT

This study presents 32-bit Phase Accumulator (PA) design, using the pipelining stages with modified Brent-kung (BK) adder. In this design, clock pulse division technique applied to reduce the number of the registers and thus reduce the power consumption. The new architecture of the 32-bit Phase accumulator with modified BK adder and clock pulse division technique, reduce the number of PA registers from 119-81 registers correspond to about 32% reduction. The comparing results of the proposed PA designs with the other designs, using the ALTERA software (Quartus 2 Cyclone 3) reveals that the PA designs with modified BK run about 27% faster and less delay compared with the previous works, as well as with the lowest number of registers and logic cells.

Key words: Phase accumulator, brent-kung adder, direct digital frequency synthesizer

INTRODUCTION

The rapid development in the field of Radar and telecommunications requires a system capable of operating at a higher output frequency, precise frequency resolution and fast switching channel. Direct Digital Frequency Synthesizer (DDFS) is a system capable to meet these requirements and is increasingly attracting researchers to apply such system for telecommunications and Radar application. Phase accumulator (PA) is one of the main components in the DDFS system that gives huge impact to the performances that contain adder as one of its core elements in the architecture. Several techniques used to develop phase accumulator. Some of the solutions proposed to improve the speed and reduce the complexity by using parallel or pipelining design technique. The pipelining technique used to increase the throughput of the output frequency (Betowski and Beiu, 2003; Geng *et al.*, 2010; Jensen, 2012; Ibrahim *et al.*, 2012) but this leads to increase the power consumption and the chip area. The clock gating technique and two discrete clock drivers are used to drive two different flip flops applied in the phase accumulator design of DDFS to reduce the number of registers required in the pipeline without performance retraction by Yong Sin and Sung-Mo (2006), Chen *et al.* (2012) and Yoo *et al.* (2012), respectively. A high speed DDFS with low power pipelining parallel accumulator designed with 32-bit and 24-bit input (Yang *et al.*, 2002; Chappell and McEwan, 2004; Horowitz and La Rue, 2005) based on pipelining parallel technique.

This study proposes a new design of 32-bit pipelined phase accumulator based on Brent-Kung (BK) Adder (Brent and Kung, 1982; Marso, 2008) and clock pulse division technique. Some modifications added to the BK adder structure in order to be used in a pipelining architecture. The PA based on 4 pipeline stages; each stage contains a modified 8-bit adder and an 8-bit register as a storage element. The carry-in of 8-bit BK adder in the first stage set as zero, while the carry-out connects to the carry-in of the next BK adder.

Phase accumulator architecture: The frequency resolution of a DDFS determined by the clock frequency (F_{clk}) and the number of N input bit of the PA ($F_{res} = F_{clk}/2^N$). The number of the pipeline stages depends on FCW bit and the number of bits in each stage.

A large number of pipeline stages, increase the number of registers (Fig. 1), which leads to a higher power consumption. Therefore, in this design, a clock division technique used to reduce the number of registers while preserving the high speed operation. In this technique, D flip-flops (DFFs) used to connect between each row of the pipeline stages and control the FCW input registers in the stages. These registers clocked by the pipelined pulses with one clock cycle based on the dividing clock pulses. Doubling the DFFs between the pipelining rows, to overcome the doubling of clock frequency and reach the synchronization of the PA during the operating time. The new architecture of the 32-bit Phase accumulator with modified BK adder and clock pulse division technique shown in Fig. 2.

Considered the input bit of PA is N. The phase accumulator partitioned into L stages with B DFFs in each stage Fig. 1, a number of the pre skewing registers R are:

$$R = \frac{N*(L+1)}{2} \quad (1)$$

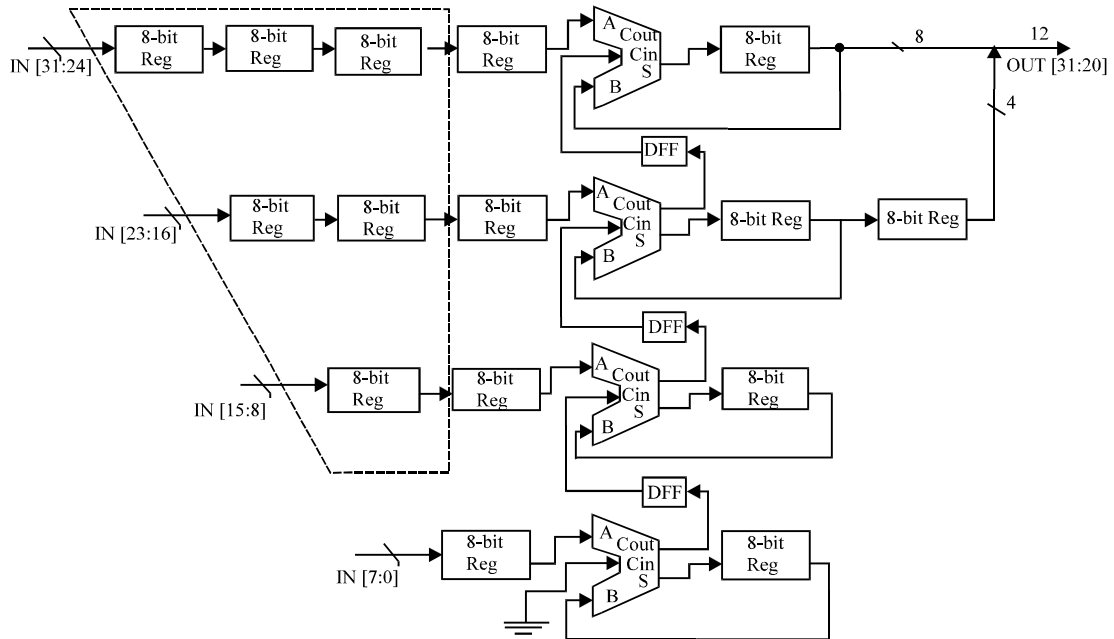


Fig. 1: Block diagram of 32-bit pipeline phase accumulator design

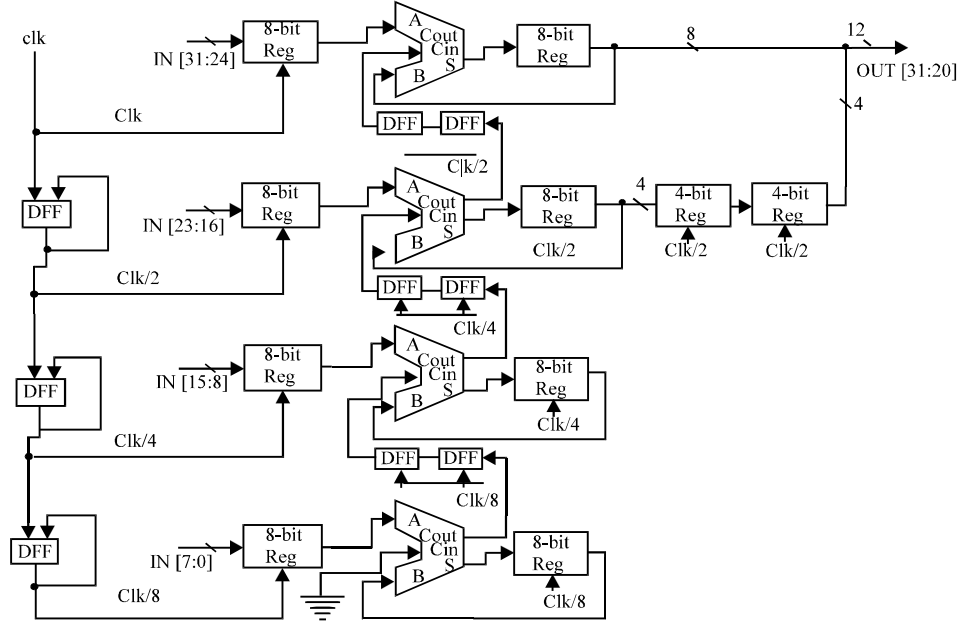


Fig. 2: Block diagram of 32-bit pipeline phase accumulator design based on 8-bit modifying Brent-Kung adder with clock division technique

Applying the clock pulsing division method for the proposed design, the calculation of pre skewing registers R becomes:

$$R = [N+3 (L-1)] \quad (2)$$

With the clock pulse division, the numbers of pre skewing registers reduced to a 48.7% reduction.

Pipelined PA starts counting only after (L+1) clock pulses, (L-number of pipeline stages). Applying the clock pulse division technique, the PA circuit operation passed with one clock pulse only and the output values appear after the second clock pulse.

With the clock pulse division technique, the numbers of PA registers reduced from 119-81 registers correspond to about 32% reduction (Fig. 1).

Brent-Kung adder is a fast adder and all the carries computed simultaneously through a binary tree of "BK" cells. BK cells consist of combinational logic gates and it computed as a sum of G and P (Bazargan, 2006):

$$BK = G+P \quad (3)$$

$$G = g''+p''.g' \quad (4)$$

$$P = p''.p' \quad (5)$$

where, g'' g' , p'' p' higher-lower generate and propagate function, respectively. The p-propagate function ($p_i = x_i \oplus y_i$) and g is a generate function ($g_i = x_i \cdot y_i$).

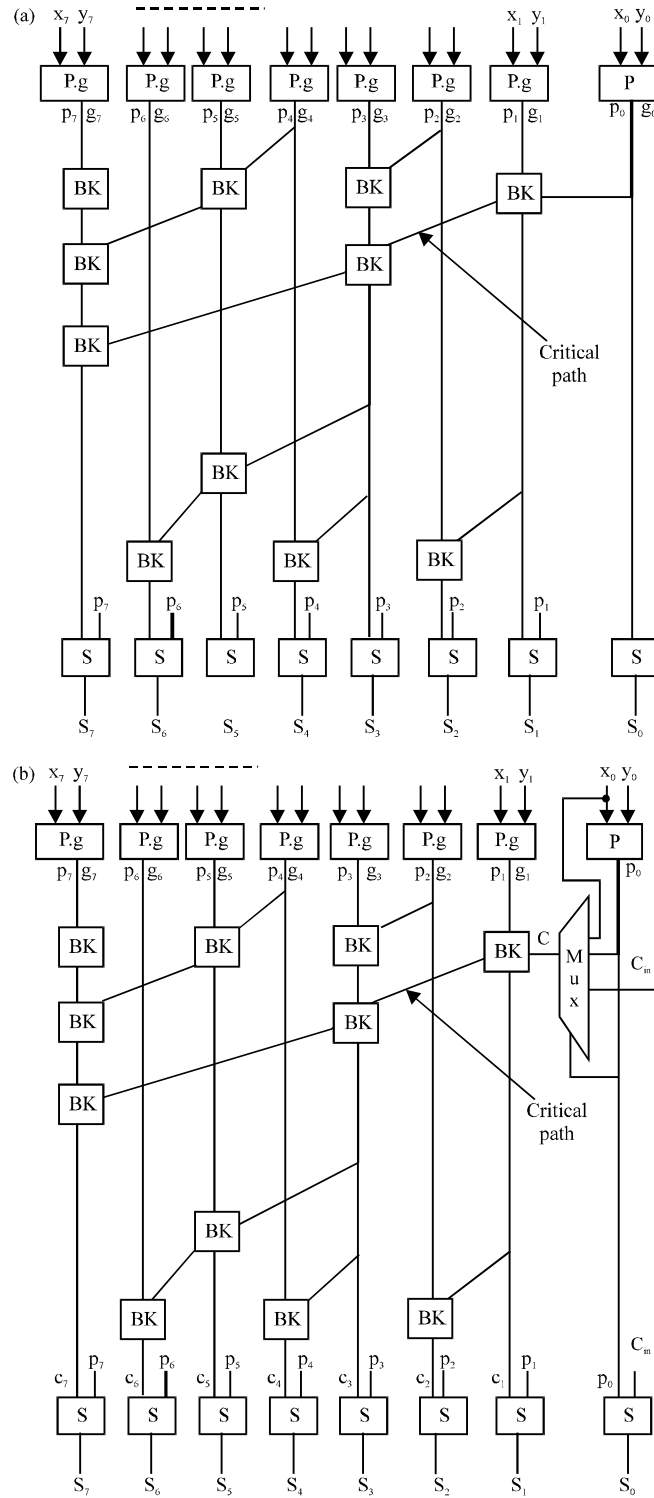


Fig. 3(a-b): (a) Conventional Brent-Kung adder and (b) Modified Brent-Kung adder

To be able to use the BK adder in pipelining architecture, the adder modified by replacing the (p.g) block of the first bit Fig. 3a with an Exclusive OR gate (XOR) with the

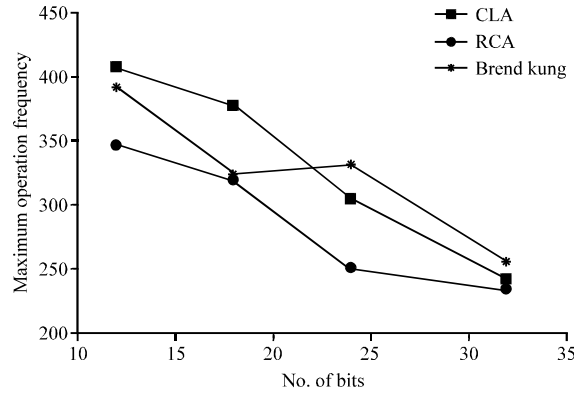


Fig. 4: Comparison result of maximum operating frequency (f_{Max}) for phase accumulator with Brent Kung, Carry Look-ahead (CLA) and Ripple Carry Adder (RCA)

(X_0) input is multiplexed with carry input (C_{in}) and carry out as the output of the multiplexer ($C_1 = (p_0 \cdot C_{in}) + (X_0 \cdot p_0^-)$), shown in Fig. 3b. Where: C_1 -carry out, P_0 -propagate function, C_{in} -Carry input and X_0 -first bit input. The carry-out equations for each bit of the modified BK adder written below:

The sum and carry-out equations of the modified 8-bit BK adder shown in the Eq. 6-8:

$$S_0 = P_0 \oplus C_{in} \quad (6)$$

$$S_{(7 \dots 1)} = P_{(7 \dots 1)} \oplus C_{(7 \dots 1)} \quad (7)$$

$$C_{out} = g_7 + P_7 \cdot C_7 \quad (8)$$

Several comparisons made for pipelining PA designs based on BK, CLA and RCA adder, including 12, 18, 24 and 32-bit. The comparison result shown in Fig. 4 and it shows that the proposed architecture is faster than conventional architectures, especially in PA with a large (8-bit) adder design.

EXPERIMENTAL RESULTS

Proposed architecture successfully implemented on the Cyclone 3 FPGA platform, as shown in Fig. 5. The implementation shows that the Q output of the PA Increases steadily by FCW for every successive clock pulse, as long as the PA output $Q = 2^{N-1}$, then it resets back to zero. The Fig. 5 shows the output of the PA from the FPGA kit which appears as a saw tooth shape.

The performance of the proposed PA architecture compared with some previous works. For this purpose, the previous works re-designed and implemented on the same FPGA kit.

Table 1 shows the comparison results between the proposed phase accumulator and others previous works. The comparison shows that the proposed architecture performs significantly better compared to other architectures on a similar FPGA platform. The proposed architecture achieved

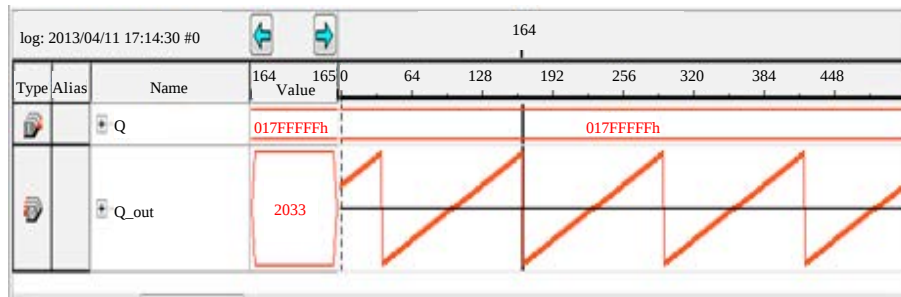


Fig. 5: Signal tap logic analyzer for PA with 32-bit BK adder implemented on Cyclone 3 FPGA Kit

Table 1: Comparison result between the proposed phase accumulator and others previous works

Ref.	Max. Freq f_{Max} (MHZ)	Propag. Data delay T_d (nano sec)	Logic cells	Registers
Chen <i>et al.</i> (2012)	83.56	11.90	113	86
32 bit PA with RCA	136.50	7.25	127	113
This work	268.31	8.40	20+4 LUT LCs	82

higher operation frequency and smaller delay while keeping the lower number of components. The improved performances give an indication of bigger possibilities that can be achieved by the proposed design, when it's translated into integrated circuits.

CONCLUSION

A new architecture for high speed phase accumulator successfully designed and implemented. The new architecture of the 32-bit Phase accumulator with modified BK adder and clock pulse division technique, reduce the number of PA registers from 119 to 81 registers correspond to about 32% reduction. Comparison with the previous architecture on a similar FPGA platform shows that the proposed architecture runs about 27% faster and less delay compared with the previous works. All this is done, with a low number of components suggesting to lower power consumption.

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