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Low Energy, Low Power Adder Logic Cells: A CMOS VLSI Implementation

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ABSTRACT

The importance of adder sub-systems are well known by every designers and engineers. Hence the engineers are still doing research with them by incorporating novel design techniques to speed up the circuit along with power reduction. Adder logic-cells are used in many applications like within a microprocessors, digital signal processors, etc., especially where the digital data is being processed. A Complementary Metal Oxide Semiconductor (CMOS) design techniques are implemented here with different logic styles. We implement some novel design ideas which will have less number of transistors along with variable length and width of the transistors to implement the addition. Reduction of clock frequency, supply voltage and the load capacitance are the pertinent techniques to reduce the dynamic power dissipation. Methods like clock gating, transistors with high thresholds, increasing the length of the transistors are few techniques to reduce the static power dissipation. We simulate our adder logic-cell designs using DSCH (Digital Schematic) Computer Aided Design (CAD) tool. A Microwind which is a Layout Editor tool is used to acquire better results of power dissipation and they are compared along with the conventional CMOS logic, Pass-transistor logic, Transmission-gate logic styles. We conclude pass-transistor logic based results are better as compared to the other designs. All simulation results are made using 90 nm foundry technology libraries using Microwind software tool. Our work will be further extended by designing novel XOR/XNOR circuits for the improvement of power reduction of the adder logic-cells.

Key words: Adders, CMOS VLSI, dynamic power, low energy, low power, static power

INTRODUCTION

Moore's law state that the number of transistors double once in every eighteen months. Since there are millions and millions of transistors are being integrated to perform the function of the device, there is a huge amount of power is being dissipated. This cause a major problem with reliability, since the chip becomes heater. An another problem is that to charge the device very often. Alternative solution may be to increase the storage capacity of battery. But the battery technology is not having a rapid growth like the semiconductor ICs due to the risk factors involved with batteries. So designers need to find an alternative solution to overcome this power issue (Peiravi *et al*., 2009; Yeap, 1998; Kang and Leblebici, 2003).

A circuit is to be modified in such a way that the power dissipation will be reduced in a device or chip. Static and dynamic power dissipations are the major broad source of power in semiconductor devices (Hu *et al*., 2011). Even during the sleep or idle state of the device, the

transistors may leak some current like reverse-biased PN junction leakage current, sub-threshold current, etc. This is being referred to as static or leakage power dissipation which is a major problem nowadays because of shrinking the technology. Earlier this is not a major issue where the number of transistors are minimum in a device (Priya *et al*., 2012; Reddy, 2011; Vigneswaran *et al*., 2006). But with many more transistors, this will be a quite reasonable amount compared to the dynamic power. By reducing the width or increasing the length of a transistor, this leakage current can be minimized.

Similarly, by blocking the transistors or circuitry which is not used during the functionality of the device, the dynamic power dissipation can be minimized. Also by assigning multiple operating voltages, V_{dd} to the circuit, we can able to control the dynamic power. An another approach is by analyzing the critical and non-critical path in a circuit. The speed of the transistors which are in non-critical path can be reduced by offering less V_{dd} and hence the power is too. Speed can be compromised by applying more V_{dd} to the transistors which are in the critical path (Chandrakasan and Broderson, 1995; Vigneswaran and Reddy, 2006).

Adders are playing a vital role in any kind of scientific computations. Even sub systems like multipliers can be designed with the help of adders (Haghparast and Navi, 2007). So, power reduction with adder will make a dramatic overall power change in a chip. A study of adder design by efficient XOR gates is made and in turn they are used for adder design. XOR/XNOR gates are designed with few number of transistors in turn help to reduce the size and power the adder circuitry. A pass-transistor logic style can used for the design of XOR/XNOR gates. Dynamic and domino logic styles are also can be used to reduce the number of transistors but at the cost of power. Since the clocking circuitry is involved here, there will be a large amount of power dissipation may occur.

A main objective of this work is to design low-power adder circuits with the help of efficient XOR/XNOR gates. XOR gates are being designed using 6 transistors, 4 transistors and 3 transistors and are used in designing full adders respectively. This study focus more on reducing the layout area of the adder design which in turn minimize the power. Area, Power and Speed are the three major optimization goals in the filed of VLSI domain. These all the parameters can be analyzed and compared with each other designs using software tool. All the implementation along with the results are produced using Electronic CAD tools like Digital Schematic (DSCH) and Microwind layout editor (Elamaran and Upadhyay, 2013; Elamaran *et al*., 2012).

FULL ADDER SCHEMATIC DESIGNS

Any processor or a controller needs an ALU (Arithmetic Logic Unit), performing all the basic mathematical and comparative operations. Adders are the integral part of the ALU and also very frequently invoked to generate addresses for various branching instructions. Adder sub-systems play an immense role in the area of signal processing like during the calculation of convolution, Fast Fourier Transform, etc. All kind of multipliers like array multiplier and Wallace-Tree multiplier are being designed with the help adder sub-systems.

An efficient adder design which dissipates less power may help to reduce the overall power of the system. The full adders with A, B, C in as inputs and Sum, Cout as outputs can be implemented in several ways. It is expressed as in Eq. 1, which is the most traditional method.

$$\begin{aligned} \text{Sum} &= A \oplus B \oplus Cin \\ \text{Cout} &= A.B + Cin.(A \oplus B) \end{aligned} \quad (1)$$

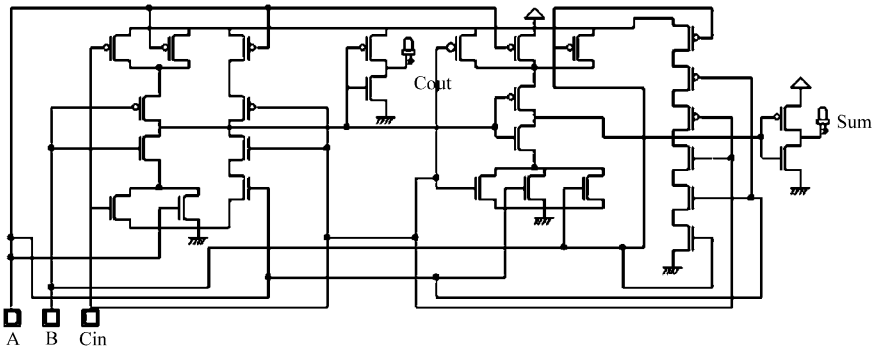

Fig. 1: Full adder-conventional style

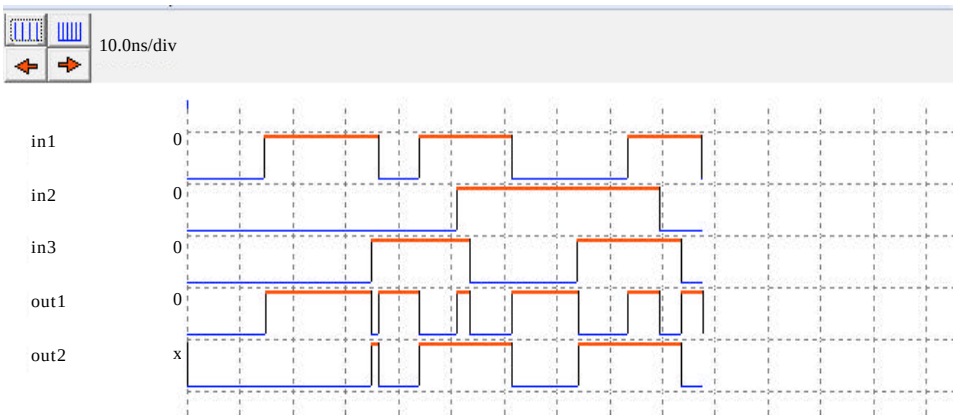

Fig. 2: Full adder-functional timing diagram

Full adder schematic-conventional style (28 transistors): The conventional and the most basic CMOS design consists of 14 PMOS and 14 NMOS transistors (Weste, 2006) following the symmetry, has been illustrated in Fig. 1.

It is the primitive and simple design exploiting the symmetry exhibited by the zeroes and ones in the truth table of a full adder. But the reason for the design being ignored is the number of transistors it involves and hence eating up quite a high power. The timing for the operation of full adder using the design is shown below in Fig. 2.

Full adder schematic using 6T XOR gate (24 transistors): An implementation of full adder with 24 transistors, using a XOR gate which has been put through using 6T-3 PMOS and 3 NMOS, which is shown in Fig. 3. Two such XORs are cascaded to get the sum and carry has obtained using the following expression as in Eq. 2.

$$Cout = [(A.B)' . \{(A \oplus B).C\}']' \quad (2)$$

Full adder schematic using 4T XOR gate (20 transistors): An another design which includes a XOR logic gate (Fig. 4) made of 4 transistors, which when cascaded leads to the sum output and using the same logic for carry, as explained earlier. It can be seen that our every subsequent design brings down the number of transistors necessitated in the circuitry and thus the chip density.

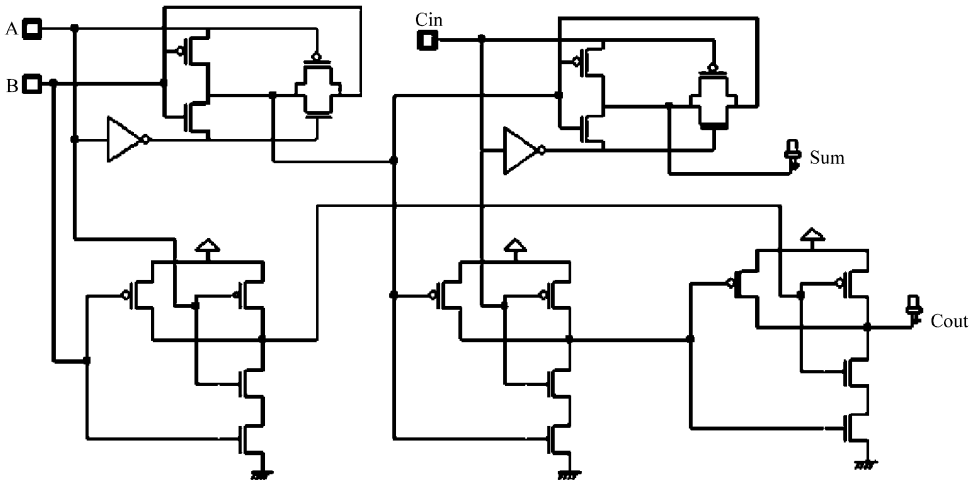

Fig. 3: Full adder using 6T-XOR design

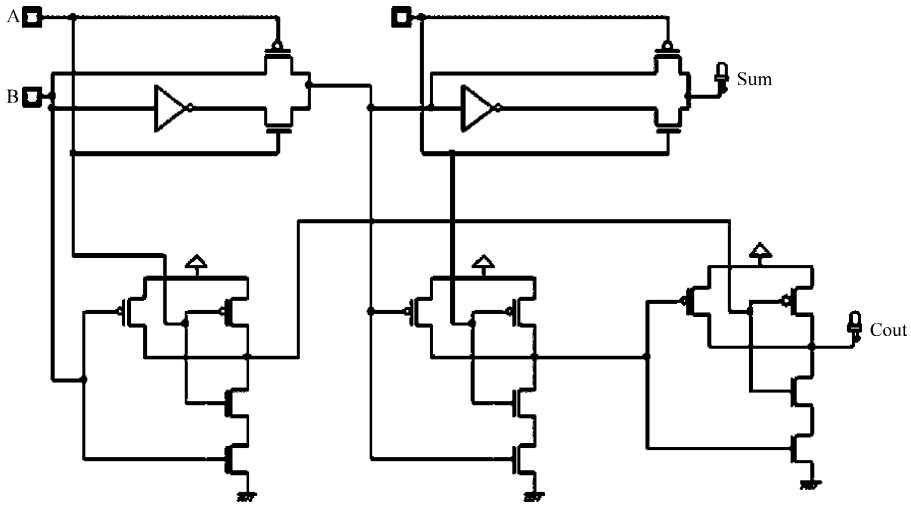

Fig. 4: Full adder using 4T-XOR design

A novel full adder schematic using 20 transistors: The novel design which includes only 20 transistors without any direct application of the logic gates like XOR or the NAND as in previous cases. Even though it has the same number of transistors, the power consumed and the complexity of the circuit has been reduced. The following Fig. 5 shows this schematic and is made during the simulation.

A novel full adder schematic using 3T XOR gate (18 transistors): This is the design which employs a 3T XOR design being cascaded to arrive at the sum. And it deals with the least number of transistors, only 18. So, the transistors have been cut down from 28 T (Conventional design) to 18T (3T-XOR design), this shows the potential of VLSI Technology in implementing low power Full Adder design with a very significant reduction in the surface area and also the power dissipated.

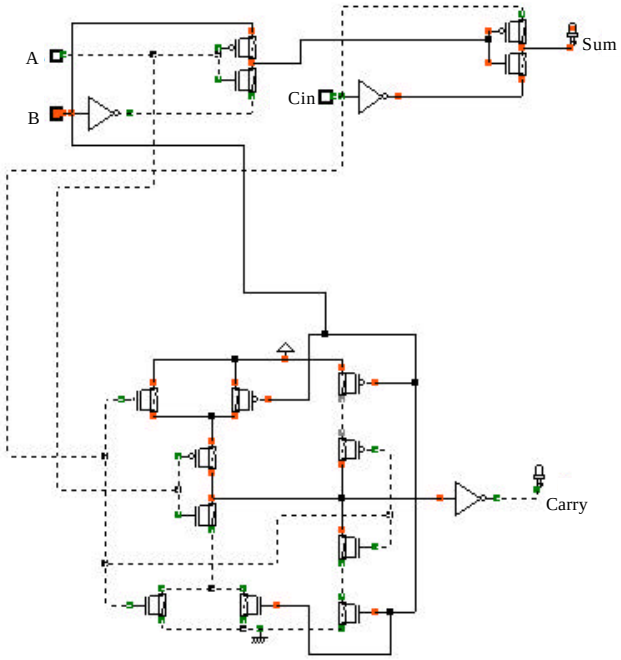

Fig. 5: Full adder using 20 T (without XOR logic)

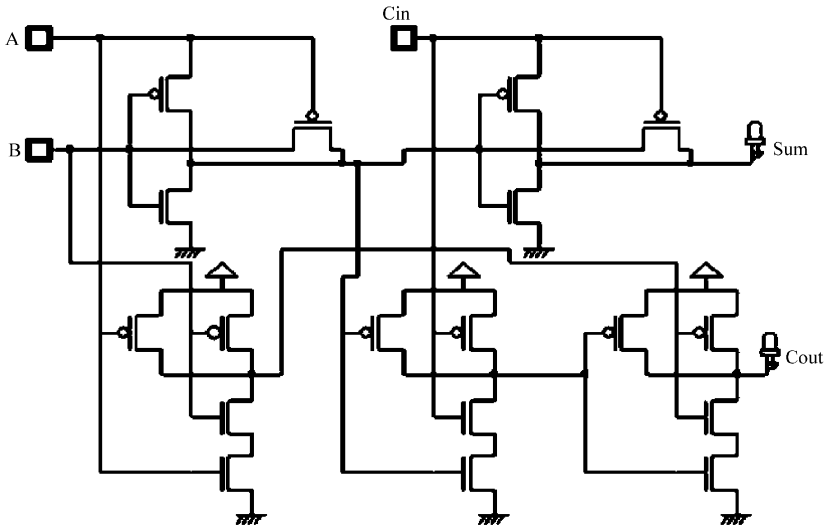

Fig. 6: Full adder using 3T XOR

The Fig. 6 shows this design and the functional verification is done using DSCH tool.

SIMULATION RESULTS

All simulation layouts presented here are produced by Microwind CAD tool which is a layout editor and simulator. A simulation can be done on the layout produced by the tool. It used mask (MSK) files to store information of the designed layout. Performance characteristics like power dissipation, rise delay, fall delay, layout area, timing diagram results can be provided by this tool.

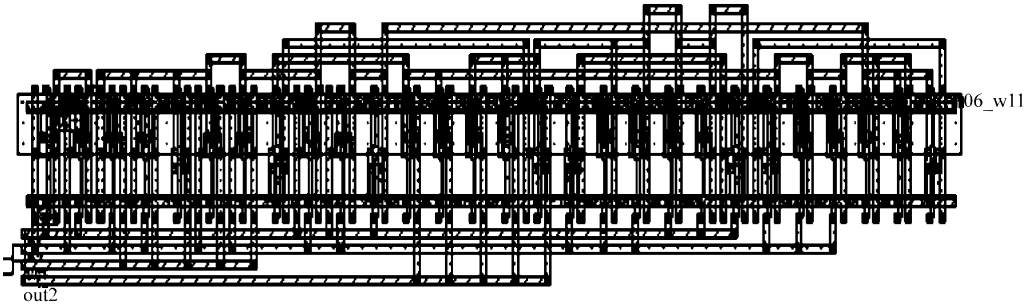

Fig. 7: Layout of 18T full adder (3T-XOR)

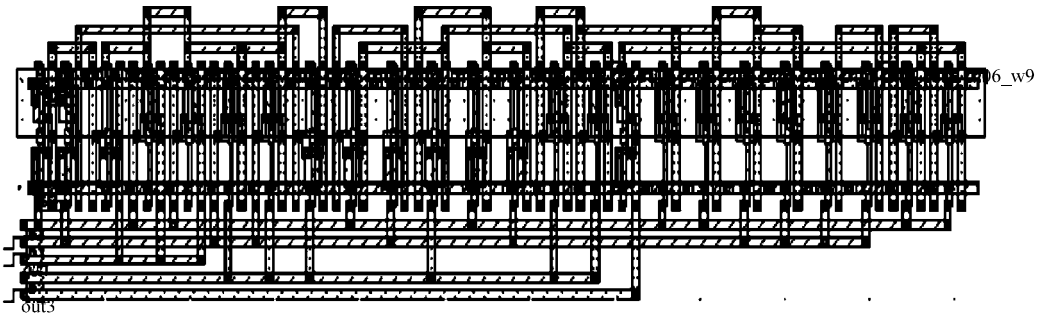

Fig. 8: Layout of 20T full adder (without XOR)

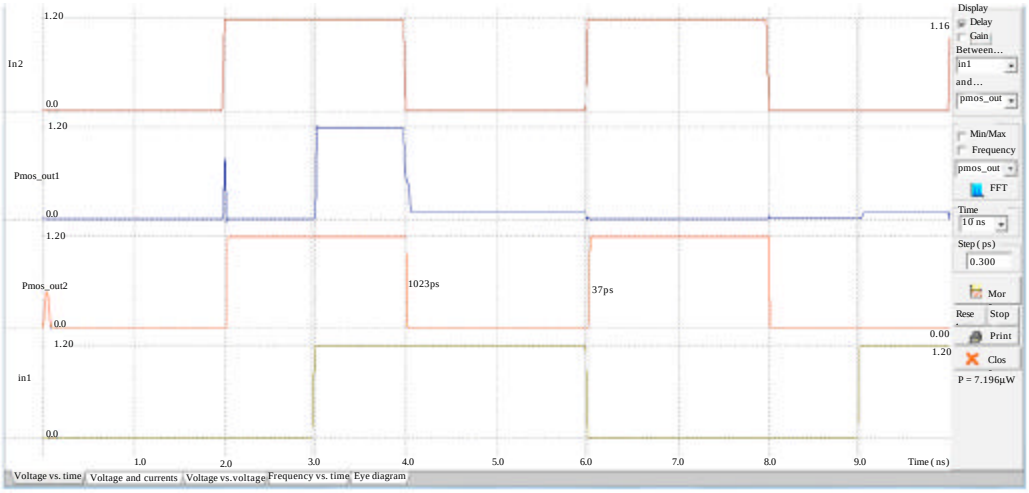

Fig. 9: Analog simulation of full adder (18 transistors)

Since, the usage of this tool is very easy, more time spent to have a better design rather than learning how to use the tool. This tool has the facility to convert the layout to Caltech Intermediate Format (CIF) which contains the information for fabrication. Metal Oxide Semiconductor Implementation Service (MOSIS) uses standard masks layout like CIF for fabrication. It has also a EXTRACT program to extract the electrical parameters. A Design Rule Checker (DRC) is invoked and convey the information about any violations of design rule for a particular foundry process.

Figure 7 and 8 show that the layout design of Full Adder using 18 Transistors (using 3T-XOR) and 20 Transistors (without XOR logic), respectively.

Figure 9 and 10 show that the analog simulation of Full Adder using 18 Transistors (with 3T-XOR) and 20 Transistors (without XOR), respectively.

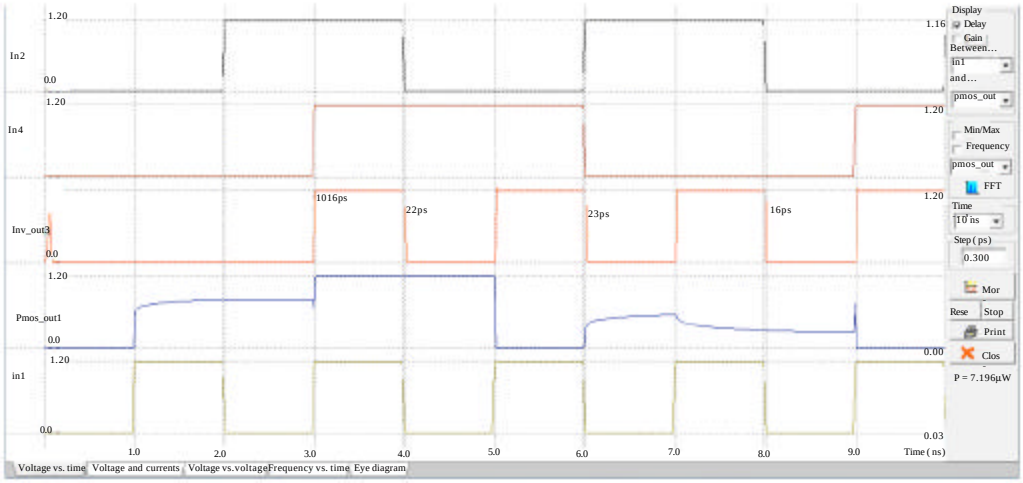

Fig. 10: Analog simulation of full adder (20 transistors)

Table 1: Simulation results on layout

Design	Power (µW)	Area(µm^2)	Transistor count
Conventional	19.179	517.1	28
FA-6T XOR	9.038	365.9	24
FA-4T XOR	14.348	315.5	20
FA with 20T	9.172	270.9	20
FA-3T XOR	7.196	347.8	18

A simulation is done on the layout for all the designs with V_{DD} = 1.2 V using 0.12 µm process for the period of 10 n sec. Table 1 provide the results of layout area with power dissipation involved in each design. A Full Adder using 3 Transistor XOR logic approach is superior with others on power dissipation aspect. It dissipates only 7.196 µW since this design has less number of transistors, 18. A Full Adder using 20 Transistors approach is better than others on area aspect. It occupies only 270.9 µm^2 only.

CONCLUSION AND FUTURE WORK

Adders are playing important roles for the operations like multiplication, filtering, counting etc. They form foundations for most of the bigger system designs. Here the XOR/XNOR gate design is effectively being implemented by pass-transistor logic. An important advantage of using this logic style is designing with less number of transistors. This work can also be implemented in future with other kind of fast adder sub-systems like carry look-ahead adder, carry-skip adder, ripple carry adder, carry chain adders, etc. ECAD tools like Digital Schematic (DSCH) and Microwind layout editor are used to implement this study. Same study can be further extended to multiplier circuits like array multipliers and Wallace-Tree multipliers. Multipliers can be designed efficiently using carry-save adders. Since, the multiplier can be designed using adders, this study helps to design multipliers with low power.

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