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Low Energy, Improved Speed and High Throughput CORDIC Cell to Improve Performance of Robots' Processor

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ABSTRACT

Robots are used in various real-time applications. The speed constraint in robotic system applications requires a real-time interface operation; this is a recent target in robotic research. The cost and size of a robotic system is often determined by hardware-based solutions. The coordinate Rotation Digital Computer (CORDIC) technique allows for an efficient execution of functions, such as inverse tangents and vector rotations, in the hardware. The CORDIC algorithm is very well suited for VLSI implementation due to the simplicity of the involved operations. This study proposed a full-adder based bit parallel iterative CORDIC circuit to improve the performance of robots' processor. The proposed full-adder and CORDIC circuit are designed and their layouts are generated by VLSI CAD tool. The parametric analysis is done using by BSIM4 analyzer. The output parameters such as propagation delay, area and power dissipation are calculated from simulated results of CORDIC cell. The proposed adder based CORDIC circuit designed for low energy, improved speed, low EPI and high throughput. The simulated result of proposed adder based CORDIC circuit is compared with other published CORDIC circuits. From the analysis of these simulated results, it was found that proposed adder based CORDIC circuit gives better performance in terms of power, propagation delay, speed, EPI and throughput than other published results. The results are extended to analysis of temperature coefficient, thermal conductivity and thermal flux for CORDIC cells' chip. The proposed circuit gives better tolerance of temperature and less leakage current than other adder based CORDIC cell.

Key words: CORDIC, full adder, robot, EPI, throughput

INTRODUCTION

In real-time digital control systems such as intelligent robot control system, it is essential to perform a large amount of computation at high speed because the robot must respond quickly to the environmental movement. The robotic system's applications require a real-time operation to interface speed constraints is one of the major trends in current robotic research. It is essential to perform a large amount of computation at high speed because the robot must respond quickly to the environmental movement (Shimabukurat *et al*., 1992). Most of the robotic system's applications require a real-time operation to interface speed constraints. There are also scenarios where area and power efficient solutions are valuable. These include robots in hospitals and home automation systems that are battery-driven and can accommodate only a small payload. Hardware-based solutions also have an impact on size and cost of overall system. Leena *et al*. (2009) considers a core

element of many robotic algorithms, namely, the rotation of vectors in a plane (and update of coordinates for a reference point on a mobile robot) and develops an area-efficient hardware-directed solution. Soft computing technologies were used to design a robust autonomous mobile robot control system, which is suitable for online applications with real-time requirements (Velagic *et al*., 2006).

The CORDIC algorithm is an iterative algorithm, which can be used for computation of trigonometric functions, multiplication and division (Volder, 1959). The CORDIC is very simple and iterative convergence algorithm that reduces complex multiplication, greatly simplifying overall hardware complexity. This serves as an attractive option to system designers as they continue to face the challenges of balancing aggressive cost and power targets with increased performance required in next generation signal processing solutions. The basic principles underlying the CORDIC based computation and present its iterative algorithm for different operating modes and planar coordinate system (Kumar and Sappal, 2011). This algorithm attracts more and more attention in elementary function evaluation and signal processing applications (Haviland and Tuszynski, 1980; Hu, 1992). The advances in VLSI technology have extended the application of CORDIC algorithm to the field of biomedical signal processing (Banerjee *et al*., 2001), Neural networks (Meyer-Base *et al*., 2003) and robotic exploration (Leena *et al*., 2009).

The bit parallel iterative CORDIC circuit may implement in robots' processor that is to improve speed and power. The core component of CORDIC circuits is designed in terms of transistor models for logic operation. The basic CORDIC has components such as register, multiplexer and full adder designed using by Pass Transistor Logic (PTL) that are used less number of transistor than existing circuit. According to number of transistor the circuits analyses for power dissipation, propagation delay, area, EPI, throughput, latency, temperature coefficient, thermal flux, thermal conductivity and leakage current. The existing adder circuits are implementing into CORDIC circuit and then compared to proposed adder based CORDIC circuit which gives better performance than existing adder based CORDIC circuit. The proposed CORDIC circuit compared with other existing CORDIC circuit in terms of power, maximum operating frequency, propagation delay, number of transistor and area which gives better results.

MATERIALS AND METHODS

Recent advances in VLSI have allowed the mapping of complex algorithms to hardware using systolic arrays with advanced computer arithmetic algorithms such as CORDIC algorithm. CORDIC have been used in robotics for inverse kinematics (Harber *et al*., 1988; Kameyama *et al*., 1989; Lee and Chang, 1987), for nonredundant robots and for control (Butner *et al*., 1988; Wang and Butner, 1987). According to Walker and Cavallaro (1994), CORDIC arithmetic in the novel design of special-purpose VLSI array, forming a key part of an efficient architecture for redundant robot kinematics computations. The proposed adder sacrificed area but it gives better performance in terms of power consumption and speed.

Proposed full-adder layout: The full-adder performs the computing function of the CORDIC. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. In this design, the three inputs have been designated as 'A', 'B' and 'C' (Velrajkumar *et al*., 2013). The LVS is analysed for the designed full adder circuit by using various methods. The generated full adder layout is shown in Fig. 1, which imposed parametric analysis.

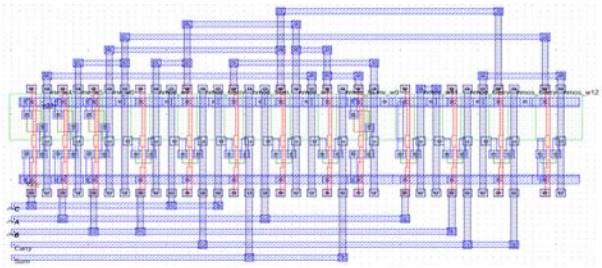

Fig. 1: Proposed full-adder layout

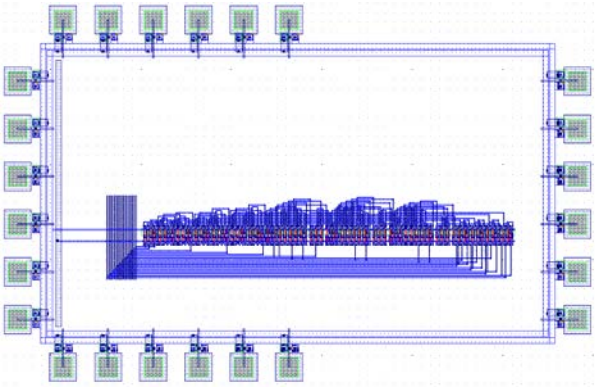

Fig. 2: Bit parallel iterative CORDIC layout

Bit parallel iterative CORDIC cell layout: The proposed CORDIC cell is designed using proposed adder and its combinational circuit. The bit parallel iterative CORDIC circuit has basic components such as register, multiplexer and full adder. All these basic components were designed using PTL technique. The proposed full adder based bit parallel iterative CORDIC circuit layout is shown in Fig. 2 for 65 nm CMOS feature size. The design aspects are started from hierarchy method. The multiplexers have been used in the CORDIC circuit for input and output signals selection. The multiplexer is implemented using pass transistor logic. This design is simple and efficient in terms of area and switching events. The pass transistor design reduces the parasitic capacitances due to short channel effect. According to Uyemura (2002), the selection input and its complementary inputs are fed into gate terminal transistors of 'A' and 'B', which reduced two transistors than CMOS design techniques. The output of multiplexer stage is passed as input to full-adder.

The truth table proposed for the bit-parallel iterative CORDIC circuit, which aided in the circuit development process, is presented in Table 1. The proposed truth table of bit parallel iterative CORDIC circuit for 'n' bit CORDIC cells where 'n' stands for number of stage. The inputs are get ascending order of binary number. The outputs depend upon mathematical calculations of CORDIC cells and control multiplexer cell. As per previous literature, the CORDIC cell is in algorithm mode which is changed into truth table verification mode by multiplexer based design. The author represents stages by binary ascending node authentication. So, this truth table can be verified to hardware CORDIC cells. Based on the selection input, bit words are stored in the register and are then transferred into the adder/substracter cell. Depending upon the register output, the appropriate full adder sum/carry are activated and the results calculated. The CORDIC circuit performs according to the mode of operation, which is illustrated in Table 1.

Table 1: Truth table for bit parallel iterative CORDIC

Inputs			Output		
X_0	Y_0	Z_0	X_n	Y_n	Z_n
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	1	1	0
1	1	1	0	0	1

RESULT AND DISCUSSION

In the proposed adder based bit parallel iterative CORDIC circuit to get a rough estimate of propagation delay, Microwind 3 simulation was performed for full adder and smaller but frequently occurring logic gates. The propagation delay for each of these components was used in estimating propagation delay for entire circuit. The worst-case scenario for the delay was determined to be one in which all inputs was set to logic low to high (000-111). The speed of proposed adder based CORDIC circuit can be determined by maximum delay along the critical path. The delay chain techniques have been developed to reduce the energy dissipation of CMOS design systems. The minimization of power can be carried out by reducing supply voltage, capacitance, number of transitions and optimized timing signals. By reducing V_{DD}, the energy dissipation decreases quadratically but delay increases and performance is degraded. A possible solution is using different supply voltages in different inputs of the circuit. The inputs not in critical path are supplied by lower voltages, while critical one by higher voltage. The proposed adder based CORDIC circuit transistor model output value of pull-up register is determine by considering the fan-out of CORDIC tie and number of devices in CORDIC tie. The pull-up register value is maintained between V_{OH} and V_{IL}. For reducing noise margin the channel resistance values should be maintains. According to layout editor, the channel resistance value can be estimated by Eq. 1:

$$\text{Channel resistance } (R_{\square}) = \frac{V_{DD} - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})} \quad (1)$$

The proposed CORDIC circuit is connecting regular tree structure, which may reduce channel resistance and critical path, which gives lower power dissipation and improved speed than other CORDIC circuits. The improved version of CORDIC circuit simulated results is shown in Table 2. The Energy Per Instruction (EPI) is product of capacitance toggled while processing the instruction and supply voltage of corresponding feature size (Hong *et al*., 2006). The EPI is a measure of amount of energy expanded by a circuit for each instruction that the circuit execute which gives power efficiency of circuit. It records the average amount of energy expanded per instruction processed by circuit. The EPI is calculated for four different types of adder based CORDIC cells in order of pico-Watts/Instruction Per Second (pW/IPS), which is denoted in Table 2. Generally, latency is reducing the speed of circuit which may defined as sum of total time in circuit and product value of number of stage and propagation delay of defined circuit (Muhammad *et al*., 2001; Mergen and Tong, 2007). The observation of proposed adder based CORDIC cell obtained lower latency than other adder based CORDIC cell, due to cell arrangements and less critical path in circuits. Throughput always equal to proportional to number of stage and inversely proportional to latency of defined circuit. According to circuit arrangement and number of transistor reduced, proposed adder based CORDIC cell gives better throughput than other adder based CORDIC cell.

Table 2: Power dissipation, delay, area, number of transistors, EPI, latency and throughput for bit parallel iterative CORDIC Cell

Parameters	CORDIC cell	65 (nm) 0.7 V	90 (nm) 1.0 V	130 (nm) 1.2 V	180 (nm) 2.0 V
MCIT 7T adder CORDIC	P_D (μW)	3.1	3.45	3.3	3.07
	τ (ps)	40	79	40	11.8
	Area (μm^2)	1095	1140	1656	7600
	No. of trans	98	98	98	98
	EPI (pW/IPS)	15.63	38.01	60.588	85.08
	Latency (ns)	2.4	2.47	2.54	2.59
	Throughput (Gbps)	0.42	0.405	0.3937	0.386
Mixed shannon adder CORDIC	P_D (μW)	3.15	9.46	3.166	2.9
	τ (ps)	19.8	19.8	58	39.6
	Area (μm^2)	1260	1305	1890	8463
	No. of trans	107	107	107	107
	EPI (pW/IPS)	16.58	39.589	64.566	88.857
	Latency (ns)	3.18	3.39	3.558	3.96
	Throughput (Gbps)	0.315	0.295	0.281	0.253
Shannon adder CORDIC	P_D (μW)	3.07	4.17	1.835	2.1
	τ (ps)	19.8	47.5	79	35.6
	Area (μm^2)	1632	1802	2560	11130
	No. of trans	119	119	119	119
	EPI (pW/IPS)	16.1	38.963	62.888	86.964
	Latency (ns)	2.91	2.94	3.079	3.35
	Throughput (Gbps)	0.344	0.34	0.324	0.299
Proposed adder CORDIC	P_D (μW)	1.94	1.033	1.705	1.96
	τ (ps)	15.8	23.8	35	15.8
	Area (μm^2)	1280	1344	1900	8528
	No. of trans	104	104	104	104
	EPI (pW/IPS)	14.63	37.76	56.159	83.206
	Latency (ns)	2.015	2.023	2.035	2.058
	Throughput (Gbps)	0.496	0.494	0.492	0.486

P_D: Power dissipation, τ: Propagation delay, No. of trans: Number of transistors, EPI: Energy per instruction

Table 3: Comparison of proposed CORDIC Cell's power dissipation, delay, area, number of transistors and maximum frequency

Approach	P_D (μW)	Reduction (%)	τ (ps)	Reduction (%)	Area (μm^2)	No. of transistor	Maximum frequency (GHz)
Proposed	1.94	-	15.8	-	1280	104	63.29
Reddy and Reddy (2009) CORDIC	2.3606	17.82	4.4×10^3	99.64	2558.05	-	0.23
Musicer and Rabaey (2000) CMOS	3.45×10^3	99.94	7.57×10^3	99.79	-	11500	0.13
MCML (No. adaptive pipelining)	18.6×10^3	99.98	3.29×10^3	99.51	-	16500	0.304
MCML (with adaptive pipelining)	18.6×10^3	99.98	2.94×10^3	99.46	-	16500	0.34
Chandrakanth and Kumar (2011)							
Basic CORDIC	1261.35	99.84	-	-	3328.19	-	-
Control CORDIC	1175.95	99.83	-	-	3328	-	-
Parallel angle recoding	5612.95	99.96	-	-	67274	-	-
Proposed CORDIC	1687.99	99.88	-	-	24512	-	-

The proposed adder based CORDIC circuit's simulation results were then compared with the CORDIC cells proposed by Reddy and Reddy (2009), Musicer and Rabaey (2000) and Chandrakanth and Kumar (2011) with respect to propagation delay, power dissipation, number of transistors, area and maximum frequency; the results are shown in Table 3. The Reddy and Reddy (2009) circuits are compared with the proposed CORDIC circuit. The proposed circuit provides exceptional improvement with respect to power dissipation, area and propagation delay. The architecture of the CORDIC cell in Reddy and Reddy (2009) was processed through an ASIC design with the help of Verilog HDL; it consumed more power with higher delays compared with the proposed full adder-based CORDIC cell (implemented with PTL logic), which offered 17.82 and 99.64% improvement, respectively. Musicer and Rabaey (2000) proposed a MCML-based CORDIC and a CMOS CORDIC that were compared with the proposed PTL-based CORDIC circuit. The proposed circuit showed exceptional performance with respect

to number of transistors, delay, maximum frequency and power dissipation because of its NFET drivability. Chandrakanth and Kumar (2011) presented a basic CORDIC, a control CORDIC, a parallel angle recoding circuit and a proposed CORDIC that were compared with the proposed CORDIC circuit in terms of power dissipation and area. The improved parallel angle recoding circuit was used to design the extra logic for the CORDIC hardware system. The extra logic consumed more power, created transition delays and occupied more area. The proposed circuit consumed less power and occupied less area because fewer transistors were used.

Thermal effect in CORDIC cell: The conduction of temperature in components affects the sensitivity of devices; in integrated circuits, temperature conduction determines their power dissipation capabilities. Determining the thermal properties of a CORDIC cell (such as the thermal flux and thermal conductivity) is an important and challenging layout task. Feature size geometrics can shrink and device densities can increase when power can be drastically increased in the integrated circuit. Therefore, the dissipation of heat is important in maintaining an optimal operating temperature. Conduction, radiation and convection are the three most common ways to dissipate heat from a device. The measure of an object's ability to dissipate heat or the heat efficiency at its boundary is deemed its thermal resistance. Table 4 shows the operational conditions of the proposed adder-based CORDIC cell layout parameters in robotic applications for 65 nm feature size.

The temperature analysis of layout has done by BSIM4 advanced analyzer. The junction temperature is important to find thermal resistivity and conductivity, which is finalized the output current in output node at maximum temperature. According to Remsburg (2001), the layout temperature is varying with feature size corresponding 100-120°C. In BSIM4 analysis, temperature varied from -40-120°C. In this analysis, the CORDIC layout has taken maximum junction temperature. The junction temperature calculated for determines the necessity of heat sink, which is denoted in Eq. 2:

$$T_J = T_A + P \times \theta_{JA} \tag{2}$$

The ambient temperature is breaking through point of current flow maximum which depends upon junction capacitance and power dissipation. The measurement and analysis has done using by BSIM4 and Eq. 3 is illustrated:

$$\theta_{JA} = \frac{T_J - T_A}{P} \tag{3}$$

In the other way of ambient thermal resistance also calculated for lower feature size which is indicated in Eq. 4:

$$\theta_{SA} = \frac{T_{JMAX} - T_A}{P - \theta_{JC} - \theta_{CS}} \tag{4}$$

Table 4: Operating condition of proposed adder based CORDIC cell layout parameter for 65 nm feature size

Parameters	Values
Dimensions (μm)	$80\times16\times1.5\times10^{-9}$
Number of layers	11
Layer thickness (μm)	1.5×10^{-9}
Power (μW)	1.94
Maximum T_A (°C)	60
Maximum T_J (°C)	120

Table 5: Leakage current, temperature coefficient, thermal conductivity and thermal flux of the CORDIC cells for 65 nm feature size

CORDIC cell	Leakage current (mA)	Temperature coefficient (mV/°C)	Thermal conductivity (W/m°C)×10^{-8}	Thermal flux (W/m^2)×10^{-6}
MCIT 7T	0.179	3.1	5.16	8.256
M. Shannon	0.075	3.7	5.25	8.4
Shannon	0.048	1.6	5.12	8.192
Proposed	0.025	1.8	3.23	5.168

Based on the results of simulation, it is clear that the proposed adder based CORDIC circuit design offers exceptional performance with respect to thermal conductivity and thermal flux compared to the other three adder-based CORDIC cells for 65 nm feature size as shown in Table 5. As for the device analysis, this article may involve the study of temperature effects, including chip ambient temperature, assembly tolerance temperature and parasitic effect temperature. Based on the low power dissipation and improved speed, this thesis may be useful for all mobile devices that require minimized power to accommodate many advanced features. The transistors that have been used in this CORDIC circuit were properly connected to the tree by seriously considering the critical path; they consistently provide exceptional performance with respect to propagation delay, power dissipation and speed.

Parameter component analysis: The dynamic power dissipation is calculated in CORDIC circuit in terms of output capacitance charged or discharged during charge flow in output capacitance. The dynamic dissipation may calculate using by Eq. 5:

$$P_{dynamic} = \alpha C_L V_{DD}^2 f \tag{5}$$

where, α is switching activity (the average number of high-to-low transitions per cycle), C_L is load capacitance, which derived from layout analysis, V_{DD} is supply voltage and f is operating frequency. According to CORDIC circuits, supply voltage depends upon feature size, which is denoting in Table 2. The operating frequency varied in adder based CORDIC circuits from 0.23-4.3 GHz. The average number of high to low transition occur in our proposed circuit is 0.515 ns. The dynamic power dissipation is measured according to above mentioned conditions. Since, we will be focusing on dynamic power, the total power dissipation can be approximated as Eq. 5 and the energy consumption during the time interval [0, T] is given by:

$$E = \int_0^T P(t)dt \propto V_{DD}^2 fT = V_{DD}^2 N_{cycle} \tag{6}$$

where, P(t) is total dynamic power dissipation at t and N_{cycle} is number of clock cycles during the interval [0, T]. Equation 6 indicates that a significant energy saving can be achieved by reducing the supply voltage V_{DD}. A decrease in supply voltage by a factor of 2 yields a decrease in the energy consumption by a factor of 4 (Chen, 2006).

The total dynamic power dissipation measured from CORDIC cell layout output parameters, which derived from output 'x_n' of CORDIC circuit. The total power dissipation depends upon layout channel effect. The proposed adder based CORDIC circuit gives less power dissipation due to lower channel effect, less critical path and minimized transition time. According to PTL design concept, we have chosen only logic '1' as a source input of all transistors. So, the power dissipation would be happened only dynamic. The operating frequency 'f' always equal to dynamic power dissipation and reciprocal of square of supply voltage and load capacitance which is shown in Eq. 7:

$$f = \frac{P_D}{C_L V_{DD}^2} \tag{7}$$

According to Eq. 7 the capacitance varied from 10-100 fF and speed of overall CORDIC circuits varied to approximately 4.3-0.23 GHz respectively. The dynamic power dissipation determines according to switching events of transistor, which is illustrated in Table 2. The energy gap of load capacitance is depends upon supply voltage which leads to performance degradation. When scaling technique is Ultra Deep Sub Micron (UDSM) device, the current passing through the terminal is channelized. So, the voltage energy saving is satisfied by UDSM. Our proposed adder based CORDIC circuit gives higher speed (4.3-0.88 GHz) corresponding to 10-100 fF, than other reference circuits that are shown in Fig. 3.

The bit parallel iterative CORDIC circuits' capacitance versus leakage current is shown in Fig. 4.

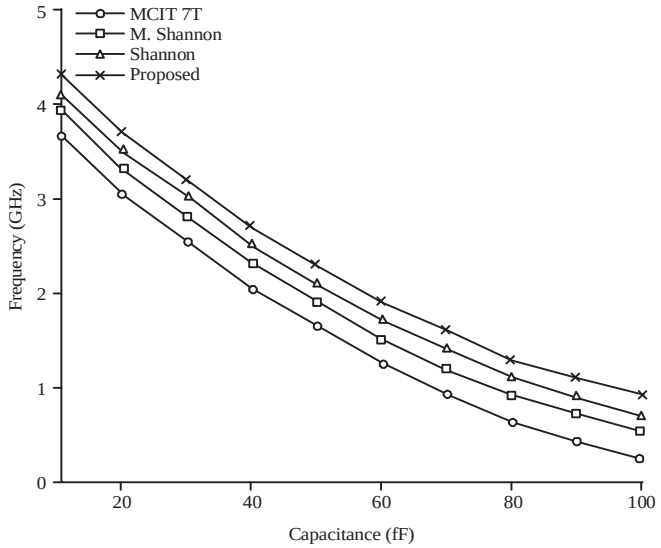

Fig. 3: Capacitance versus operating frequency for different adder based CORDIC cell

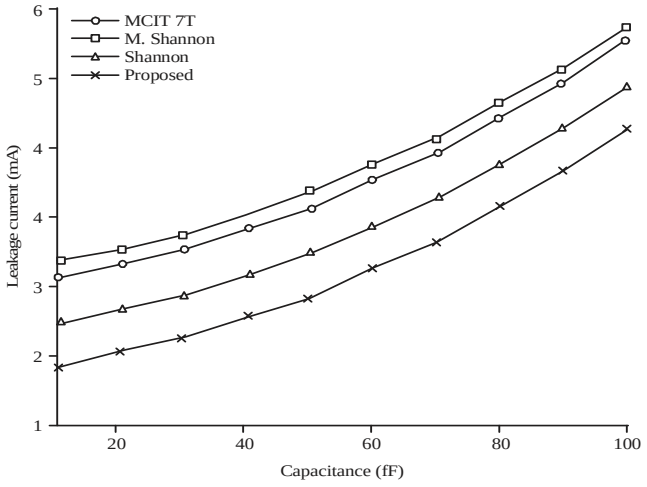

Fig. 4: Capacitance versus leakage current for different adder based CORDIC cell

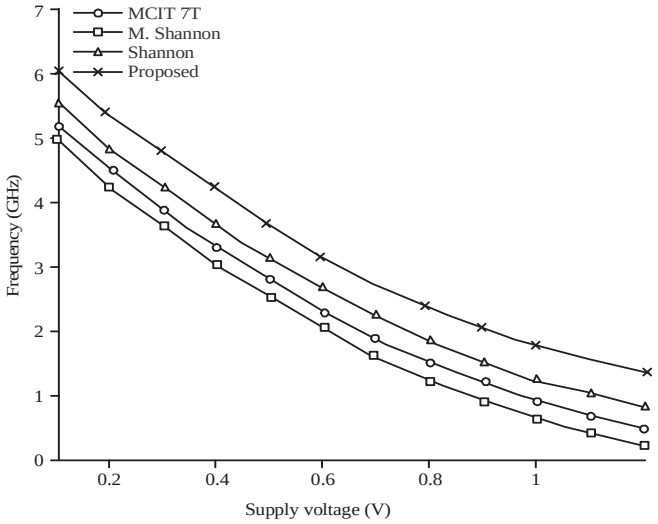

Fig. 5: Supply voltage versus operating frequency for different adder based CORDIC cell

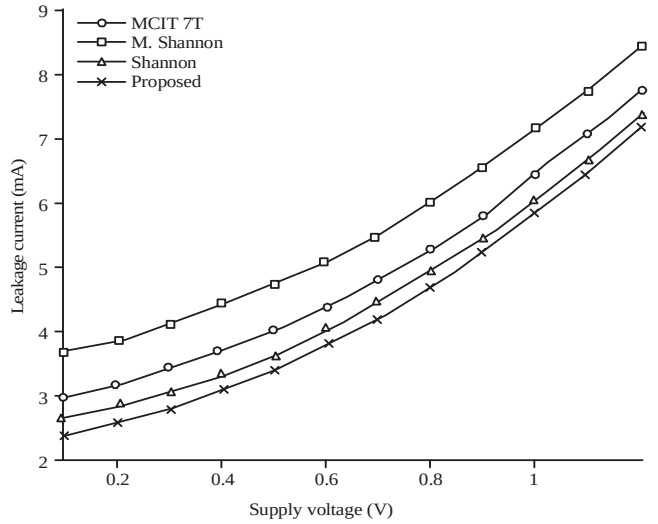

Fig. 6: Supply voltage versus leakage current for different adder based CORDIC cell

The shrinkage of gate capacitance and gate area of MOSFET is changing charge channel values, which increased leakage current due to improper arrangement of transistor tree structure and longer critical path being in circuit (Senthilpari *et al*., 2009). The proposed adder based CORDIC circuit has lower leakage current than other CORDIC circuit due to reduce the critical path. The pass logic design basically reduced two transistors per logic that means the channel effect is reduced. The proposed adder based CORDIC circuit has lower operating current than other CORDIC to trade-off in critical path. The maximum leakage current can be found from PMOS to NMOS aspect ratio (W/L) of CMOS inverter, which also affects the performance of CORDIC circuit. Reducing operating voltage is one of the most promising techniques for reducing dynamic power consumption:

$$f = \frac{k\left(V_{DD} - V_{th}\right)^{\alpha}}{V_{DD}} \tag{8}$$

where, k, a design-specific constant and α, a process-specific constant ranging from 1-2. As a result, for low values of Vth (threshold voltage) and α = 2 and all other things being equal, halving V_{DD} implies halving frequency, f (Chen, 2006). According to our design aspect of logic cell, the design specific constant k is 3.12 for six metal layers, α is 2 for pass transistor technique. According to body bias condition, Vth can be modified. As per CMOS design rules, for feature size 65 nm, if supply voltage is 0.7 V and corresponding Vth is 0.021 V. The proposed adder based CORDIC circuit shown better speed than other existing CORDIC circuit due to design specific ratio. The variation of speed is compared with existing adder based CORDIC circuit which is shown in Fig. 5.

The supply voltage versus dynamic leakage current (mA) of CORDIC circuits is shown in Fig. 6. As seen from Fig. 6, the maximum operating current of CORDIC circuit increases as the supply voltage increases, irrespective of design technique. Other important observation is that the proposed adder based CORDIC circuit show lower leakage current compared to other CORDIC circuits.

CONCLUSION

The bit parallel iterative CORDIC circuits were designed using PTL logic based proposed adder, multiplexer and registers. The proposed adder based CORDIC circuit outperforms the other adder based CORDIC circuits. The proposed adder based CORDIC cell achieves better performance in terms of power dissipation, propagation delay, area, EPI, latency and throughput due to less critical path compared to other CORDIC circuits. The proposed circuit can be used to improve the performance of robots' processor due to its lower delay, lower power dissipation, improved speed and high throughput. The proposed adder based CORDIC circuit can be with-stand temperature and assumed to be giving less leakage current than other CORDIC circuit for ambient temperature.

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