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CMOS VLSI Design of Low Power SRAM Cell Architectures with New TMR: A Layout Approach

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ABSTRACT

Rapid increase in technology for faster and smarter innovations that smoothens the needs of humans resulting in use of super tech gadgets, which use memory, such as, RAM. To meet the increasing demands, the size is getting reduced and the need to save power arises which reduces the equipment for cooling processes and maintenance. The SRAM cells with lower power dissipation and proper read and write stability is required. This study deals with the design of SRAM cells with low power dissipation in comparison with the conventional SRAM cell design. The SRAM cell design ranges from 3-14T depending on the importance of the application. Here we choose the 6T SRAM cell. The elementary structure uses pass transistor and CMOS, while the proposed SRAM consists of Transmission gates, CMOS, Pseudo-NMOS. This proposed model is compared with two other models of varied 6T SRAM cell. This study also exemplify with the new Triple Modular Redundancy (TMR) techniques with SRAM cell architecture and the layout area with power dissipation results are compared with the existing voting mechanism in 50, 70 90 and 120 nm foundry fabrication process technologies. It is apparent that the proposed voting circuit produces less area at the cost of power dissipation.

Key words: CMOS logic, low power, layout, microwind, SRAM cell

INTRODUCTION

With the advancements in technology that are happening in the world, the demand for large storages of data is increasing in a way that needs to be faster than the existing technologies (Yeap, 1998). For it, low power Random Access Memory (RAM) is the usable technology in order to meet the demands. RAM has two classifications Static RAM (SRAM) and Dynamic RAM (DRAM). The SRAM is the most preferred of both because it offers less leakage current unlike in that of DRAMs because SRAMs do not use capacitors for storing data. The RAM is basically used to store data and retrieve back upon requirements. Another advantage of SRAM over DRAM is that it has higher data retaining ability. Additionally, it easily exhibits easy interface for the users benefit (Weste *et al*., 2012).

The paper has discussions on various models of an SRAM cell with elaborated explanation of their operations. This starts with conventional SRAM cell, which uses 6 transistors, shortly called as 6T SRAM cell, to store a bit and observed to have low power dissipation and leakage power as well. Then, we shall move into some proposed models, which have more functional advantages with respect to data retention stability, power consumption, leakage power etc. However, they have more area occupancy, which can be overlooked for the sake of aforementioned benefits. Briefing of the

functioning of the circuits along with issues and benefits will be done in the following matter. This will be followed by power analysis of all the circuits implemented for better understanding of them in the intended manner (Navabi, 2006).

To implement circuits, software named Digital Schematic (DSCH) editor will be effectively used (Rajesh *et al*., 2014). This software has the ability to automatically generate Verilog code. Microwind is another software which we will need to perform power analysis, which uses Verilog codes to form layouts of the circuits and subsequently, determining the layout area and power dissipation (Elamaran *et al*., 2012; Subramani *et al*., 2014).

The sole objective of this study with novel SRAM cell architectures along with the TMR techniques to improve the reliability of the system. As case study, the SRAM cell write operation is tested with a conventional and a proposed voting circuits and the performance metric results line the layout area and power dissipation are compared.

MATERIALS AND METHODS

Sram cell-6T architecture: Conventional 6T SRAM cell is the most typical type which can store binary information. A latch is created by making use of two CMOS back-to-back inverter circuits that is responsible for holding data. It is found that the cell is more stable during read operation than during write operation (Pedroni, 2008; Subhamkari and Kumar, 2013). Power supply should be continuously supplied and during this time data can be made to retain. Figure 1 shows a 6T SRAM cell. The two transistors placed outside inverter circuits are called access transistors as they control the access of data to the cell during read and write operations (Kaushik *et al*., 2014; Athe and Dasgupta, 2009; Yu *et al*., 2010).

Bit Line (BL) and Word Line (WL) are needed to perform read and write operations. The BLB is the complementary line to BL, as shown in figure. Initially, WL line is kept low. Write operation can be performed by raising the BL line to the required state and then pull the WL line to high state. This way, the binary information moves into the back-to-back inverter circuits, which holds the data on BL line. The operation goes as follows, the BL line drives second inverter circuit and its inverted output drives the first inverter circuit giving both original and inverted signals of BL line.

To do read operation, two capacitors are required to be placed at the BL and BLB lines, respectively. Both the capacitors need to be pre-charged and one of the capacitors will be pulled low due to the zero bit present at that respective node (Athe and Dasgupta, 2009). Figure 2 shows the timing diagram of 6-T SRAM cell output.

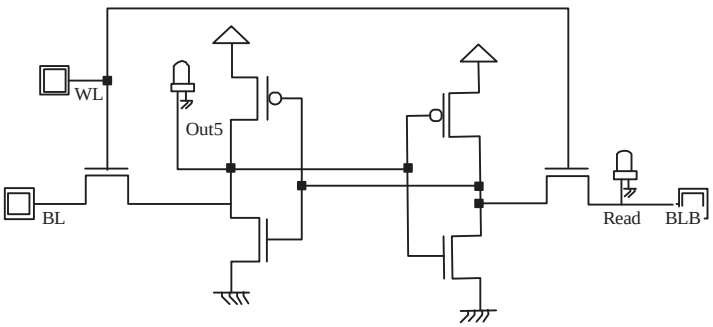

Fig. 1: 6-T SRAM cell

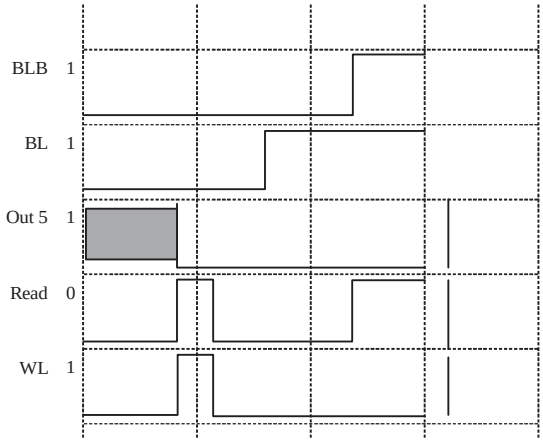

Fig. 2: Timing diagram result of 6T SRAM cell

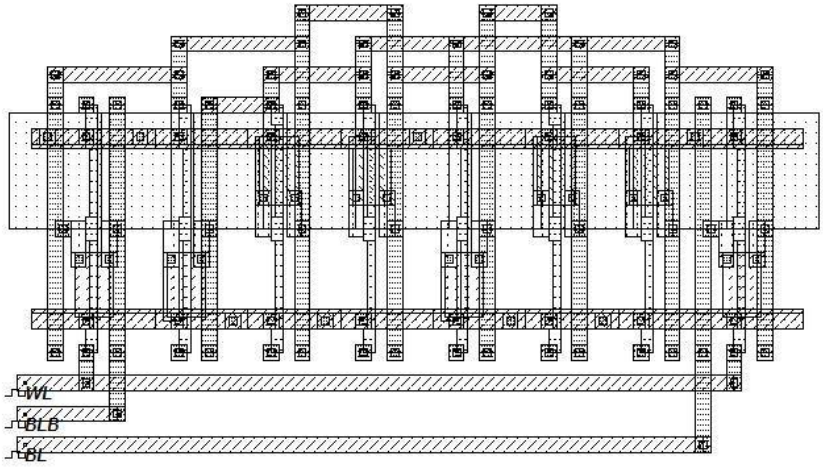

Fig. 3: Layout of 6T SRAM cell

```
module SRAM_6T (WL, BL, BLB);
      input WL, BL, BLB;
      nmos #(10) nmos (BLB, w2, WL);
      nmos #(31) nmos (w4, vss, w2);
      pmos #(31) pmos (w2, WL, w4);
      nmos #(31) nmos (w2, vss, w4);
      pmos #(31) pmos (w4, WL, w2);
      nmos #(31) nmos (w4, BL, WL);
endmodule
      #1000 WL=~WL;
      #2000 BL=~BL; #3000 BLB=~BLB;
```

The above written code is the Verilog program for 6T cell and layout of 6-T SRAM cell as shown in Fig. 3.

Modified sram cell architecture: This cell is similar to conventional model in many ways except in performance and design (Majumdar and Basu, 2011). Design modifications done in this cell is

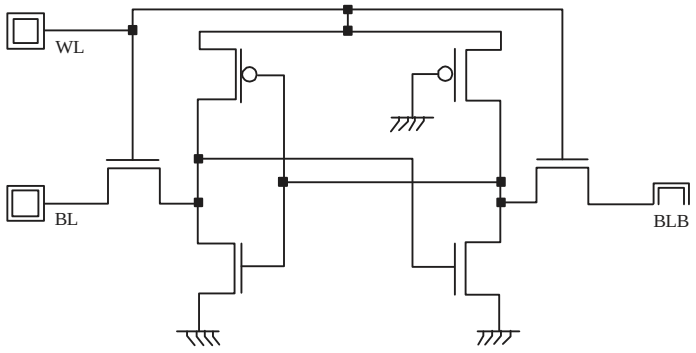

Fig. 4: Modified 6-T SRAM cell

only in the 2nd inverter circuit which uses a different MOS technology model: Pseudo NMOS technology, while in conventional cell, both inverters are of CMOS technology. The pseudo NMOS technology gives additional benefits over CMOS technology such as low gate capacitance which offers faster switching ability. Figure 4 presents the modified 6T SRAM cell.

This cell has same area occupancy as that of conventional model but is effective in terms of power dissipation, which is found to be lower than the previous model. The data retention stability also increases due to the pseudo NMOS technology used (Elamaran and Upadhyay, 2013; Uyemura, 2006; Yeap, 1998). Its working is totally similar to that of the above model.

```
module prj_sram_6t_pmos (WL, BL, BLB);
    input WL, BL, BLB;
    nmos #(10) nmos (BLB, w2, WL); //1.0u 0.12u
    nmos #(24) nmos (w4, vss, w2); //1.0u 0.12u
    pmos #(31) pmos (w2, vdd, vss); //2.0u 0.12u
    nmos #(31) nmos (w2, vss, w4); //1.0u 0.12u
    pmos #(24) pmos (w4, vdd, w2); //2.0u 0.12u
    nmos #(24) nmos (w4, BL, WL); //1.0u 0.12u
endmodule
    #1000 WL=~WL;
    #2000 BL=~BL;
    #3000 BLB=~BLB;
```

The above written code is the Verilog program for modified 6T cell.

Sram cell architecture using transmission gates: This new model that will be discussed is not solely based on pass transistors but also on transmission gates. Transmission gates have to replace the pass-access transistors of the conventional model. The pmos and nmos transistors can transmit only strong 1 and strong 0, respectively and poor 0 and poor 1, respectively. This issue can be resolved with the usage of transmission gates which can transmit both 1 and 0 bits in strong manner (Brown *et al*., 2008; Hussain and Jahinuzzaman, 2012). Figure 5 shows the SRAM model-I. With the use of transmission gates, area occupied is increased highly relative to conventional model but its usefulness surely precedes its one disadvantage (Weste *et al*., 2012). Also, this cell produces very low power dissipation. The cell operation (read and write) is identical to that of above cells (Yu *et al*., 2010).

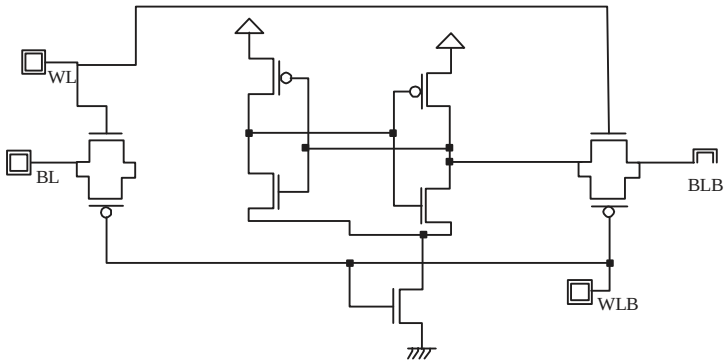

Fig. 5: SRAM model-I

```
module 6T SRAM_6 (in3, in5, in4, out3);
      input in3, in5, in4;
      output out3;
      nmos #(10) nmos (w3, out3, in3); //1.0u 0.12u
      pmos #(10) pmos (w3, out3, in5); //2.0u 0.12u
      nmos #(38) nmos (w6, w5, out3); //1.0u 0.12u
      pmos #(45) pmos (out3, vdd, w6); //2.0u 0.12u
      nmos #(45) nmos (out3, w5, w6); //1.0u 0.12u
      nmos #(17) nmos (w5, vss, in5); //1.0u 0.12u
      pmos #(38) pmos (w6, vdd, out3); //2.0u 0.12u
      nmos #(38) nmos (w6, in4, w8); //1.0u 0.12u
      pmos #(38) pmos (w6, in4, in5); //2.0u 0.12u
endmodule
      #1000 in3=~in3;
      #2000 in5=~in5;
      #3000 in4=~in4;
```

The above written code is the Verilog program for SRAM cell model-I.

Proposed sram cell architecture: This model is again similar to the above mentioned model-1 except a pseudo NMOS technology is used on second inverter. The added advantages are that this cell has low power consumption and more data retention stability (Navabi, 2006). Besides, this has high area occupancy. Figure 6 and 7 depicts the SRAM model-2 and the layout, respectively.

```
module 6T SRAM_4 (in3, in5, in4, out3);
      input in3, in5, in4;
      output out3;
      nmos #(10) nmos (w3, out3, in3); //1.0u 0.12u
      pmos #(10) pmos (w3, out3, in5); //2.0u 0.12u
      nmos #(31) nmos (w6, w5, out3); //1.0u 0.12u
      pmos #(45) pmos (out3, vdd, in5); //2.0u 0.12u
      nmos #(45) nmos (out3, w5, w6); //1.0u 0.12u
      nmos #(17) nmos (w5, in5, in5); //1.0u 0.12u
      pmos #(31) pmos (w6, vdd, out3); //2.0u 0.12u
      nmos #(31) nmos (w6, in4, w8); //1.0u 0.12u
      pmos #(31) pmos (w6, in4, in5); //2.0u 0.12u
endmodule #1000 in3=~in3;
#2000 in5=~in5;
#3000 in4=~in4;
```

The above written code is Verilog code for proposed SRAM cell.

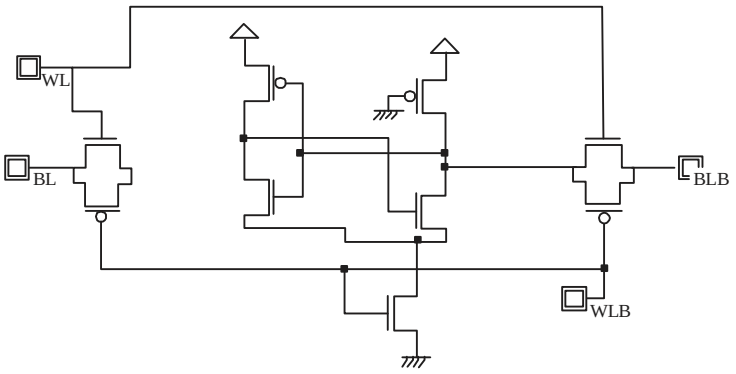

Fig. 6: Proposed SRAM cell

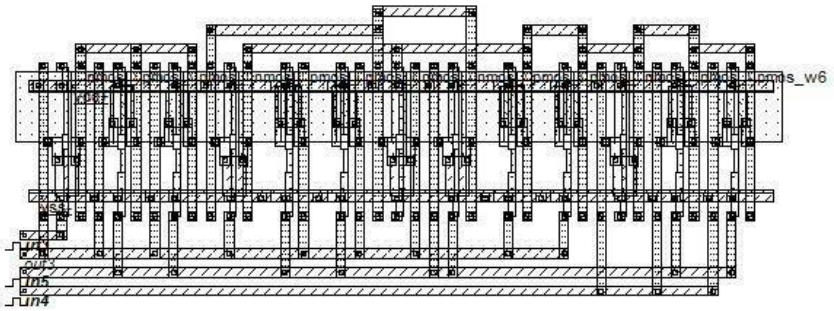

Fig. 7: Layout of proposed SRAM cell

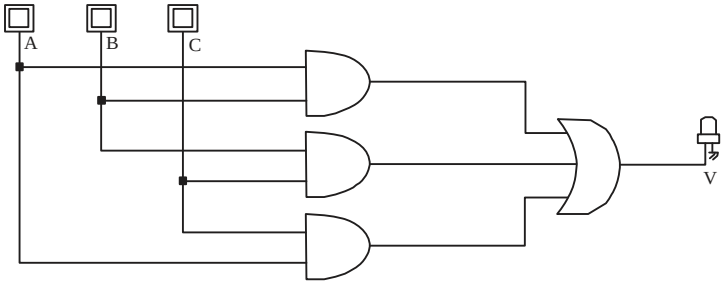

Fig. 8: Conventional voting circuit

Existing voting methodology: The TMR is the mostly useful technique to improve the reliability of the system if the Single Event Upset (SEU) kind of fault is occurred (Marques *et al*., 2010). The system should obtain the fault-free response by means of having three copies of the original circuit module and finding the majority out of them (Pagliarini *et al*., 2013; Kshirsagar and Patrikar, 2009). This conventional approach is shown in Fig. 8. This voter output can be expressed as follows:

$$V = AB+BC+CA \quad (1)$$

Sram write using existing voter circuit: The SRAM write operation is tested with the existing voter circuit and is shown in Fig. 9. To induce an fault in the circuit, a fault injection model is used

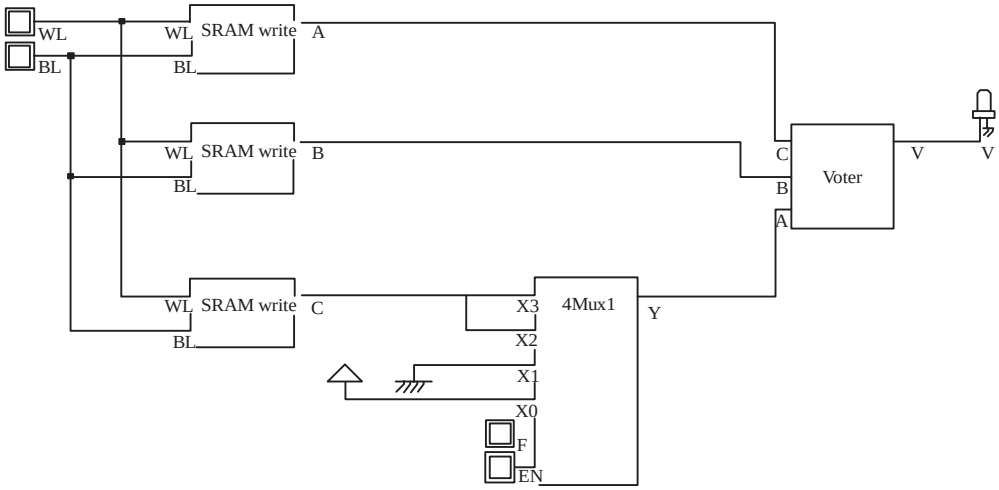

Fig. 9: SRAM write operation with conventional voting mechanism

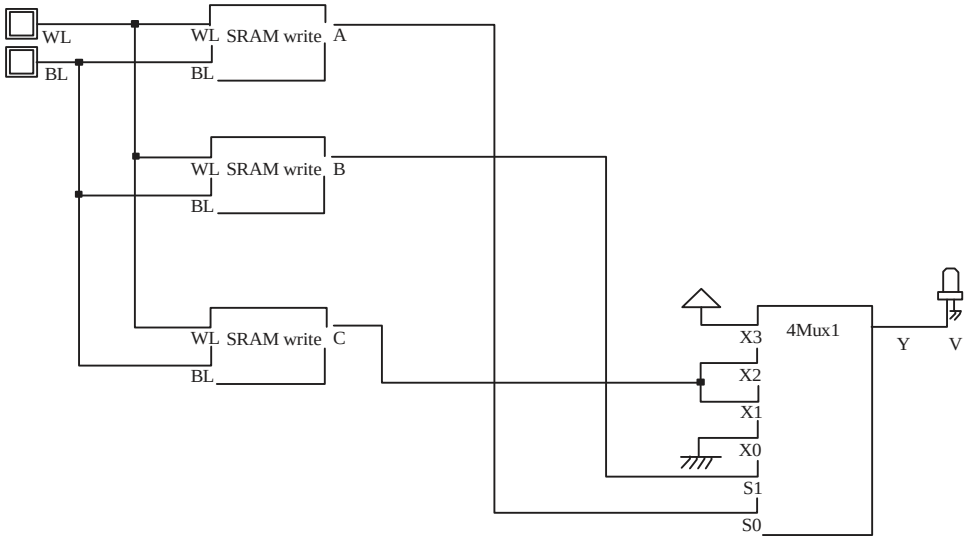

Fig. 10: SRAM write operation with proposed voting mechanism

here. The fault injection model contains a 4-to-1 multiplexer which obtains a fault-free data to the output if 'F' is '0'. If 'F' is '1' and 'EN' is '0', the fault '0' is injected. If 'F' is '1' and 'EN' is '1', the fault '1' is obtained as the multiplexer output.

Proposed voting circuit: The proposed voting methodology contains only a 4-to-1 multiplexer to determine the majority of the input. This circuit consumes very less layout area as compared with a conventional voting circuit. A SRAM write operation with this proposed voting mechanism is shown in Fig. 10. The first and fourth data line of the multiplexer are '1' and '0', respectively. The second and the third data line are tied with the output of the third module. The working of a multiplexer is described in the Table 1 and is easy to implement to obtain the majority function.

Table 1: Multiplexer role in a voter circuit

S1	S0	V
0	0	1
0	1	Output of 'C'
1	0	Output of 'C'
1	1	0

If A = B = C = 0, which becomes S1 = S0 = 0. If the fault is occurred at the output 'C' i.e., C = 1, the output becomes '0', which is the majority one. Similarly, if A = B = C = 1, which becomes S1 = S0 = 1. If the fault is occurred at the output 'C' i.e., C = 0, the output becomes '0' which is the majority one. Let the fault is occurred at the output of 'A', when A = B = C = 0. That is the output of 'A' becomes '1'. This creates S0 = 0 and S1 = 0 and the multiplexer obtains the output of 'C' as the output which is the majority here. Similarly, if the fault is occurred at the output of 'A', when A = B = C = 1. That is the output of 'A' becomes '0'. This created S0 = 0 and S1 = 1 and the multiplexer produces the output of 'C' as the output, which is again the majority here.

RESULTS

This section has the estimated values of power dissipation for the following models- 6T SRAM cell, Modified SRAM cell, SRAM cell model-I and proposed SRAM cell. The results are available in Table 2. The present proposed method results are compared with the previous studies (Kaushik *et al*., 2014). It is apparent that the proposed 6-T SRAM cells are good with low power dissipation for the 70, 120 and 180 nm technologies. The below tabulation justifies all the mentioned statements on power consumption comparisons. Table 3 presents an information on layout areas of various designs presented here and compared with the previous studies (Kaushik *et al*., 2014). The proposed SRAM cells are having the similar performance compared with the previous studies. Evidently, it can be said that the layout area is strictly dependent on the number of the transistors and other components and not MOS technology. The utility of the tools like DSCH and Microwind is good for measuring these performance metrics like layout area, number of transistors and power dissipation.

Power and layout area comparison with voting circuits: The schematics which are generated using the DSCH software tool can be converted to the Verilog Hardware Description Language (HDL). This script is compiled using the Microwind layout editor software tool to generate a layout with 50, 70, 90 and 120 nm fabrication process foundry technologies. The power dissipation of the SRAM cell with a proposed voter circuit consumes more power for 90 and 120 nm technologies. The proposed power dissipation results are obtained in Fig. 11 compared with the existing voting approach (Oliveira *et al*., 2007). Figure 12 shows the layout area convey that the SRAM cell with a proposed voter circuit occupies very less area in all the nanometer fabrication process foundry technologies compared with the existing voting approach (Oliveira *et al*., 2007). The reason behind this is, the SRAM cell with conventional voter circuit has 49 nMOS and 43 pMOS transistors i.e., with total of 92 transistors. The SRAM cell with a proposed voter circuit has 36 nMOS and 30 pMOS transistors i.e., with total of 66 transistors. These transistors count are depicted in Fig. 13 and 14 for the conventional voting approach and proposed voting approach, respectively. Figure 15 shows that the power dissipation result of the SRAM cell write operation with a proposed voting circuit with 44.278 μW.

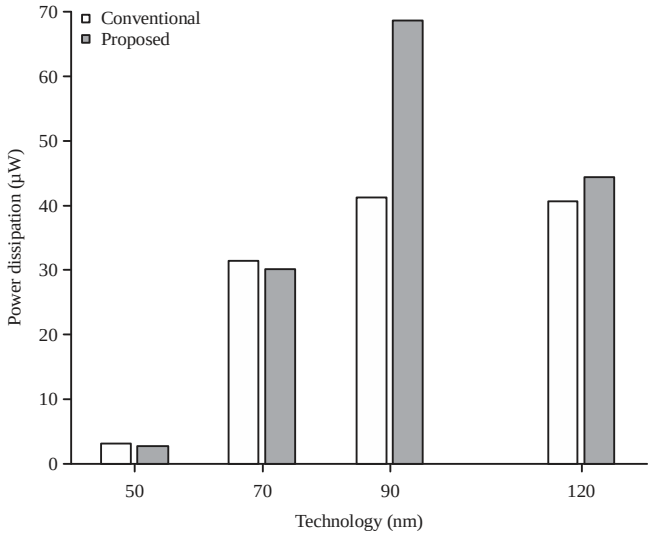

Fig. 11: Comparison of power dissipation results

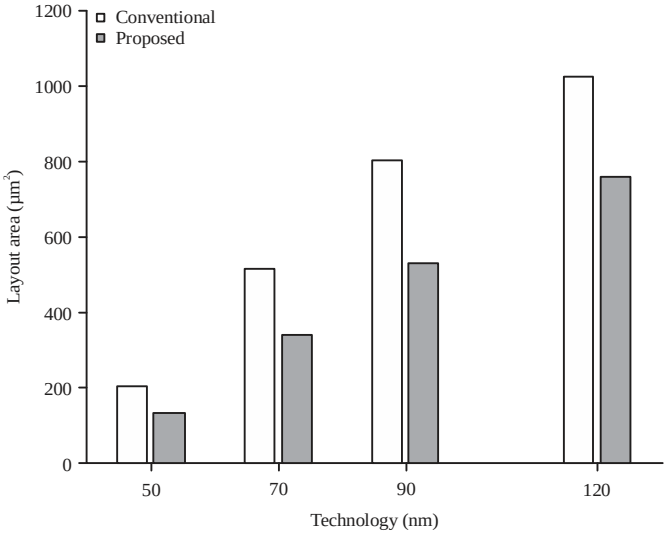

Fig. 12: Comparison of layout area results

Table 2: Power dissipation results

	Technology (nm)		
Designs	70	120	180
6-T SRAM cell Kaushik *et al*. (2014)	0.198 µW	0.146 µW	0.217 µW
Modified 6T SRAM cell	0.139 µW	0.129 µW	0.213 µW
SRAM cell Model I Kaushik *et al*. (2014)	3.015 µW	3.442 µW	21.585 µW
Proposed SRAM cell	2.411 µW	2.580 µW	17.536 µW

Table 3: Average power dissipation

Designs	No. of transistors	Layout area (μm^2)
6-T SRAM cell Kaushik *et al*. (2014)	6	87.7
Modified 6T SRAM cell	6	87.7
SRAM cell model-I Kaushik *et al*. (2014)	9	147.3
Proposed SRAM cell	9	147.3

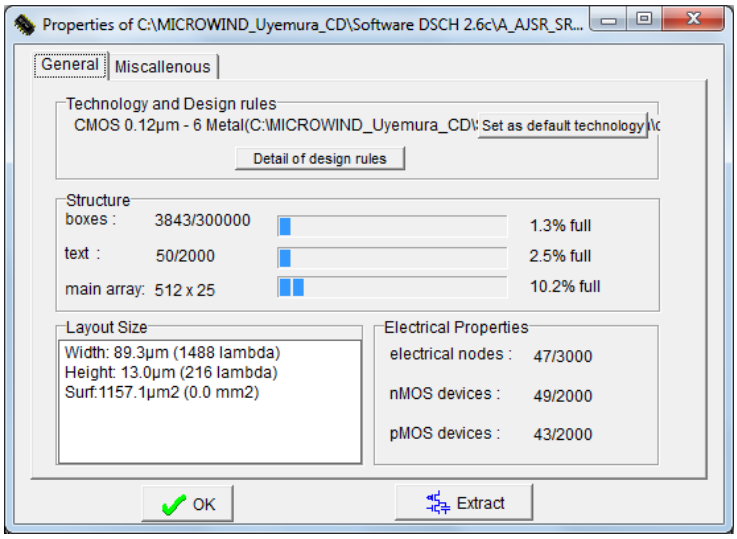

Fig. 13: Transistors count and layout area results with conventional voting circuit

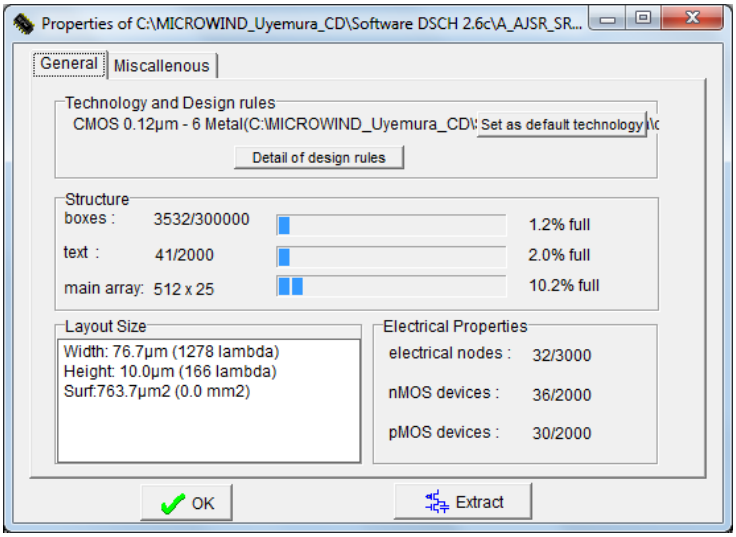

Fig. 14: Transistors count and layout area results with proposed voting circuit

DISCUSSION

This study dealt with a conventional 6T SRAM model improvising subsequently in the later models. All the justifications and explanations have been appropriately briefed in the above discussions. Power analysis have been performed and organized well in the above division. The area occupancy has proven to be disadvantageous in the improvised models, but it can be overlooked for the benefits in power consumption. Also the principle of TMR concept is implemented with SRAM write operation using a conventional and a proposed voting mechanism. The layout area and power dissipation results are taken as performance metrics for the comparison. The proposed SRAM cells offer a better power dissipation results at the cost of layout area

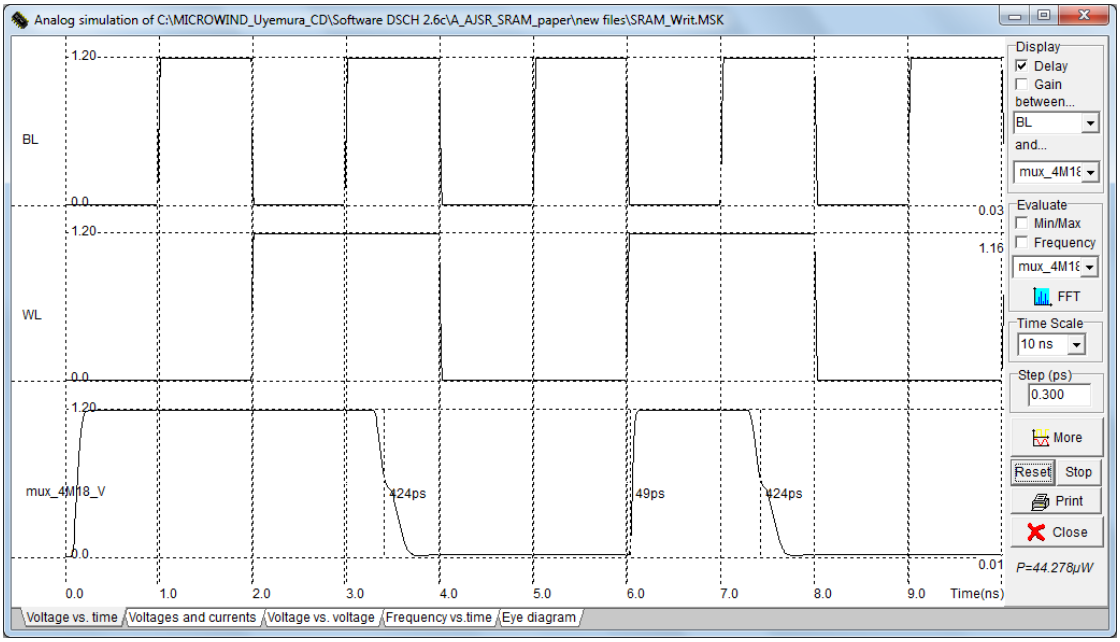

Fig. 15: Power dissipation result with a proposed voting circuit for 120 nm process

compared with the studies made by Kaushik *et al*. (2014). The proposed TMR with SRAM cell offer a better layout area at the cost of power dissipation compared with the approach made by Kshirsagar and Patrikar (2009).

CONCLUSION

The system reliability is more important in the applications like medical imaging, defense communications, computing sciences, etc. More specifically, the SRAM subsystems are important in which the information is stored and it can be read later. Improving the reliability of the SRAM cells would increase the reliability of the whole system. This study provides few novel techniques to enhance the fault-tolerant capability of the memory subsystems. Simulation results show that the proposed voting circuits offer less layout area compared with the existing voting mechanism. The power dissipation results are also analyzed in detail. These results are produced with the help of EDA tools such as DSCH and Microwind effectively. This study further can be extended to arithmetic and logic circuits such as CPU, signal processing circuits such as Digital Signal Processors (DSPs), etc.

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