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Low Power Digital Barrel Shifter Datapath Circuits Using Microwind Layout Editor with High Reliability

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ABSTRACT

Since the performance of portable electronic products increases continuously with demand, there is a need for low power digital VLSI design. Due to limited backup time of batteries, the operating time of portable electronic products is highly restricted. So, the designers now concentrate on low power rather than the speed of the device or system. We implement a 4 bit barrel shifter using different flavors like conventional CMOS logic, pass transistor logic and transmission gate logic styles. Electronic Computer Aided Design (CAD) tools like Microwind and a DSCH are used in our simulations by which the comparison of power in each style is provided. Microwind is used a layout editor and DSCH (Digital Schematic) is used as a schematic editor. Results show that the pass transistor logic consumes less power with minimum area and good performance. We used BSIM4 MOSFET model in 0.12 μm for experimental results. To improve the reliability of the circuits, fault tolerant voter circuits are implemented. The results are compared with the existing approaches and the proposed methods.

Key words: Barrel shifter, low power, voter circuits, reliability, transmission gates

INTRODUCTION

High power dissipation also leads to the reduced time of operation, higher weight due to batteries, reduced mobility, cooling cost and reduced reliability. Battery life time depends on the mean time between charging and system cost. Since the device temperature increases due to high density of transistors, the failure rate, cooling and packing costs are the reasons for the low power digital VLSI design. Also, it disturbs the environment in the form of heat, it becomes a major problem now-a-days (Yeap, 2008).

Because of higher weight batteries and lagging in battery technology, designers are forced to implement their designs with low power. To reduce the low power, both the dynamic and static power are being considered during the system operation. Techniques like by increasing the length of the transistors or reducing the width of the transistors in a circuit help to minimize the leakage power dissipation. Also, the methods like Multi-threshold mechanism, adaptive body biasing are used for minimizing leakage power. Like leakage power, the dynamic power can be reduced by reducing the switching capacitance, the operating supply voltage and clock frequency. By doing so, the life time of a device or system can be increased (Yeap, 2008).

Dynamic power and static power occupy most of the total power for a chip design. The power dissipated when the transistors are active, that is when signals are switching values, is known as

the dynamic power. But the static power dissipates across transistors even they are idle. We implement the barrel shifter as an example for reduction of power using different styles of CMOS logic (Weste *et al.*, 2012).

Triple Modular Redundancy (TMR) technology will protect the functionality of the FPGAs against the Single Event Upsets (SEUs) (Lala, 2008). Triple Modular Redundancy is the most common technique used to introduce fault tolerance in digital circuits. It simply involves redundancy in modules and determining the majority among those modules as the fault-free output. A voter circuit is generally employed to find this majority and carry it to the output. This technique is applicable if only the single fault is occurred. This majority function can be easily calculated with the help of the carry out of a single-bit full adder (Elamaram *et al.*, 2014).

To improve the reliability of the system voter circuits are incorporated with these 4 bit barrel shifter datapath circuits. The existing voter circuit is implemented and the results are compared with the proposed voter architecture (Peng *et al.*, 2012; Kshirsagar and Patrikar, 2009). The proposed voter circuit is made with only 2-1 multiplexers.

The sole objective of this study involves with the design of low power barrel shifters with improvement in reliability of the circuit. The subsequent sections convey the low power VLSI design architectures of the barrel shifter using conventional, pass transistor and transmission gate logic styles. A proposed voter circuit is implemented in each of the style and the results are compared with the existing approach.

MATERIALS AND METHODS

Barrel shifters: We implement a 4 bit barrel shifter which is a circuit will shift the 4 bit data to the right or left depends on the information applied to the control inputs. So, obviously this circuit demands the use of multiplexer (Khandekar and Subbaraman, 2008). A 4-1 multiplexer along with the appropriate connections are used to build a 4 bit barrel shifter. Barrel shifters are playing a crucial role in the microprocessor central processing unit while performing arithmetic, logic or circular mode of operations for a given task (Brown *et al.*, 2008; Wakerly, 2008).

Here, we use 4-1 multiplexer for the design of barrel shifter which is shown in Fig. 1. 4-1 multiplexer can be implemented using different CMOS logic styles and the best one will be identified by means of low power dissipation, less layout area and high performance. Conventional CMOS, pass transistor and transmission logics are used for the comparison. Since, conventional CMOS occupies more layout because of more number of transistors, the pass transistor logic would

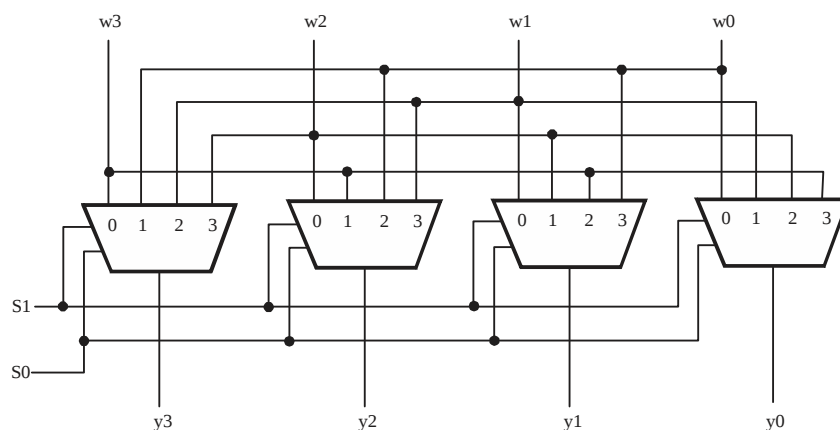


Fig. 1: A barrel shifter circuit

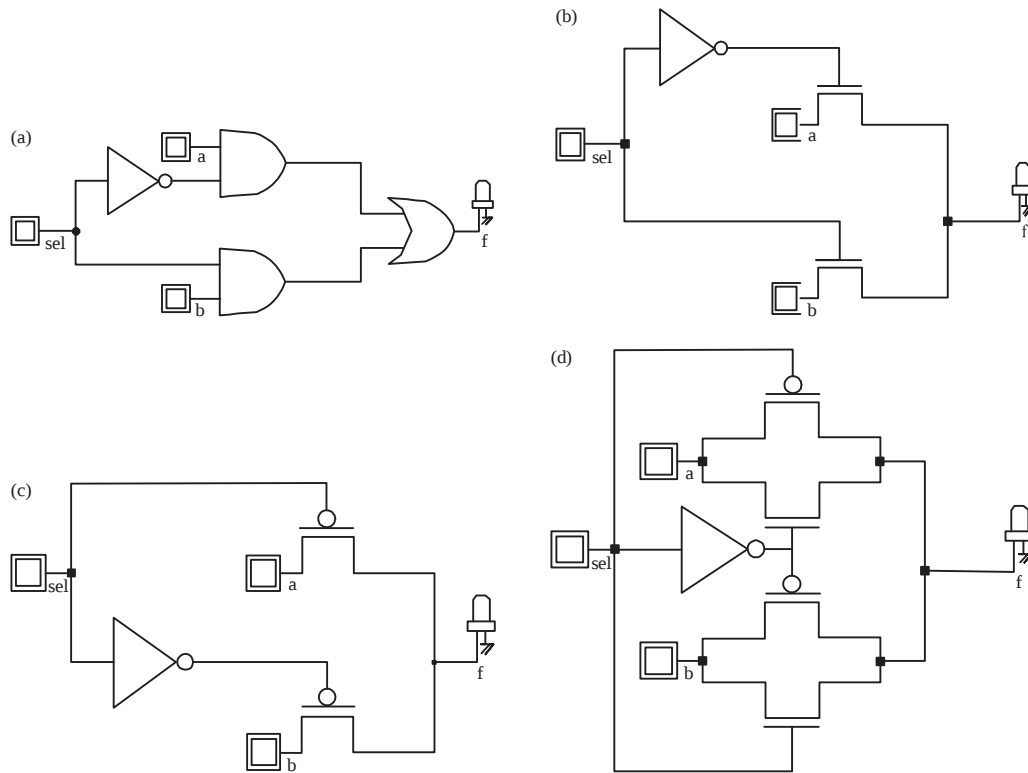


Fig. 2(a-d): Mux with (a) Conventional style, (b) nMOS logic, (c) pMOS logic and (d) Transmission gate logic

be more suitable as far as layout area wise concerned (Bardizbanyan *et al.*, 2010; Uyemura, 2006). Transmission logic would be more suitable to avoid threshold loss problems since this logic style has both nMOS and pMOS transistors.

Multiplexer designs: A 4-1 multiplexer is designed using two 2-1 multiplexer using conventional style, nMOS pass transistors, pMOS pass transistors and transmission gates (Pedroni, 2008). Figure 2a shows the 2-1 multiplexer using conventional style. The same multiplexer is designed with the help of nMOS transistors alone which is shown in Fig. 2b. A nMOS transistor is good for passing logic '0'. It suffers from threshold loss problem while it pass logic '1'. In Fig. 2b, if the select input is zero, the top transistor is ON and passes the data 'a'. If the select input is one, the bottom transistor is ON and passes the data 'b'. Similarly, a 2-1 multiplexer is designed using pMOS logic and transmission gate logic which are shown in Fig. 2c and d.

Barrel shifter schematics/layouts: For the design of 4-bit Barrel Shifter, we use Microwind/DSCH EDA tools to produce layout and power analysis results. The power of such tools are explored and the results and comparative analysis report is produced (Govindarajulu *et al.*, 2010).

Barrel shifter-conventional approach: Schematic diagram and timing diagram results of a 4 bit barrel shifter using conventional 2-1 multiplexer are produced in Fig. 3 and 4, respectively. Functional verification of the circuit is done using DSCH tool (Elamaram *et al.*, 2012; Subramani *et al.*, 2014).

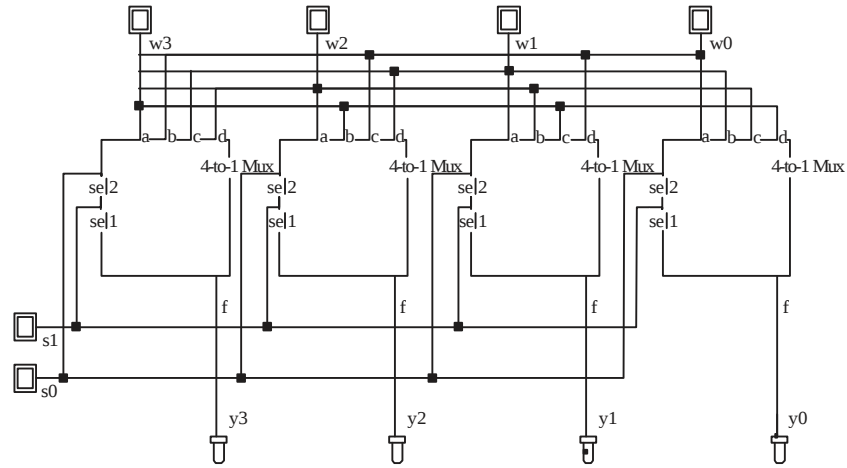


Fig. 3: 4 bit Barrel shifter

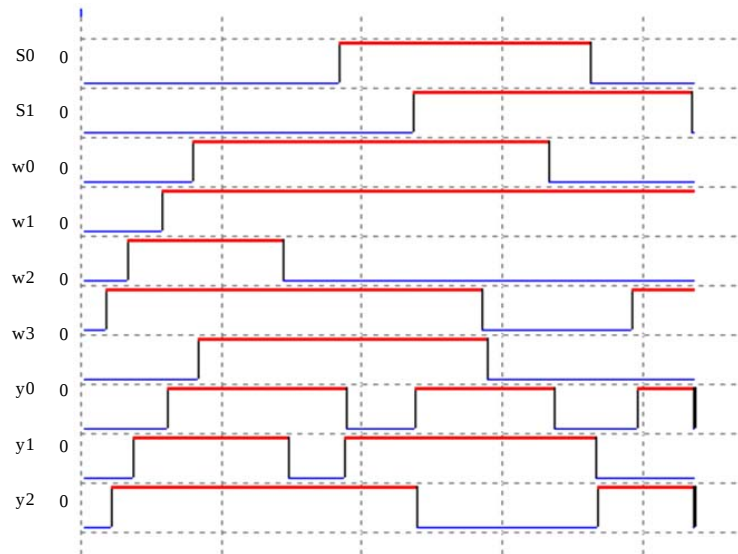


Fig. 4: Simulation results (conventional)

Figure 5a shows the layout diagram using Microwind tool and much useful for the analysis of power, propagation delay and area. A functional verification can be done also on the layout presented here and can be verified with previous DSCH results. Also the number of transistors both pMOS and nMOS involved in the design can be obtained (Elamaram *et al.*, 2012; Elamaram and Upadhyay, 2013).

Barrel shifter-pass transistor logic: We implement a 4 bit barrel shifter using multiplexer which is designed by nMOS pass transistor. A very less number of transistors involved in the design is the main advantage compared to other logic styles and in turn the layout size is much reduced which is shown in Fig. 5b. Pass transistor logics are much popular where the device density is high with small size like memory circuits (Priya *et al.*, 2012; Vigneswaran *et al.*, 2006).

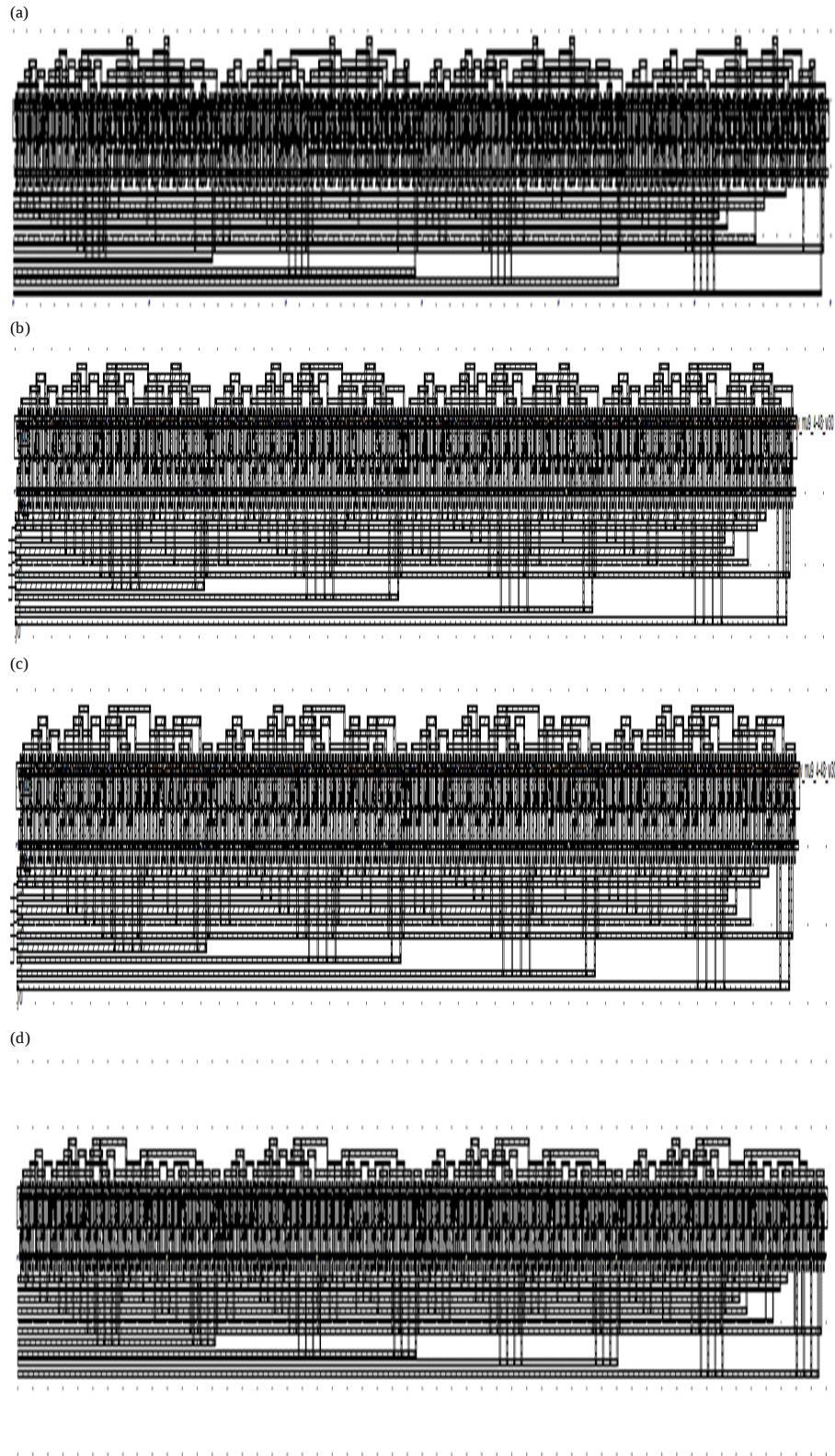


Fig. 5(a-d): Layout using (a) Conventional approach, (b) nMOS pass transistor style, (c) pMOS pass transistor style and (d) TG logic approach

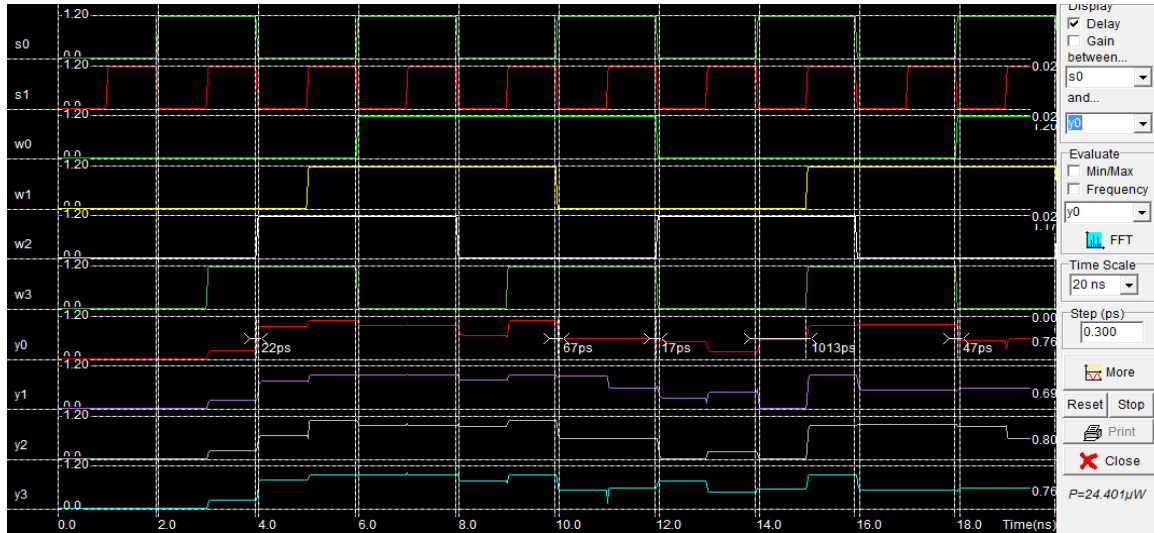


Fig. 6: Timing diagram result of TG logic style

An implementation of the same using pMOS pass transistor style is done and the layout is produced as in Fig. 5c. Generally, pMOS transistors are much slower than nMOS. Hence, this kind of implementation is rarely used.

Barrel shifter-TG logic: Threshold loss problem is a major drawback of pass transistor logic in circuits. This occurs due to the characteristics of pMOS and nMOS transistors. A ground or zero potential charge is transferred without loss by nMOS transistor. But for the supply, loss is occurred with threshold voltage of the transistor. Similarly, Vdd is transferred without loss by pMOS transistor. But loss occurs when the zero potential charge is transferred with the threshold voltage of a transistor. Here we implement Transmission Gate (TG) logic for this barrel shifter design to overcome the drawback of pass transistor (Elamaram *et al.*, 2014) and the layout is shown in Fig. 5d. Input signals can be applied on the layout and the functionality is verified with the timing diagram result which is obtained in Fig. 6. To verify the functionality, using DSCH tool timing diagram can be obtained for the given schematic design by applying the inputs appropriately. Similarly, functional verification can be done using Microwind tool with the help of the generated layout for the given circuit design (Rajesh *et al.*, 2014). For the sake of simplicity, only one such layout simulation for 4 bit barrel shifter using conventional CMOS style is made as in Fig. 6.

Existing fault tolerance using TMR: Triple-Modular Redundancy (TMR) is a very commonly used form of fault tolerance technique implemented in digital systems. The main idea of TMR is that a digital circuit can be made tolerant to faults by using three independent copies of the same module and giving all the outputs to the voter which performs a majority vote on the output of all three circuits (Peng *et al.*, 2012). The voter outputs the logic value that belongs to at least two of its inputs. If the inputs of the voter are taken as A, B and C_i and the output as C_{i+1} , respectively, then C_{i+1} is a Boolean variable whose value is calculated as in the equation below (Elamaram *et al.*, 2014):

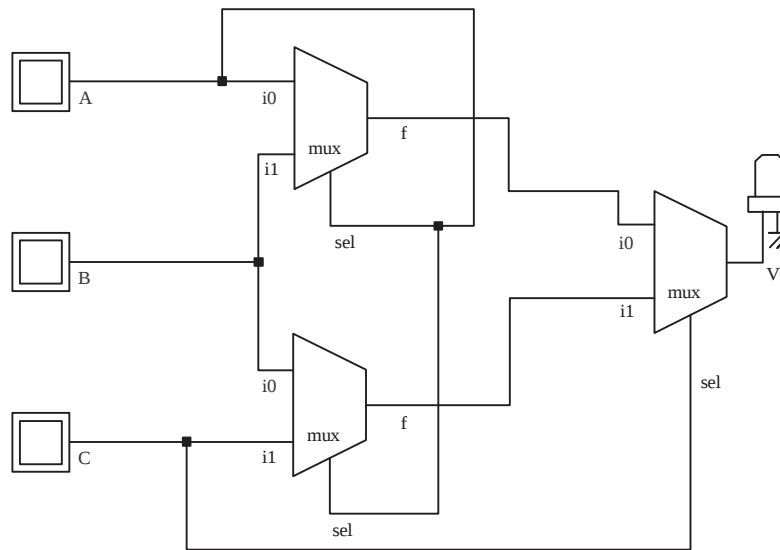


Fig. 7: Proposed voter circuit using 2-1 multiplexers

$$C_{i+1} = (A \oplus B) C_i + AB \quad (1)$$

This majority function can also be calculated as using the concept of Carry Look Adder (CLA) concept. Here the term “Generate” is used as the logical and operation of the data “A” and “B”. If $A = 1$ and $B = 1$, then the majority function output (C_{i+1}) becomes 1, otherwise 0. An another term “Propagate” is used as the logical Ex-OR operation the data “A” and “B”. If “A” is not equal to “B”, then this propagate term becomes 1. If $C_i = 1$, then the majority function output becomes 1 otherwise 0.

Assuming that all the redundant digital circuits used are identical, the reliability of the system using TMR can be assumed to be a function of the reliability of one circuit, assuming the voter circuit gives the correct output. This system will be error free even if only two of the three modules are operational.

Assuming that all the redundant digital circuits used are identical, the reliability of the system using TMR can be assumed to be a function of the reliability of one circuit, assuming the voter circuit gives the correct output. This system will be error free even if only two of the three modules are operational. The reliability term is defined as the probability of all modules giving the correct output plus the probability of any two modules obtain the correct output.

Proposed voter circuit design: The voter circuit is implemented using logic gates and multiplexers to produce a fault free output even in the presence of a faulty circuit. This results in fault tolerance for all types of stuck at faults (Peng *et al.*, 2012). The voter circuit presented here is expected to have a higher reliability and fault tolerant capabilities as opposed to a voter circuit used in the TMR systems in general. The proposed voter circuit is shown in Fig. 7. Figure 8 shows that the barrel shifter with a proposed voter circuit.

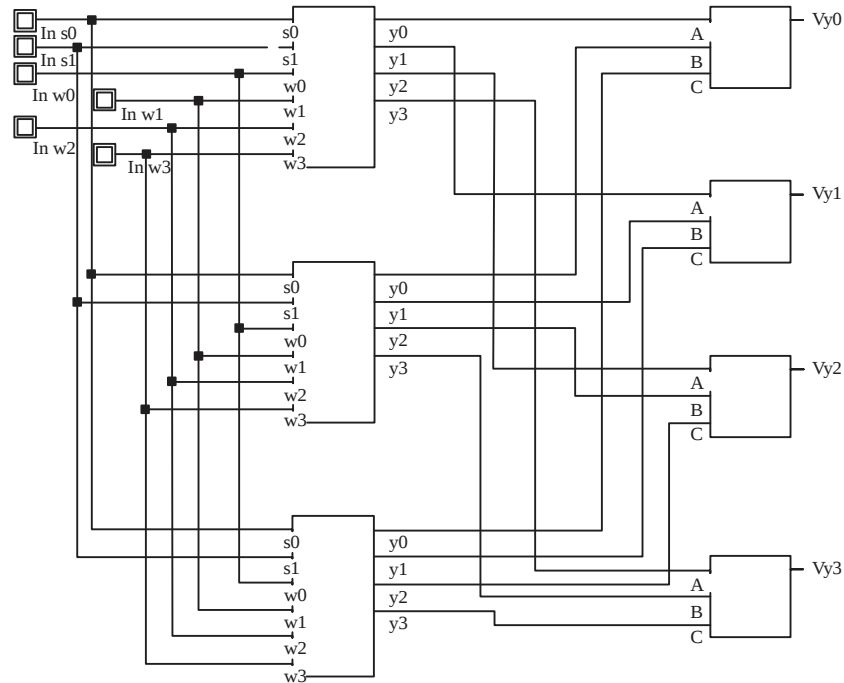


Fig. 8: Barrel shifter with a proposed voter circuit

RESULTS

The above timing result is produced for all kind of logic styles presented here and the output of the design is verified in each case. Since the speed, power and area are important in semiconductor circuit designs, the results are compared and tabulated with the help of Microwind tool. The importance of DSCH tool is the capability to convert the schematic designs in to Hardware Description Language (HDL) codes. Here the generated Verilog HDL code is compiled to produce a layout using Microwind tool. This is much useful for larger designs.

Average power dissipation results are obtained over the interval 20 nsec with all logic style approaches. Since less number of transistors are involved in the pass transistor logic, not only the area is reduced also the power. If the design has more number of transistors, the dissipated power will be huge. Simulation results show that nMOS pass transistor logic approach is much better than other styles with 6.533 μ W.

Table 1 provide the results of number of transistors involved in each design and layout area in micro square meter. Microwind tool provides the information about the number of nMOS devices, pMOS devices, electrical nodes involved in the circuit. Table 1 shows the electrical properties of the corresponding design style. Simulation is made using CMOS 0.12 μ m 6 Metal process at 27°C temperature. Table 2 shows that the power dissipated in each design style with average delay. Also the power delay product is obtained from these results. The lower the Power Delay Product (PDP), the result is better in the circuit. Results show that the nMOS pass transistor logic provide a better result in terms of layout area and power dissipation with lowest PDP as 3.08e-15.

With the help of Microwind EDA tool, all the results are verified with BSIM4 MOOSFET model in 0.12 μ m technology. We had a good exposure with working different designs involved here using Microwind ECAD tool. More accurate and detailed analysis report and comparison charts can be produced by using industry standard tools like Cadence, Synopsys, Mentor Graphics, etc.

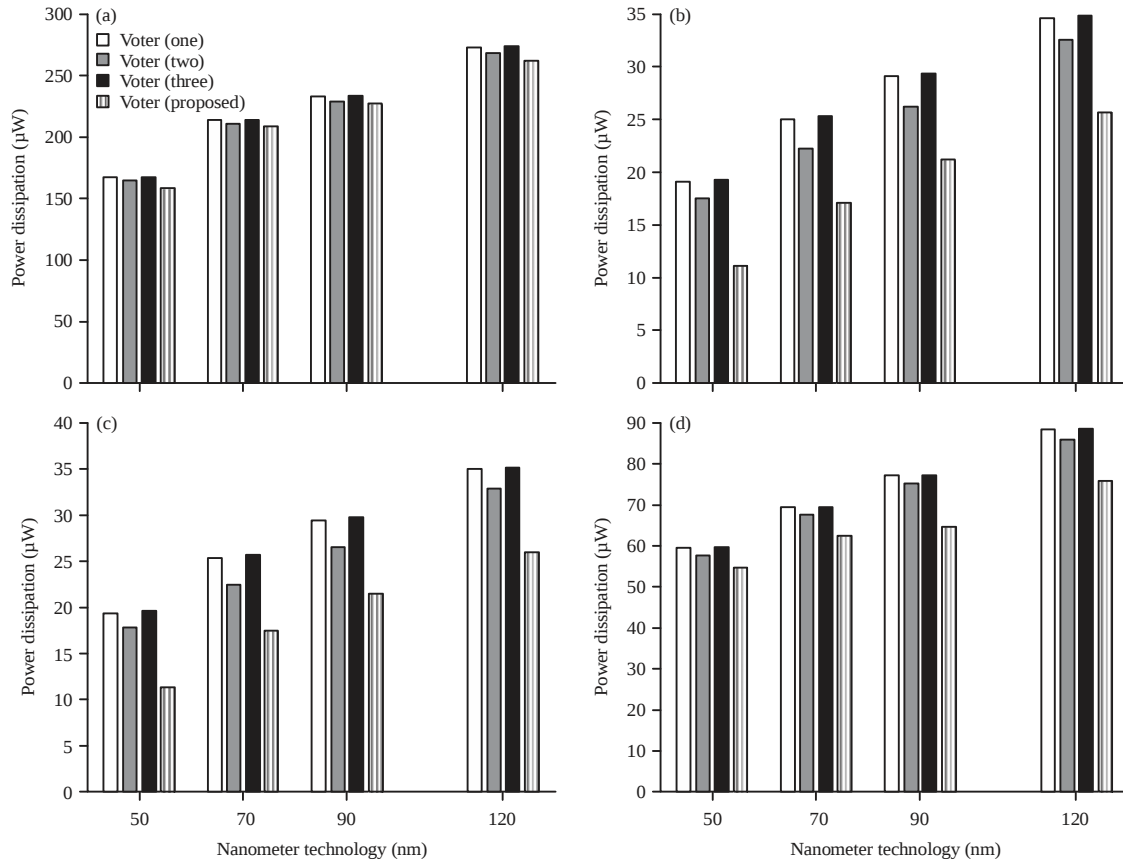


Fig. 9(a-d): Barrel shifter using conventional (a) CMOS logic, (b) nMOS logic, (c) pMOS logic and (d) TG logic

Table 1: Number of transistors and layout area

Design	No. of NMOS transistors	No. of PMOS transistors	Layout area (μm^2)
Conventional CMOS	156	156	2026.3
nMOS pass transistor logic	72	48	1380.2
pMOS pass transistor logic	48	72	1380.2
TG logic	72	72	1753.5

Table 2: Average power dissipation

Design	Average power (μW)	Delay (nsec)	Power delay product (J)
Conventional CMOS	86.40	1.136	9.82e-14
nMOS pass transistor logic	6.553	0.47	3.08e-15
pMOS pass transistor logic	6.815	0.66	4.5e-15
TG logic	24.401	0.756	1.85e-11

Dynamic power dissipation can be analyzed also during the period of 10, 20 and 30 nsec etc. Also the foundry selection can be made with 180, 120, 90 and 60 nm etc., with the help of the tool libraries. Here all the implementations are done with $0.12 \mu\text{m}$ by not violating any layout design rules.

To improve the reliability of the barrel shifter datapath circuits, the voting mechanisms are implemented with the concept of Triple Modular Redundancy (TMR). Figure 9a depicts the power dissipation comparison results among the existing voter and proposed voter with the barrel shifter

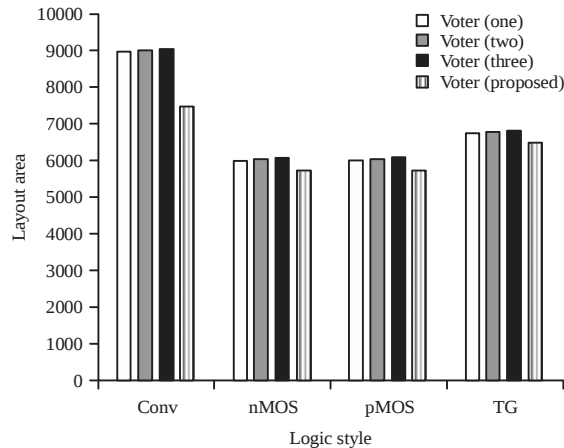


Fig. 10: Layout area comparison results with barrel shifter

systems. It is apparent that the proposed voter circuit produces a low power dissipation compared with the existing voter (one) (Peng *et al.*, 2012). For example, the proposed voting approach obtain $262.82 \mu\text{W}$ and the existing voter (one) produce $274.2 \mu\text{W}$ for a 4 bit barrel shifter. It indicates also that the existing voter (two) which is based on the majority function voting, i.e., $V = AB + BC + BA$ obtain $270.12 \mu\text{W}$. An another existing fault-tolerant voter (three) circuit (Kshirsagar and Patrikar, 2009) produce $275.2 \mu\text{W}$. Figure 9b conveys that the proposed voter circuit obtain $25.74 \mu\text{W}$ and the existing voter (one) produce $34.659 \mu\text{W}$. The voter (two) and the voter (three) circuits are producing 32.6427 and $34.87 \mu\text{W}$ for the barrel shifter with nMOS logic style. Similarly, in Fig. 9c and d interpret the power dissipation comparison results of a barrel shifter using pMOS and TG logic with existing and proposed voter circuits, respectively.

The layout area results of the barrel shifter using conventional CMOS logic, nMOS logic, pMOS logic and TG logic are compared and displayed in Fig. 10. For example, the barrel shifter using conventional logic with a conventional voter (one) occupies a layout area of $9002 \mu\text{m}^2$ and with a proposed voter occupies a layout area of $7510 \mu\text{m}^2$. The voter (two) and the voter (three) circuits occupies layout area as 9060 and $9090 \mu\text{m}^2$, respectively. It is apparent that the nMOS and pMOS logic styles offer a very low layout area as 6010 and $5755 \mu\text{m}^2$ for conventional voter and proposed voters, respectively. For the sake of simplicity, these layout area calculations are evaluated only with the $0.12 \mu\text{m}$ default rule library with the Microwind tool.

DISCUSSION

This study dealt with a barrel shifter datapath circuits with improved reliability along with low power designs. The reliability of a system is more important nowadays especially for the applications like space technology, medical electronics and defense communications (Lala, 2008). The proposed barrel shifter implemented here is made using nMOS, pMOS and TG logic style approaches (Elamaram *et al.*, 2012; Khandekar and Subbaraman, 2008). The DSCH schematic editor and Microwind layout editor tools are used for the complete analysis of this study (Elamaram *et al.*, 2014; Rajesh *et al.*, 2014; Elamaram and Upadhyay, 2013). The proposed voting circuit presented here provide less power dissipation than the existing voter (Peng *et al.*, 2012). The conventional majority function, $AB + BC + CA$ and the voter (Kshirsagar and Patrikar, 2009) offers more power dissipation than the proposed barrel shifter in all the nMOS, pMOS and TG logic

styles. The layout area results also indicate that the proposed voting circuit offer a better result compared with all the three existing approaches. This study can be further extended to other logic styles like pseudo nMOS, dynamic CMOS and domino CMOS logic styles too for further improvement in performance, layout area and power dissipation.

CONCLUSION

Designers and engineers are still working towards low power circuit designs which help a lot to the consumer electronics market. People tend to move towards the product which save more power rather than speed and additional features. A good knowledge on designing low power circuits help a lot for this kind of study. The three important VLSI optimization goals are speed, area and power. Here we focus more on area and power. More specifically dynamic power is calculated and analyzed. By modifying the length and width of the transistors used in the circuit, further a leakage power will be reduced. Also techniques like multi-threshold, adaptive body biasing can be used to minimize the leakage power too. To improve the battery back up time, designers should think about dynamic power reduction methods while the system in the active mode and static power reduction methods while the system in the sleep mode.

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