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Review Article
Designing Ultra Low Voltage Low Power Active Analog Blocks for Filter Applications Utilizing the Body Terminal of MOSFET: A Review

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Abstract
The propelling demand for ultra-low voltage low power electronics has provided the much needed impetus to the research and design of analog building blocks working below 1 V supply. Numerous techniques are being adopted by the researchers to achieve ultra-low voltage low power operation and each vying to become the universal design choice. This study presents a survey of the two techniques namely the bulk driven technique and dynamic threshold technique that utilize the body terminal of the MOSFET to achieve the aforementioned objectives. A brief review of the principles of the two techniques, including a technical analysis of their applicability and limitations is presented. An inspection of extensively researched analogue active building blocks the operational transconductance amplifier and current conveyor designed using the body techniques is done. Various performance parameters like the supply voltage requirement, power dissipation, frequency response and dynamic range are discussed. The spectrum of applications that can be realised by these active blocks are also highlighted. In this study, operational transconductance amplifier and current conveyor active blocks will be designed utilizing the body techniques for tunable filter applications. The designed blocks are expected to work in between 0.4-0.8 V power supply dissipating 10 nW to 100 μW of power. The expected frequency response is in the range of 100-500 kHz for low frequency applications and frequency response in the range of 4-200 MHz for high frequency applications. The designed blocks will be suitable for integration with biomedical devices and communication systems.

Key words: Bulk driven, dynamic threshold, current conveyor, operational transconductance amplifier, ultra-low voltage low power, current mode

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INTRODUCTION

The proliferation of portable devices, implantable biomedical systems, development of energy harvesting systems for self-powered wireless sensor nodes and the recent internet of things (IOT) in the last few decades[1-8] has seen the shift of focus in the study and development of analog integrated circuits. As with more and more battery operated portable devices like mobile phones, tablets, blood pressure monitors and wearable ECG machines, etc., becoming ubiquitous power dissipation is posing a serious issue. Moreover, packing density, high speed and wafer area limitations are other challenges faced by the engineers. The cumulative effect of the mentioned factors have resulted in rapid shrink in size of the semiconductor devices to achieve ultra-high scale integration which has led to scaling down of the power supply rails to curb power dissipation and achieve performance optimization[2,4,9,10]. This trend proved advantageous for the digital designs but it posed new challenges to the analog industry. The threshold voltage becoming a substantial fraction of the total supply voltage is the main hindrance when it comes to analog design since the threshold voltage cannot be scaled in the same ratio as the supply to keep leakage within acceptable limits. This has led to severe performance degradation in analog circuits and so the designing of analog circuits working in Ultra Low Voltage Low Power (ULVLP) regime has become the area of active research. Designing the devices capable to perform well under low supply constraints is a tedious task but the researchers have adopted distinct approaches to mitigate the problem. The low voltage design approaches as adopted by many researchers can be categorised in to four distinct groups. Circuit level design, device (transistor) level, technology level and operation level. The first technique aims at altering the design at the circuit level with novel implementations using standard primitives (gate driven MOSFETS). This approach caters to a specific targeted application area for Low Voltage (LV) implementation. It includes adopting numerous circuit level techniques to achieve high performance like level shifting[11], self cascode[11], subthreshold operation[11] and composite transistor[11]. Second, includes slightly modifying the standard MOS transistor to alter the way input and output signals are coupled to the circuit like floating gate MOS (FG-MOST)[11-13], bulk driven MOS (BD-MOST)[13-16] and dynamic threshold MOS (DTMOS)[17,18] techniques. These techniques are application independent and remove the threshold voltage restriction. Third, involves adopting latest technologies like silicon on insulator (SOI), partially depleted SOI and Bi-CMOS. The last approach emphasizes in which domain the information is processed in the circuit current mode or voltage mode. The current mode approach is the best suited for Low Voltage (LV) operation as it is reported to be more immune to noise, less sensitive to supply voltage, have low electrostatic discharge, low propagation delay, high slew rate etc.[1-4]. Among various current mode devices operational amplifiers (OTA)[9] and Current Conveyors (CC)[2,3,10] are the most functional devices by virtue of their versatile features.

This study discusses the body techniques which can be categorised into two approaches. First, bulk driven approach in which the input signals are applied at the body rather than the gate terminal[14-16,19]. Second, dynamic threshold approach in which the body terminal is tied to the gate or a node in the circuit that causes its threshold voltage to vary dynamically[17,18,20].

REVIEW OF MOSFET BODY TECHNIQUES

Bulk driven technique for MOSFET: In most of the applications Metal Oxide Semiconductor Field Effect Transistor (MOSFET) was regarded as a three terminal device the body being shorted to the source or tied to the most negative or positive supply. The constraint of ULVLP put forward by the recent demand made engineers to revisit the conventional MOSFET for the solution and it was found that MOSFET is essentially a four terminal device and the body can be utilized to provide ULVLP operation. The idea is not new[15] it dates way back to 1987. The bulk technique involves using the body terminal as the input port and the gate terminal is tied to a voltage suitable enough to create the conducting channel[14,15,21]. This removes or lowers the threshold voltage limitation from route of the signal contrary to the conventional MOSFET and facilitates ULVLP operation and increase the input common mode dynamic range. The technique is demonstrated in Fig. 1. The standard CMOS fabrication technology utilizes n-well or p-well process for realizing NMOSFET and PMOSFET. This limits the type (polarity) of BD-MOSFET as bulk must be kept isolated residing in its own well rather than in the common substrate, due to this N type BD-MOSFET is available in P-well process and vice versa[16]. The cross section of a P type BD-MOSFET is presented in Fig. 2.

The operation of a bulk-driven device can be explained as follows. When a constant bias voltage enough to establish a channel between drain and source is applied at the gate terminal and the input signal is applied to the bulk, the bulk terminal affects the depletion region and hence the drain current. The bulk of BD-MOSFET serves the same purpose as the gate in JFET so BD-MOSFET can be regarded as the depletion type JFET[15,16,21]. The variation of I_D is due to the variation in V_{th} with the V_{SB} according to the relation given as in Eq. 1:

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\Phi_F| + V_{SB}} - \sqrt{2|\Phi_F|}\right) \quad (1)$$

where, Φ_F is the fermi potential, γ the body effect coefficient and V_{T0} the threshold voltage at (V_{SB} = 0). Hence, the drain current is manipulated by varying V_T through V_{SB} instead of V_{GS}. It is of prime importance to use the range of voltages low enough not to activate the bipolar parasitic transistors QP and QV resulting in latch up[15,16]. The bulk driven technique is compatible with the bulk CMOS technology and at the expense of increased cost twin well or triple well technology

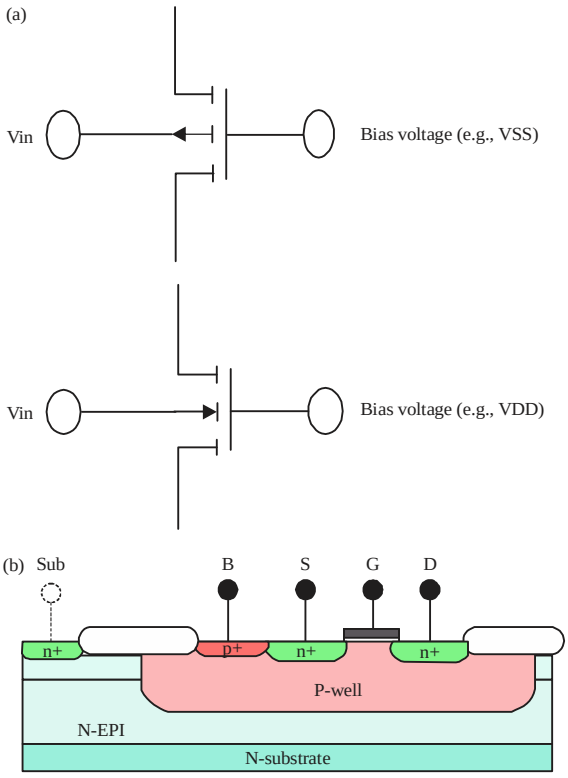

Fig. 1(a-b): Bulk driven MOSFET (a) Symbol and (b) Cross-sectional view

can be opted to get both BD-PMOST and BD-NMOST in the same circuit. The transconductance of BD-MOST is substantially lower than that of the GD-MOST[15,19,21]. The ratio of body transconductance g_{mb} to the gate transconductance g_m given by Eq. 2:

$$\eta = \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt{2|\Phi_F| + V_{SB}}} \quad (2)$$

where, the range[19] of η is 0.2-0.4. This limits the cut off frequency of BD-MOS. The relation between the BD-MOST and GD-MOST bandwidths is given by Eq. 3:

$$f_{Tbulk-driven} = \frac{\eta}{3.8} f_{Tgate-driven} \quad (3)$$

The small transconductance and low operating frequency coupled with ULVLP operating capability makes the BD techniques a formidable contender for bio medical and speech processing systems which operate in kHz range[22,23]. Moreover, the frequency range can be increased by boosting the transconductance[24].

The following are the advantages of the bulk driven technique:

- Extended dynamic range in ULVLP conditions[15,16,19]
- BD-MOST is capable of working in negative, zero or slightly positive bias voltages. This enhances the common mode input voltage range and enables rail to rail voltage swing with careful design that is unachievable in conventional design at LV operation[16,24]
- The V_T requirement is completely negated leading to increased voltage swing and low supply voltage requirement of the order slightly greater then threshold voltage[14-16]
- The behaviour can be modelled and studied using the conventional MOS models[13]

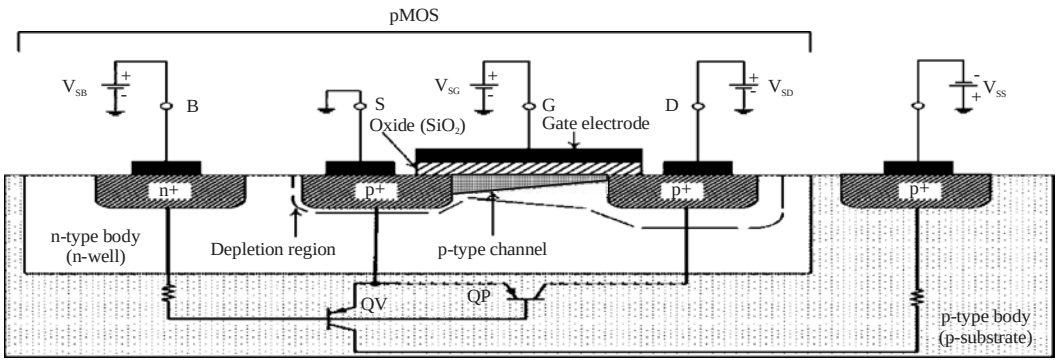

Fig. 2: Cross-sectional view of BD-PMOST in n-well CMOS technology

The shortcomings of the bulk driven technique are as follows:

- The body transconductance g_{mb} of BD-MOST is typically 3-5 times less than that of conventional GD-MOST resulting in reduced gain and cut-off frequency and increased input referred noise[14-15]
- The polarity of the BD-MOST is process related. For P-well process, only N-channel BD-MOST are available and for N-well process, only P-channel BD-MOST are available[16]
- For achieving proper isolation of the bulk terminals each BD-MOST resides within its own well this approach of differential well for BD-MOSTs results in matching problem leading to frequency degradation[16]
- Latch up is also a concern[15]
- The input impedance of the BD-MOST is low in comparison to GD-MOST[16]

Dynamic threshold technique for MOSFET: To empower electronics circuits with the ability to work sub 0.5 V researchers are coming up with new innovations. In the same sequence[17] in his revolutionary study in 1944 proposed dynamic threshold metal oxide field effect transistor (DTMOS) based on MOS silicon on insulator (SOI) process technology. The study presented the underlining principle of DTMOS in great detail, the concept is to tie the gate and body of the transistor together there by modulating the threshold voltage of the MOS as per the input voltage as is conferred from Eq. 4-6:

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\Phi_F| + V_{SB}} - \sqrt{2|\Phi_F|}\right) \quad (4)$$

$$V_{T0} = V_{FB} + \Phi_O + \gamma\sqrt{\Phi_O} \quad (5)$$

$$\gamma = \sqrt{\frac{2q\varepsilon_{si}N_A}{C_{ox}}} \quad (6)$$

where, γ is the body effect coefficient, V_{T0} threshold voltage for ($V_{SB} = 0$), V_{FB} is the flat band voltage, Φ_0 is the total surface band bending, N_A is the substrate doping, ε_{si} is dielectric permittivity of silicon and Cox is the oxide capacitance per unit area.

More accurate approximation of Φ_0 can be made using Eq. 7:

$$\varphi_0 = 2\Phi_F + \alpha\Phi_t \quad (7)$$

where, α is an experimental fitting parameter and Φ_t is the thermal voltage[22,25,26]. The DTMOS can be fabricated using bulk CMOS process technology with acceptable performance,

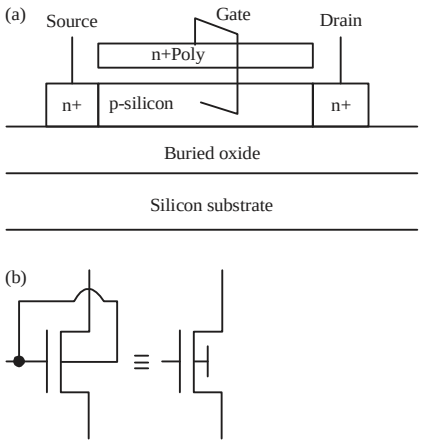

Fig. 3(a-b): (a) Cross sectional view of DTMOS[17] and (b) Symbol

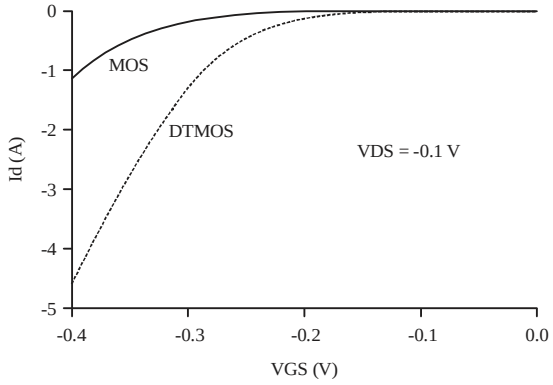

Fig. 4: Drain currents variation of DTMOS and conventional MOS[20]

twin well, triple well and SOI technology yields high performance DTMOS transistors. Figure 3 shows the symbol and cross sectional view of DTMOS in SOI process. The DTMOS suffers from latch-up issue if operated at higher supply voltage. This problem can be avoided if it is operated in the range of (0.4~0.5 V) as discussed by Assaderaghi *et al.*[17] and Uygur[20]. The higher supply voltage can be used by adopting innovative techniques[27] requiring additional transistors hence, a compromise between chip area and frequency response has to be made.

The DTMOS transistor exhibits elevated transconductance than a conventional MOSFET and bulk driven MOSFET. The reasons being the threshold voltage reduction and the reduction of the channel vertical electrical field improving the mobility of the charge carriers there by leading to higher current drive[18]. Figure 4 presents a comparison between the drain current variation of DTMOS and conventional MOST with the gate to source voltage being swept from (-0.4 to 0 V) at a constant drain to source voltage[20]. This behaviour make

DTMOS a good candidate for ultra-low voltage applications providing higher current drive. The subthreshold regime of operation is the choice for circuits developed to enable ultra-low voltage operation. The current and voltage in the subthreshold region are exponentially related as the current transfer is mainly due to the diffusion of carriers. The V-I equation and the transconductance of DTMOS transistor is given in Eq. 8 and 9. The transconductance is identical to that of the BJT being proportional to the current[28]. Furthermore, it is theoretically proved using approximations[25,29] that the DTMOS shows better subthreshold swing than the conventional MOST. The assumptions are validated experimentally by Lee *et al.*[30] for long channel DTMOSTs having lengths of channel exceeding 0.4 μm exhibiting near ideal subthreshold swing of 60 mV/dec. This makes DTMOS the first choice for ULVLP design:

$$I_D = \frac{W}{L} I_{DO} e^{qV_{GS}/nKT} \quad (8)$$

$$g_m = \frac{q}{nKT} I_D \quad (9)$$

In the design of analog circuits, correct modelling of semiconductor devices plays a crucially important role for the accuracy of simulations. Before starting with the design we need to ascertain that existing MOSFET models like BSIM, EKV are capable of modelling the performance and operation of DTMOS in spice simulators. The widely employed BSIM and EKV models assume total depletion approximation i.e., complete absence of mobile carriers in the channel. However, this assumption does not apply to DTMOS transistor but the existing models can still be applied with good accuracy as validated experimentally by Tsividis[25], Jimenez-P *et al.*[29] and Jimenez-P and De la Hidalga-W[31] given the condition that the body voltage remain in between (0.4~0.5 V) with channel length not very small.

The merits of DTMOS technique are listed:

- Extended dynamic range in ULVLP conditions[17]
- DTMOS exhibits higher current drive and transconductance than conventional MOST in ULVLP[18,18]
- The threshold voltage changes dynamically leading to extend input range and low power dissipation[20]
- The DTMOS exhibits near ideal subthreshold slope leading to linear circuit design under subthreshold regime[17]

The limitations of the technique are listed:

- The polarity of the DT-MOST is process related. For P-well process, only N-channel BD-MOST are available and for N-well process, only P-channel BD-MOST are available[16]
- Leakage currents originating from lateral bipolar transistors if operated at higher supply is an issue[20]

REVIEW OF ANALOG BUILDING BLOCKS

As this study is focused on the design of the universal Analog Building Blocks (ABB) the Current Conveyor (CC) and Operational Transconductance Amplifier (OTA), the subsequent section discusses the state of the art recently proposed CCs, OTAs and their variants to emphasize the importance of the body techniques.

The 1 V bulk driven CMOS fully differential second generation current conveyor[32] was proposed. The circuit utilised bulk driven high gain Fully Differential Difference Amplifier (FDDA) and bulk driven transconductor in feed forward mode to achieve increased differential mode gain in FDDA and suppressed common mode input signals. The circuit achieved excellent linearity along with (-3 dB) bandwidths of 30 MHz for (I_Z/I_X) and 25.7 MHz for (V_X/V_Z), while working below 1 V. The complete circuit and the corresponding equations are shown in Fig. 5. In[19] BD-CCII designed in 0.18 μm TSMC technology operating at 0.5 V is proposed. The circuit consisted of bulk driven differential pair based on bulk driven flipped voltage follower for voltage following action between Y and X terminals and bulk driven MOS cascode topology for facilitating the current transfer between nodes X and Z together with increasing the input impedance at the output. The circuit exhibited good performance with a power dissipation of only 4.7 μW. To validate the design BD-CCII was configured for inductance simulation achieving 88.2 degree phase difference between voltage and current. The circuit schematics is shown in Fig. 6. A BD-CCII based on bulk driven folded cascode OTA in unity feedback configuration was implemented in 0.18 μm CMOS technology[22]. The OTA was realised using bulk driven NMOS differential pair while cascode current mirrors were used for differential to single ended conversion. The circuit as shown in Fig. 7 exhibited (-3 dB) bandwidths of 13 MHz for (I_Z/I_X) and 14 MHz for (V_X/V_Z) with a current and voltage gain of unity. The input DC voltage and current range were ±380 mV and ±7 μA, respectively. The power dissipation was at 64 μW at ±0.4 V supply voltage. To confirm the design researcher presented a current mode multi-function filter capable of realising all pass, low pass, high pass, notch and band pass responses simultaneously. Moreover, the quality factor and pole frequency of the filter was independently tunable.

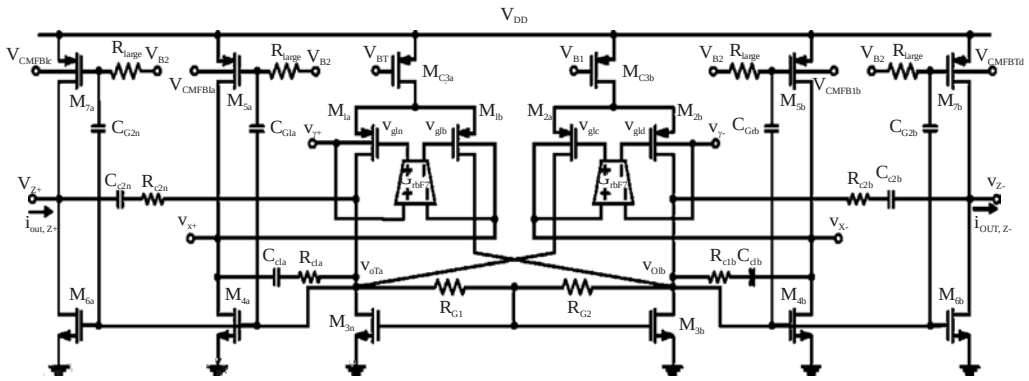

Fig. 5: CMOS implementation of bulk driven FDCCII[32]

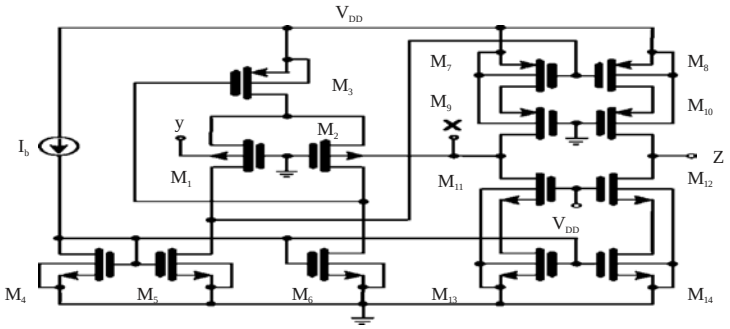

Fig. 6: CMOS implementation of bulk driven CCII[19]

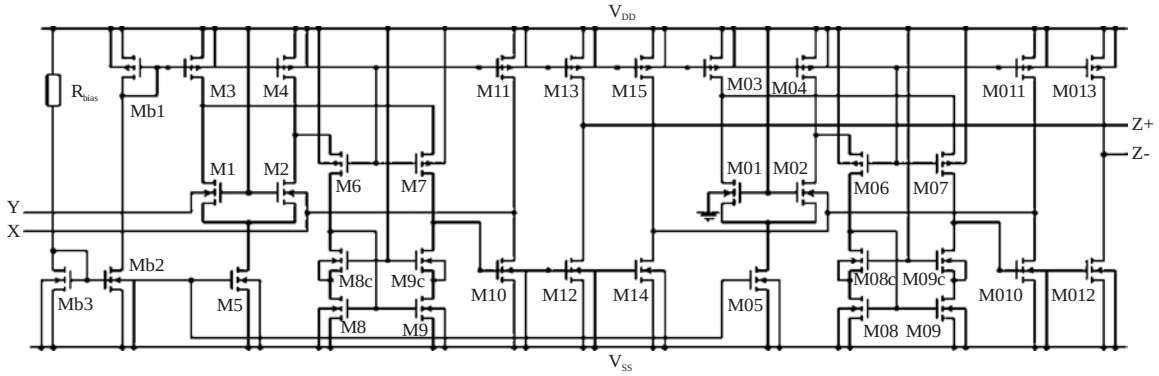

Fig. 7: CMOS implementation of BD-CCII using folded cascode OTA[22]

Recently Dabbous and Alsibai[33] presented ultra-low voltage low power Z copy current controlled current differencing buffered amplifier (ZC-CC-CDBA) utilizing the bulk driven technique. The realization included the two current followers constructed using the Bulk Driven Flipped Voltage Follower (BDFVF) and bulk driven current mirrors. The current followers provided the difference of the two input currents (I_n-I_p) (which is made available at Zc terminal and the buffered amplifier realised by the bulk driven differential pair utilizing (BDFVF) adopted for low voltage operation provided $V_w = V_z$. Another evident advantage was the presence of current controllable parasitic resistance which makes it a good choice for filter realization without using passive components. The circuit realised in 0.18 μm TSMC technology provided unit current and voltage gain and (-3 dB) bandwidth of 11.18 MHz for (V_W/V_Z) and 5.15 MHz and 2.4 MHz for ($I_{Z,ZC}/I_n$) and ($I_{Z,ZC}/I_p$), respectively. Furthermore, the reported current and voltage offset was less than 50 nA and 1 mV. The circuit description is depicted in Fig. 8. Raikos *et al.*[34] used PMOS Bulk driven differential pair with current mirrors as active loads together

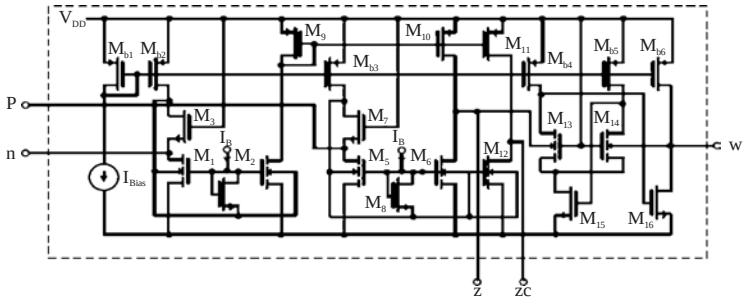

Fig. 8: CMOS implementation of bulk driven ZC-CC-CDBA[33]

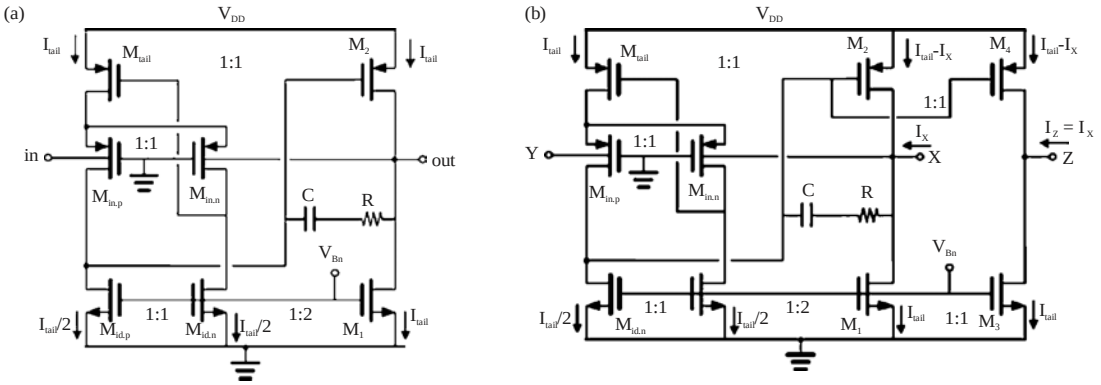

Fig. 9(a-b): CMOS implementation of bulk drivenbuilding blocks[34]

with the Flipped Voltage Follower (FVF) to form an input stage capable of working at extremely low voltage. The innovative use of FVF to bias the differential pair is such that the flipped voltage follower modified the gate voltage of tail transistor M_{tail} as shown in Fig. 9 that guaranteed equal tail current for input devices. The FVF also relaxed the minimum supply requirements and enabled the circuit to work at 0.5 V. The circuit exhibited the rail to rail input common mode range thanks to the bulk driven technique. The input stage was then used to synthesize the CCII circuit working at 0.5 V. The developed input stage was used in designing a voltage follower utilizing the two stage miller amplifier topology. The designed voltage follower is further employed in designing the current conveyor. The excellent circuit worked under low voltage of 0.5 V, while exhibiting a (-3 dB) bandwidth of 11 MHz for (V_y/V_x) and 10 MHz for (I_x/I_z), respectively. The CCII had a power dissipation of 30 μW. The CCII was then employed to realise the 3rd order leap frog filter giving remarkable performance under the give constraints.

Zhao *et al.*[35] presented an impressive technique to increase the transconductance of the bulk driven OTA. This led to the improvement in bandwidth and input referred noise of the implementation. The current recycling together partial positive feedback method was employed to achieve the desired objective. Figure 10 shows, the cross coupling of transistor M3 and the current mirrors M4 and M5 cross over connection provided the positive feedback and current recycling, respectively. The aspect ratios of the input bulk driven transistors and the rest of the transistors were carefully chosen facilitating transconductance enhancement as can be seen in Fig. 11. To improve the output impedance of the OTA modified composite transistor structure with bulk biasing was used. The bulk of the upper transistor was biased with a positive voltage leading to the decrease in the threshold voltage and subsequent increase in the drain to source voltage of lower transistor moving it into saturation and thus increasing the output impedance. Finally, the OTA was realised using the transconductance enhancement and bulk biasedcomposite transistor techniques. The OTA was fabricate in 0.18 μm CMOS technology. The values of sizing parameters m and n were selected 0.5 and 0.6, respectively. The OTA achieved 8 fold improvement in transconductance. While operating under 1 V the OTA exhibited a gain bandwidth product of 29.6 MHz and the dc gain of 86.1 dB.

An OTA circuit with DTMOS technique was proposed by Khumsat and Worapishet[36] as shown in Fig. 10. The designed OTA circuit operated under 0.5 V supply with a 61 dB dynamic range at 1% THD consuming 0.6 mW and it was used as the active element to realise a fifth-order chebyshev filter.

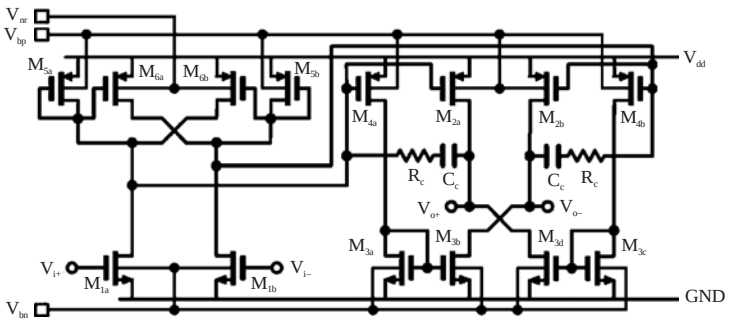

Fig. 10: Circuit of 0.5 V OTA using DTMOS technique[36]

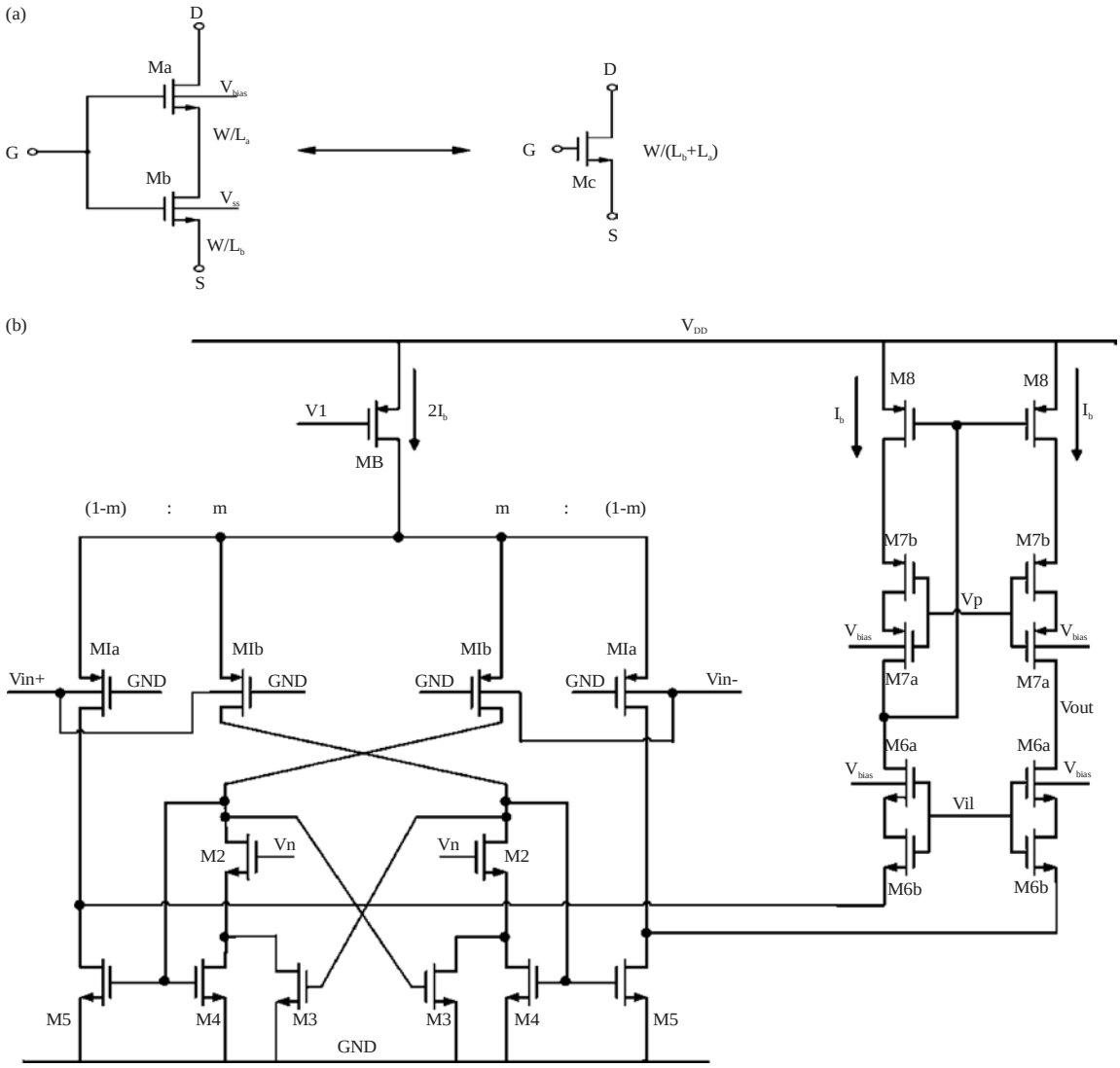

Fig. 11(a-b): (a) Bulk driven composite transistor (b) Bulk driven OTA with transconductance enhancement scheme[35]

However, to reach the bodies of both PMOS and NMOS transistors in the circuit, an expensive triple-well fabrication process was used. Maymandi-Nejad and Sachdev[37] discussed the DTMOS technique and to highlight its usefulness they proposed continuous time common mode feedback (CMFB) scheme for differential amplifier which is an essential stage for OTAs and CCs. The use of DTMOS decreased the power consumption and simplified the circuit

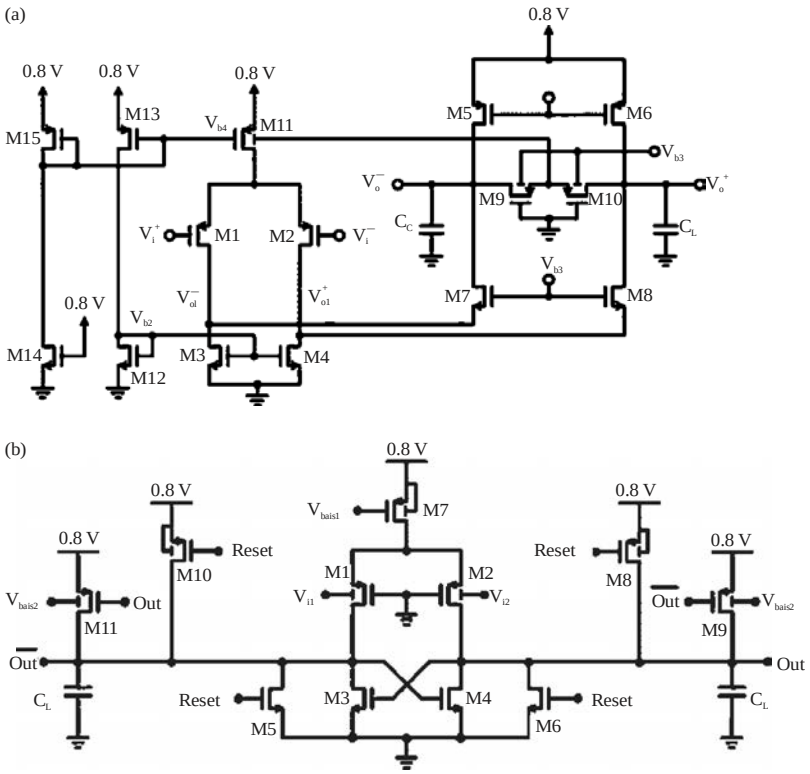

Fig. 12(a-b): DTMOS based (a) CMFB (b) Quantizer[37]

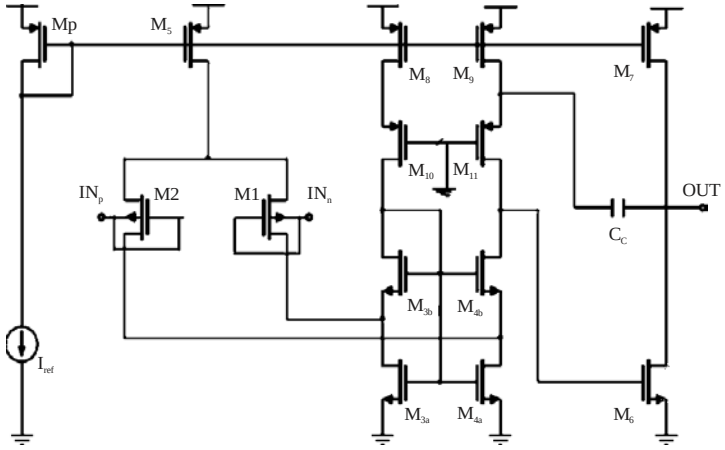

Fig. 13: 0.4 V DTMOS OTA[38]

implementation. It is reported that when applied to differential pair the technique improved the CMRR by 12 dB. In the same article a quantizer circuit with rail-rail operation was also proposed using the DTMOS. The supply voltage used was 0.8 V for both the designs emphasizing the effectiveness of DTMOS in low voltage analog design. The circuits of CMFB and quantizer are shown in Fig. 12.

Kargaran *et al.*[38] effectively applied the DTMOS technique in OTA design to achieve ultra-low voltage operation. The designed OTA worked at 0.4 V while having a unity gain bandwidth of 111.4 kHz and a power dissipation of 386 nW. The scheme as shown in Fig. 13 utilised circuit composed of PMOS DTMOS differential pairs and current mirrors operating in subthreshold regime. Uygur and Kuntman[39] presented a CCII working at 0.4 V supply. The circuit was designed for ultra-low voltage and low frequency operation. The DTMOS and subthreshold region operation were utilised. The circuit had only eight transistors and dissipated a power

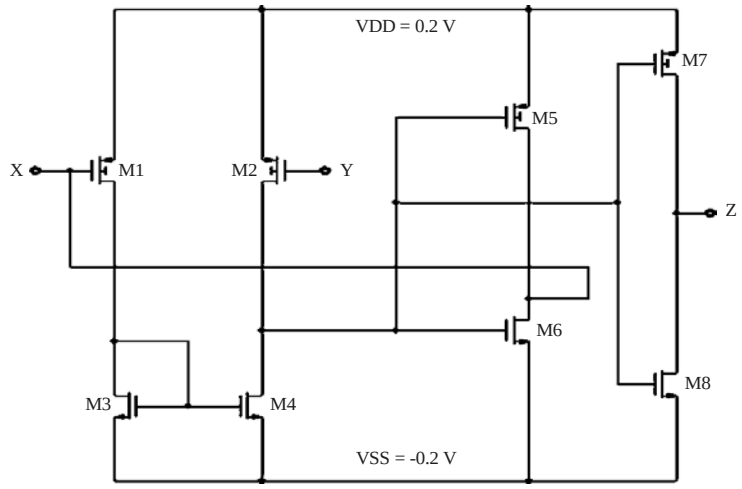

Fig. 14: DTMOS based CCII[39]

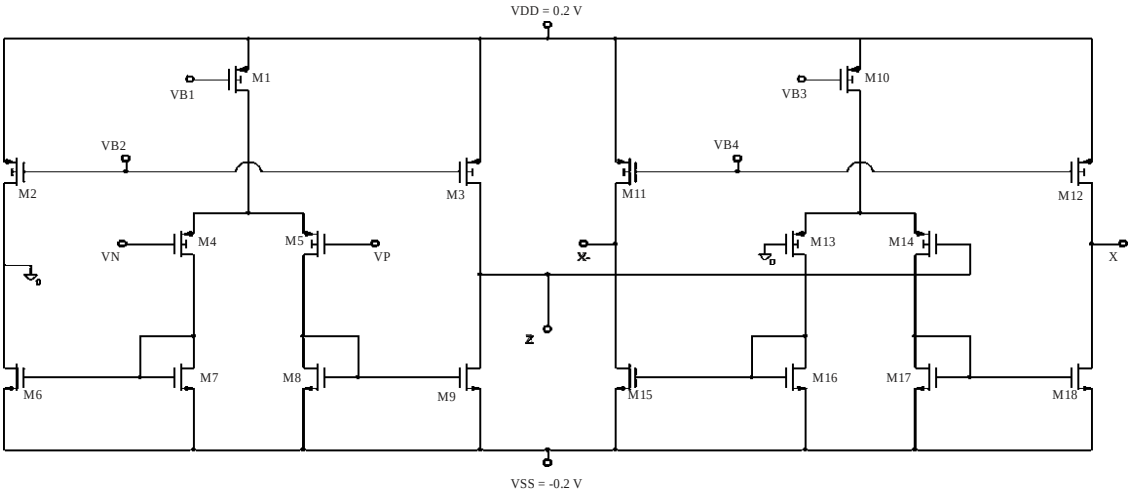

Fig. 15: DTMOS based VDTA[40]

of 214 nW while providing a 570 kHz, 3 dB bandwidth between X and Y terminals. The circuit arrangement is depicted in Fig. 14. A band pass filter was successfully synthesized using the CCII for speech processing applications. Uygur and Kuntman[40] presented another variant of CC the Voltage Differencing Transconductance Amplifier (VDTA). The circuit was realised by connecting two DTMOS OTAs. Since the n-well process is considered for the design only PMOS DTMOS transistors were available. The circuit topology of the VDTA is shown in Fig. 15. All the PMOS transistors utilised in the circuit are DTMOS. Designed in 0.18 µm, the circuit operated in subthreshold region at 0.4 V supply. The circuit's 3 dB frequency was 3.3 kHz with a reported power dissipation of 5.96 nW. As an application a fourth order band pass filter was constructed and used in processing low frequency electroencephalogram (EEG) signals.

The exemplary LVLP circuit of CCCII was presented by Ercan *et al.*[41]. The circuit utilised a low voltage DTMOS based differential pairs and low voltage PMOS level shifter current mirrors. The bodies of the input transistors of the differential pair are connected to the drain of input device M1 as shown in Fig. 16a so the threshold voltage will change dynamically this enable the differential pair to work at low voltage. Two differential pairs with the bodies of their input transistors tied together and connected to level shifter transistor M5 were used to realise CCCII as presented in Fig. 16b and by simply altering the connections of the different nodes on can get both positive and negative parasitic resistance at node X which was the exclusiveness of the circuit. When simulated in 0.18 µm TSMC parameters the circuit achieved (-3 dB) bandwidth of 70 MHz for (V_y/V_x) and 130 MHz for ($I_x/I_{(z+, z-)}$), respectively. The parasitic resistance

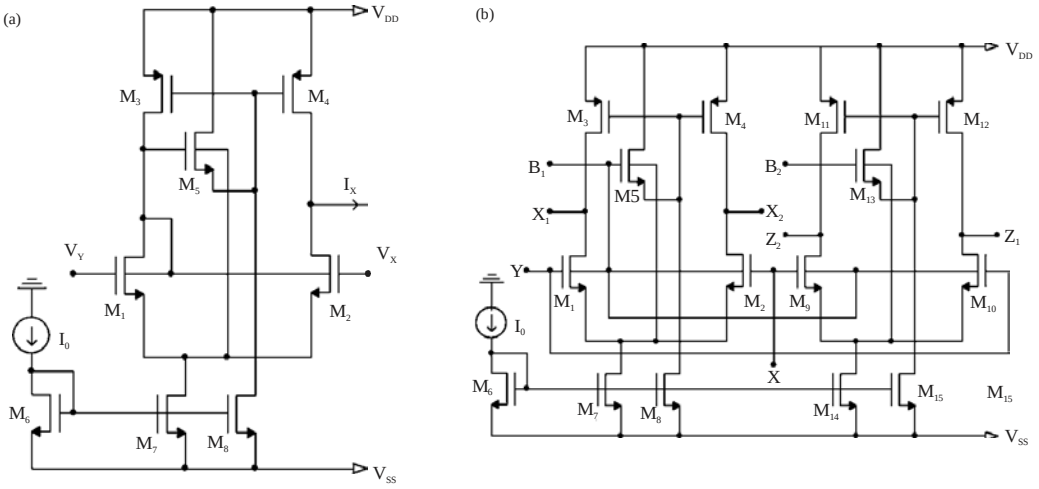

Fig. 16(a-b): (a) Low voltage DTMOS based differential pair and (b) CCCII circuit with DTMOS differential pair[41]

Table 1: Comparison between various current conveyor topologies based on the MOSFET body techniques

Parameters	Kumngern and Khateb[19] CCII+	Khateb *et al.*[22] CCII±	Uygur and Kuntman[39] CCII+	Ercan *et al.*[41] MFCCCII±	Suwansawang and Thongleam[32] FDCCII+
Technique used	BD*	BD*	DTMOS**	DTMOS**	BD*
Power consumption μW	4.7	64	0.21	4.8	403.77
Supply Voltage V	0.5	±0.4	±0.2	±0.5	1
3 dB bandwidth (I_{Z+}/I_X) MHz	25	13	-	130	30
3 dB bandwidth (I_{Z-}/I_X) MHz	-	12.5	-	130	-
3 dB bandwidth (V_Y/V_X) MHz	15.8	14	0.57	70	25.7
Voltage gain (V_X/V_Y)	-	1	-	0.989	-
Current gain (I_{Z+}/I_X), (I_{Z-}/I_X)	-	1	-	0.985	-
Node×parasitic impedance (Ω)	950	27	964	Can be tuned from (3.8 k to 1.4 M)	-
Node Y/input impedance (MΩ)	30×10^3	∞	11.8	∞	-
Node Z+/Z-/output impedance (MΩ)	10.9	0.89	2	4.28	-
Technology used	0.18 μm	0.18 μm TSMC	0.18 μm TSMC	0.18 μm TSMC	0.18 μm TSMC
DC input voltage range (mV)	400	±380	±60	±150	-
DC input current range (μA)	±4	±7	-	-	-

*BD: Bulk driven, **DTMOS: Dynamic threshold MOS

showed a wide tuning range of 3.8 k to 1.8 M. The circuit operated at ±0.5 V dissipating a very low power of 4.8 μW. The CCCII was successfully employed in inductance simulation and band pass filter applications.

The implementation of these techniques to current conveyor is still in a developing phase as limited literature is available but at the same time it opens a new area for research in this domain. Table 1 compares few of the CC implementations discussed on various performance parameters. Moreover, the applications utilizing the body driven and dynamic threshold current conveyors are limited compared to their gate driven counterpart so this is also an area calling for extensive research to design and optimize applications for these active blocks. The evaluation of various active elements yielded enough evidence that these techniques are capable of realising state of art universal current mode building blocks exhibiting exemplary performance. Although, the circuits presented showed good performance but the limited input dynamic range and the operational frequency pose new challenges that need to be overcome and the researchers are pursuing their study in this direction.

RESEARCH FOCUS AND IMPLEMENTATION PROCEDURE

The circuits reviewed were state of the art but the study pointed out several issues related to the use of body techniques. First, the bulk driven circuits did not achieve high bandwidth compared to their gate level counter parts due to low body transconductance this issue can be overcome by boosting the transconductance of the body driven transconductor as was shown by Zhao *et al.*[35] in Fig. 11. The second issue is that the body technique is not utilised to its full potential since most of the designs used the body terminals only in the input devices. The DTMOS technique is still not ubiquitous and more circuits needs to be designed exhibiting

higher frequency response to prove its usefulness. The researchers believe that new innovative techniques they are working on can overcome these shortcomings and aims at designing high performance active building blocks like current mirrors, differential amplifiers using the body techniques. All these elements will then be employed in designing novel current mode active blocks CC and OTA yielding enhanced performance over the others. The active blocks will be designed for tunable filter and inductance simulations as the target applications for low frequency implantable biomedical devices and high frequency communication systems. Filter are an integral part of any electronic system and there numerous implementations are available in literature[41-44] so, this study will be focused in realising current mode filtering applications. Filter implementations that will be realised includes KHN state variable filters[43], Tow-Thomas biquad[43] and universal filter structures. The CC and OTA are designed to achieve a frequency response in the range of 100-500 kHz for low frequency applications and frequency response in the range of 4-200 MHz for high frequency applications. The operating supply voltage will in the range of 0.4-0.8 V while power consumption will be between 10 nW to 100 μW.

To highlight the direction and objective of the study a graphical representation is given in Fig. 17 and 18. The implementation procedure and design methodology that will be adopted is depicted Fig. 19. At the onset a thorough

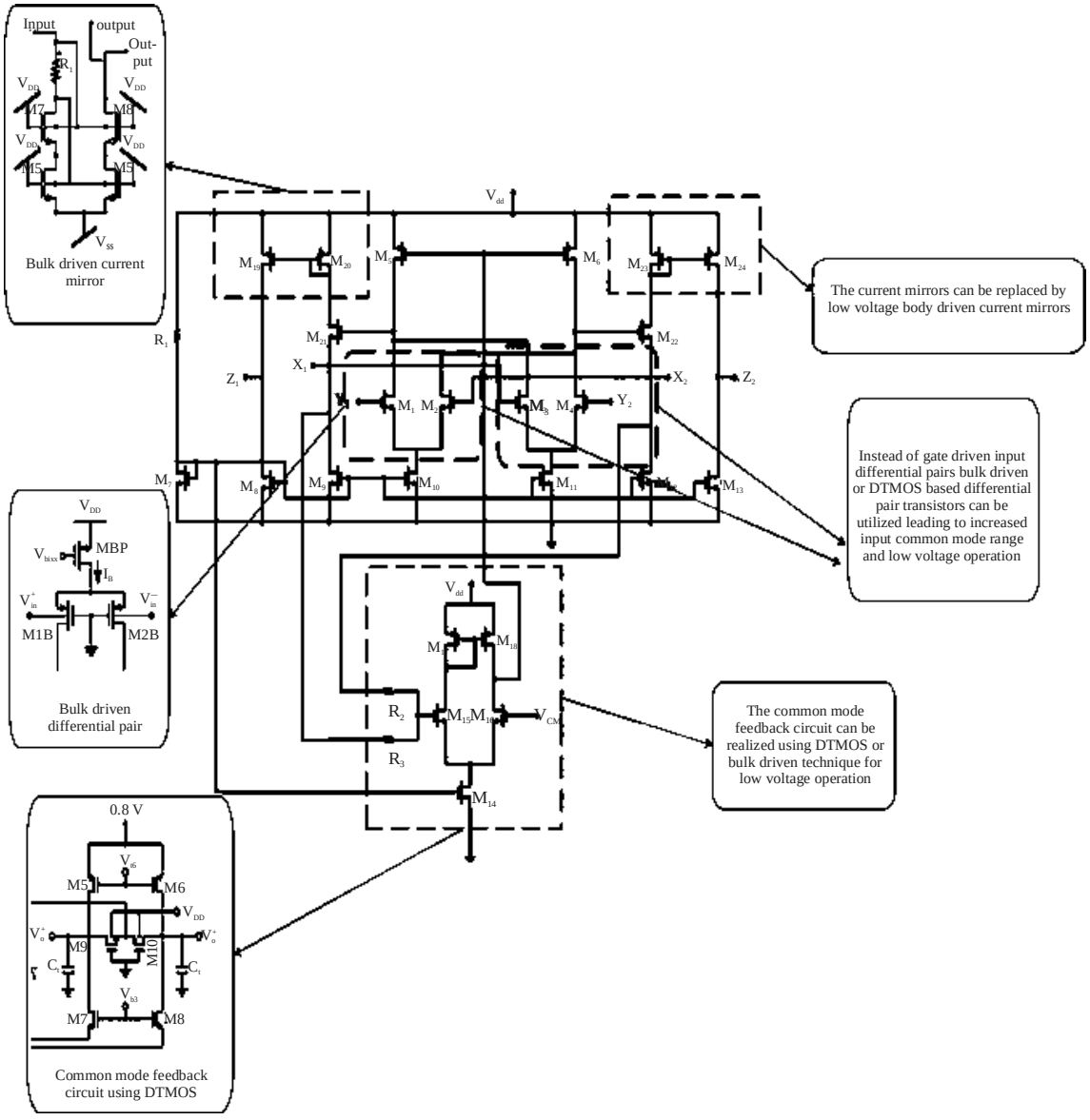

Fig. 17: Graphical representation of the research areas and direction of the research. The circuit adopted for depicting the areas and focus of the proposed research[45]

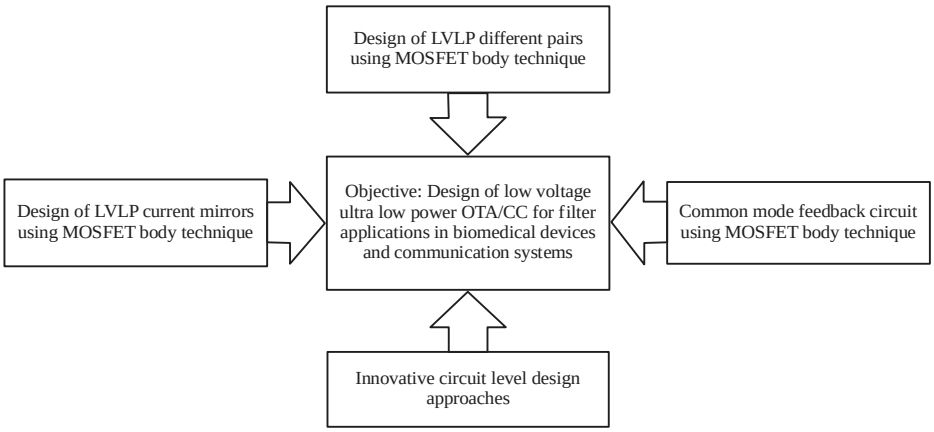

Fig. 18: Graphical representation of the objective of the research

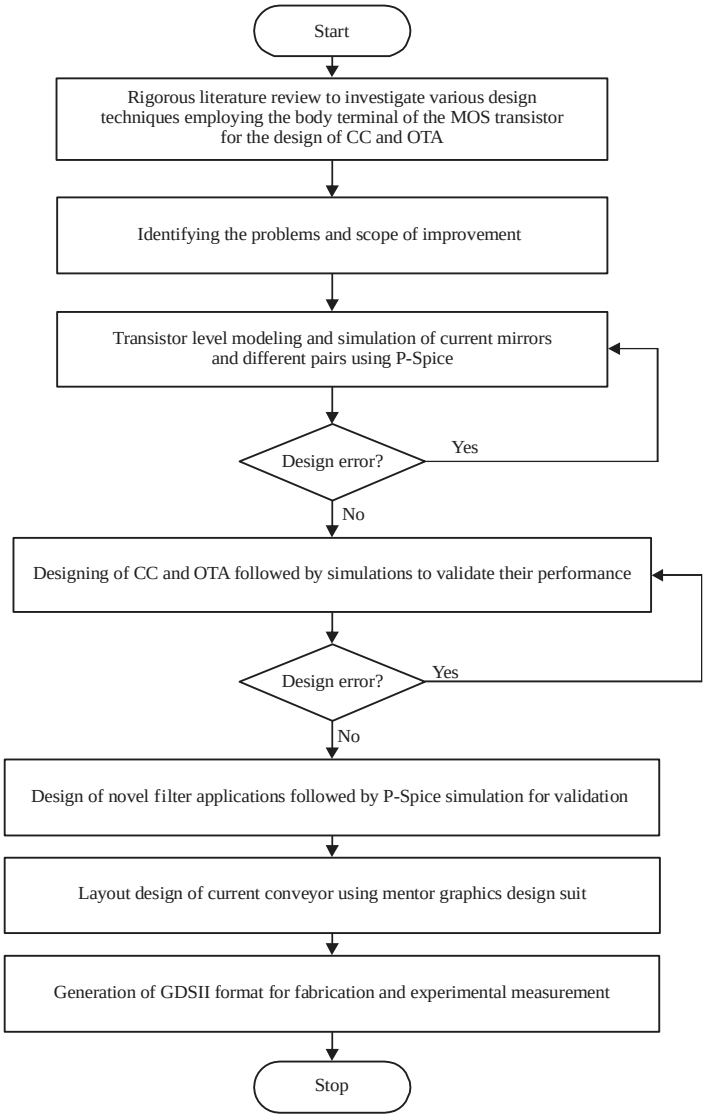

Fig. 19: Design procedure of CC and OTA using the body techniques

literature review is done to investigate various design techniques utilizing the body terminal then the existing problems and the scope of improvement will be established. The circuit level modelling is then done to hand calculate various design parameters in 0.18 µm TSMC technology node. The current mirrors and differential pairs will then be designed and simulated using BSIM 3v3.1 model in P-Spice to ascertain their behaviour and get the measure of various parameters. If the design fails to achieve the targeted design specifications then the circuit configuration will be reanalysed until the design constraints are satisfied. After that the designing of current mode active blocks (CC ant OTA) will be carried out followed by their characterization through rigorous simulations. Once the circuits are deemed fully functional then novel filter applications will be developed for these blocks and there performances are evaluated using extensive simulations. The mentor graphics IC station and design architect IC suites will then be used for layout design of current conveyor followed by generating GDSII format for fabrication. The experimental analysis of the fabricated chip will then be carried out.

CONCLUSION

A brief study of the MOSFET body techniques followed by the analysis of novel operational transconductance amplifier and current conveyor realizations using the body techniques is performed. This study was focused on their performance and range of application they are capable to realise. The study pointed that the techniques are capable of providing excellent performance if innovative design approaches coupled with new methods to overcome their limitations are effectively employed in designing the active blocks. The authors are confident that when these techniques are utilized together with novel circuit level design strategies new high performance topologies of the current conveyors and operational transconductance amplifiers capable of ULVLP operation can be designed. The designed CC and OTA are expected to achieve a frequency response in the range of 100-500 kHz for low frequency applications and frequency response in the range of 4-200 MHz for high frequency applications. The operating supply voltage will in the range of 0.4-0.8 V while power consumption will be between 10 nW to 100 µW. The designed active blocks will then be utilised in designing novel tunable filter implementations suited for integration in biomedical devices and communication systems.

SIGNIFICANCE STATEMENTS

The study reviews two techniques utilizing the body terminal of the MOSFET for ultra-low voltage low power design namely bulk driven MOS and Dynamic threshold MOS techniques. The principles of the two techniques, including a technical analysis of their applicability and limitations are presented. The state of art recently proposed operational transconductance amplifier and current conveyor designed using the body techniques are reviewed in terms of various performance parameters like the supply voltage requirement, power dissipation, frequency response and dynamic range. The challenges in using the body techniques of the MOSFET are pointed out and the researcher's direction of future research to overcome these limitations in designing operational transconductance amplifier and current conveyor for tunable filter applications are highlighted.

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