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Research Article
Implementation of Distributed Arithmatic Based Reconfigurable FIR Digital Filter

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Abstract

This study presents an implementation of a Distributed Arithmetic (DA) based reconfigurable Finite Impulse Response (FIR) filter whose filter coefficient dynamically change during runtime. This DA based structure replaces all required multiplication and addition by a Look Up Table (LUT) and shift accumulator. The dual port dynamic RAM (DRAM) used in this work is to reduce the total size of LUT by half. The scheme which are using in shift accumulator doubles the throughput, since two inner products are computed concurrently. Systolic system which consists of an array of processing element in a pipeline structure is used for application such as image processing and signal processing. The proposed work uses mainly a DA based systolic architecture which yields faster output compared to the multiplier-accumulator based design because it stores the pre computed partial result in the memory and used it in computation. The entire architecture is implemented in FPGA from ALTERA family. The proposed architecture consumes 70 nW thermal power in which core static and I/O thermal power dissipations are 47.36 and 22.64 nW, respectively. Another main advantage over DRAM is high data rate, wide data bus size and maximum throughput.

Key words: Distributed arithmetic, finite impulse response, reconfigurable architecture, systolic system, look up table

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INTRODUCTION

Reconfigurable implementation of Very Large Scale Integration (VLSI) architecture is playing crucial role now-a-days to accommodate more complex functions or subsystem into single system-on-a-chip designs (Sivanantham *et al*., 2014). Finite Impulse Response (FIR) digital filters are more used due to their role in Digital Signal Processing (DSP) applications. With the advancement in Very Large Scale Integration (VLSI) field, the high speed of FIR filter has more demanding. The complexity of implementation of filter grows with the filter order and the precision of computation. The concept of Distributed Arithmetic (DA) based reconfigurable FIR digital filter on Field Programmable Gate Array (FPGA) was presented in (Shreeharsha and Bhandarkar, 2011). A reconfigurable FIR filters are filter whose filter coefficient dynamically changes during run time was described in (Park and Meher, 2014). However, multiple constant multiplication technique, which is used for FIR filter implementation can't be used when the filter coefficient is changed.

A Distributed Arithmetic (DA) based technique is very popular because of its high throughput processing capability. The main operations in DA based computation are a sequence of Look Up Table (LUT) accessed followed by shift accumulation operation. The memory requirement for DA based technique for FIR filter is increase with increasing the order of coefficient of filter. To eliminate this problem, Meher *et al*. (2008) suggested systolic technique for large number of order (Gougam and Benazzouz, 2010).

Reconfigurable DA based FIR filter (Chen and Chiueh, 2006) need the use of rewritable RAM based LUT. This study present an efficient scheme for the shared LUT implementation of reconfigurable FIR filters using this DA based technique in which LUTs are shared by the DA units.

The ASIC implementation of DA based FIR filter also proposed by Park and Meher (2014). The main operation which is required in DA based techniques is a sequence of Look Up Table (LUT) selection followed by shift accumulation. The LUT and also shift and add operation can efficiently and easily mapped to FPGA (Park and Meher, 2014). Therefore, DA based computation is well suited for FPGA realization.

The proposed architecture called Distributed Arithmetic (DA) based reconfigurable Finite Impulse Response (FIR) filter whose filter coefficient dynamically change during runtime. The DA based structure replaces all multiplication and addition by a Look Up Table (LUT) and shift accumulator so as to speed up the operations. The proposed work utilize a dual port dynamic RAM (DRAM) to reduce the total size of LUT by half. The scheme which use shift accumulator doubles the throughput, since two inner products are computed concurrently. Systolic system which consists of an array of processing element in a pipeline structure is used for application such as image processing and signal processing. This study focuses mainly on the use of DA based systolic architecture which yields faster output compared to the multiplier-accumulator based design because it stores the pre computed partial result in the memory and used it in computation.

Reconfigurable architecture: Reconfigurable architecture means the architecture which is change at run time i.e., the change at runtime is occur in different levels of architecture. The reconfigurable architecture can be classified into main three levels:

- **System level:** In system level, reconfiguration is corresponding to the programming of the computing element i.e., different processor and memory
- **Function level:** In function level, reconfiguration is corresponding to interconnection between resources like different arithmetic modules like ALU
- **Logic level:** At logic level, the reconfiguration is deals with different LUTs and interconnection at bit level

The proposed architecture deals with "Logic level reconfiguration architecture". In DA based reconfigurable FIR digital filter, the coefficient of filter is change at run time dynamically. For, implementing this on FPGA platform, different LUTs are reconfigured. In DA based technique, all computation are replaced by LUTs. Whenever, coefficient is change at run time, it is necessary to change computational with the use of LUTs. Because of this nature the proposed architecture is called as logic level reconfigurable architecture.

MATERIALS AND METHODS

In most DSP application, out of two sequences one of the sequence derived from the input samples while the other sequence is usually fixed. The basic of distributed arithmetic is to replace all multiplication and addition by a look up table and a shifter accumulator. Basically it's extreme computational efficiency and capability of reducing the number of gate count in a signal processing unit is the motivation for using distributed arithmetic (Meher, 2006). The shift accumulator efficiently doubles the throughput since two inner products are computed concurrently (Eq. 1).

$$Y = \sum_{n=0}^{N-1} c[n] \times x[n] \quad (1)$$

In FIR, one of the convoluting arrangements is gotten from the info while the other succession is gotten from the settled coefficients of the channel. This conduct of FIR channel makes it conceivable to utilize DA based system. It gives speedier yield contrasted with other system in light of the fact that in this coefficient stores the precomputed incomplete results in the memory which can be perused out and collected to acquire the fancied result. This is another motivation behind why DA based structural planning generally utilized as a part of different DSP application.

FPGA implementation: A Field Programmable Gate Array (FPGA) is an integrated circuit intended to be designed by a client or an architect in the wake of assembling. Fundamental advantages of FPGAs incorporate the capacity to re-program in the field which is use in settle the bugs and may incorporate a shorter time to market and lower non-repeating building expenses. The LUT in FPGA gadgets contains just two bits of registers. Therefore, LUTs are required to be implemented by distributed RAM (DRAM) for FPGA (Melluer, 2006).

Here, DRAM based partial product generator (DRPPG) is used to give partial product of input and the coefficient of FIR filter. Then PPG is divided into Q section and each parallel Q section has R operation which belongs to R bit. If L is positive number and L=R×Q then Q is parallel section and R is input bit slices. The output of the filter is given by Eq. 2 (where q and r are section and time index, respectively). Here, R is time slot of same duration as clock period then we can have filter output at every R cycle.

$$Y = \sum_{q=0}^{Q-1} 2^{-R} \left[\sum_{r=0}^{R-1} 2^{-r} \left(\sum_{p=0}^{P-1} S_{r+qR,p} \right) \right] \quad (2)$$

The architecture of DA based FIR filter with R = 4 and M = 2, which is shown in Fig. 1a. The input sequence X (n) is given to Serial In Parallel Out (SIPO) register. The output of this register is goes to DRAM based partial product generator (DRPPG). Dual port DRAM used to reduce the total size of LUTs by half because at a time two DRPPG are sharing one DRAM. The structure of DRPPG is shown in Fig. 1b. This structure produces partial inner product in a single clock cycle. This DRPPG generate partial products which are added by Pipeline Adder Tree (PAT). The output of PAT are input of shift accumulator which is shown in Fig. 1c. Finally, Pipeline Shift Adder Tree (PSAT) produces the output of filter at every R cycle. If the clock period is f, this architecture can support the input rate of f/R.

RESULTS AND DISCUSSION

This section present the proposed DA-Based FIR filter architecture for R=4 and M=2, is implemented on ALTERA Cyclone II FPGA device (EP2C20F484C7). The clock frequency of 250 MHz is considered for the evaluation. For FPGA, implementation gives higher throughput for R<L. Power analysis was done to calculate the power of the whole architecture i.e., how much power dissipated by architecture. Similarly, with the use of timing analysis the setup time for the circuit and the contamination delay (i.e., minimum delay to get the output) of the circuit were computed. The power analysis and timing analysis of this structure is shown in Table 1 and 2, respectively.

From the Table 1, it is observed that the proposed DA based architecture consume thee total thermal power dissipation of 70 uW in which core static and I/O thermal power dissipation is 47.36 and 22.64 uW, respectively. In timing analysis, the set up time is 6.98 n sec and worst case contamination delay is 9.024 n sec.

Table 3 presents the power and area report of various works and are compared against the DA based FIR Filter. It is observed that both Floating-point Computation Sharing Multiplier (FCSHM) and Floating-point Carry-Save Array Multiplier (FCSAM) presented in (Sivanantham *et al*., 2013) consume more power compared to other technique since floating-point computational unit require more area against fixed point computational unit. The digit-serial technique (Nichat *et al*., 2014) and slice reduction techniques (Umasankar and Vasudevan, 2013) based FIR implementation need an area of 27050 and 28000 cells, respectively, which is comparable to the proposed DA based reconfigurable FIR filter technique. However both techniques consume more power as compared to DA based technique. The digit-serial technique consume 3.42 mW and slice reduction technique consumes 1.247 mW of power whereas DA based FIR implementation consume only 0.07 mW power. This is mainly due to the reconfigurable feature enable in the proposed technique results in reduction of dynamic power due to lesser switching activities. The shift-add technique based FIR filter consumes more power of 5.83 mW as well as occupies larger area of 28455 as expected. The main reason is more shift-add operations are required to perform multiplication. Also the other two methods like FCFHM and FCSAM also require more area due to floating-point implementations.

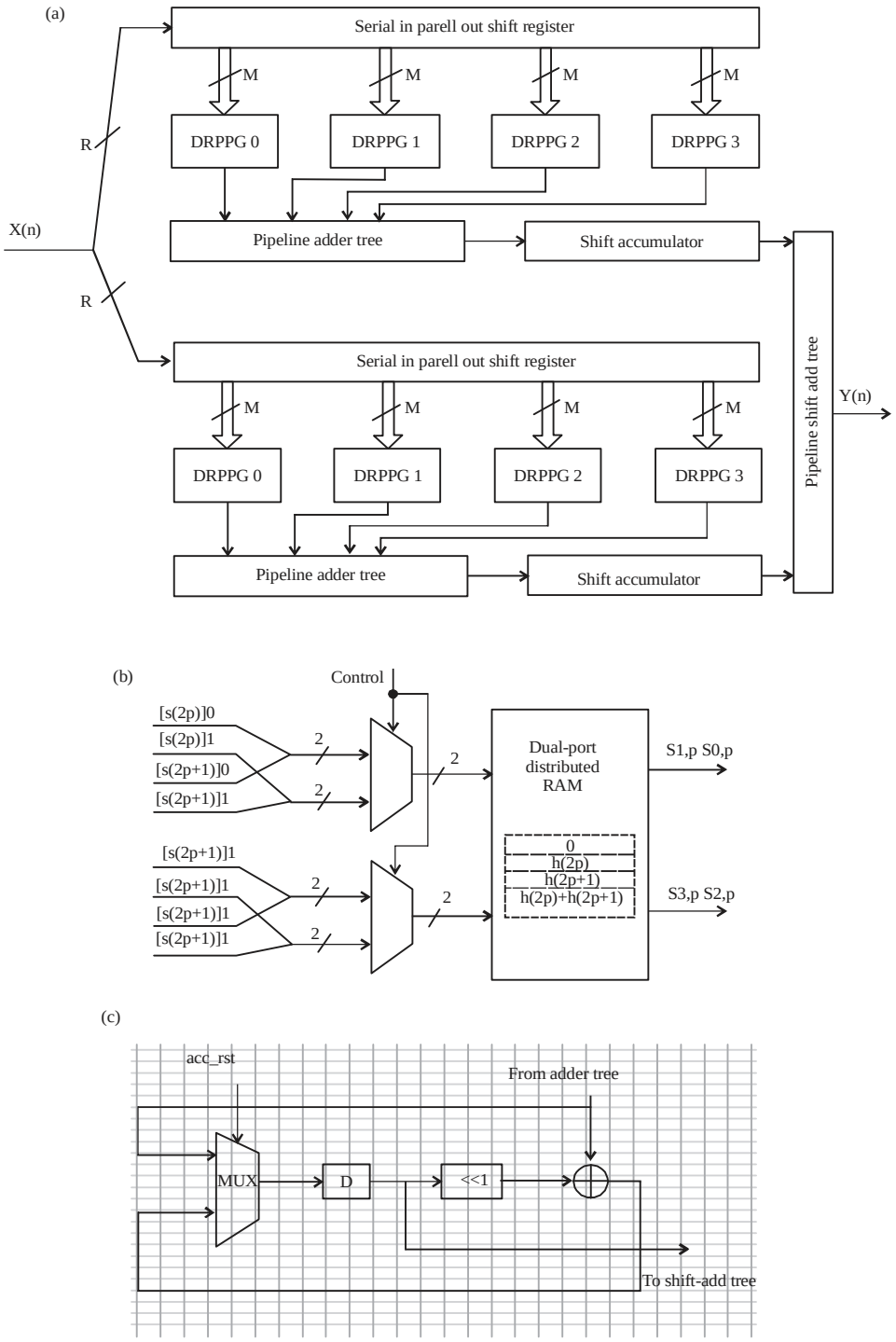

Fig. 1(a-c): Structure of (a) DA based FIR filter, (b) DRPPG for M= 2 and (c) Shift accumulator

Table 1: Power analysis of distributed arithmetic based reconfigurable finite impulse response filter

Types	Power (μW)
Core static thermal power dissipation	47.36
I/O thermal power dissipation	22.64
Total thermal power dissipation	70.00

Table 2: Timing analysis of distributed arithmetic based reconfigurable finite impulse response filter

Types	Actual time (ns)
Clock Frequency (MHz)	243.550
Worst case time (set up time)	6.985
Worst case time (contamination delay)	9.024
Worst case time (threshold time)	3.277

Table 3: Comparison of power and area analysis

Types	Power (mW)	Area	References
Digit-serial	3.420	27050	(Nichat *et al*., 2014)
Slice reduction	1.247	28000	(Umasankar and Vasudevan, 2013)
Shift-add	5.830	28455	(Nichat *et al*., 2014)
FCFHM	83.750	46521	(Sivanantham *et al*., 2013)
FCSAM	138.930	36703	(Sivanantham *et al*., 2013)
This work	0.070	28000	

FCFHM: Floating point computation sharing multiplier and FCSAM: Floating point carry assay save multiplier

CONCLUSION

An implementation of a Distributed Arithmetic (DA) based reconfigurable Finite Impulse Response (FIR) filter was presented. A methodology to dynamically change the filter coefficient during runtime was described so as to minimize the switching activities there by the total power has been reduced. The analysis for power dissipation, areas consumption for the proposed architecture was given and compared against various other techniques. From the result, it was observed that this architecture can be used to find finite impulse response of a given sequence in the run time and it clearly indicates that the architecture is suitable for high speed applications.

The Dual port DRAM used in the architecture also used to store the value of partial product in DRPPG. The DRAM stores each bit of data in a separate passive electronic component that is inside an integrated circuit board. The DRAM needs to be refreshed after few times otherwise data will be fades. The DRAM access time is 60 n sec which is small compare to other DRAM. Rambus DRAM (RDRAM) can be used in place of DRAM, since RDRAM have built-in self-refresh capability. Also it has high bus rate so data transfer will be faster because in RDRAM data transfer will be on both positive as well as negative edges of a clock. One of the major advantages of using RDRAM is that each chip can be selected by its own ID so separate chip select can be avoided as described in the architecture. The other advantages include its high data rate, wide data bus size and maximum throughput. So, using RDRAM may slightly increase the area overhead than DRAM but data transfer rate will be very high.

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