



Asian Journal of Scientific Research

ISSN 1992-1454

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Research Article

Implementation of On-chip Optical Interconnect in High Speed Digital Circuit: Two-stage CMOS Buffer

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Abstract

Background: Silicon based photonics has created strong interested in recent years, mainly in optical waveguide interconnects for microelectronic circuits. **Materials and Methods:** This study reports on the implementation of an Optical Interconnect (OI) waveguide in a digital electronic circuit, a two-stage CMOS buffer. To compare the performance between several waveguide materials with copper interconnect, the optical waveguide was designed and evaluated in OptiBPM to be in a single mode condition. Then, the OI link was simulated in OptiSPICE and their ability as an interconnection was tested in a two-stage CMOS buffer. A propagation delay performance for the whole circuit and for the interconnection only was measured using different material of interconnect. **Results:** The results showed that the OI minimized the propagation delay in the two-stage CMOS buffer circuit, as well as increased the speed of the integrated circuit. **Conclusion:** The proposed SOI-based optical waveguide in OI link are able to replace copper based electrical interconnection in electronic circuit technology.

Key words: Optical interconnect, waveguide, CMOS buffer, copper interconnect, propagation delay

Received: October 14, 2016

Accepted: November 15, 2016

Published: December 15, 2016

Citation: Siti Sarah Binti Md. Sallah, Sawal Hamid Md. Ali, P. Susthitha Menon, Nurjuliana Juhari and Md. Shabiul Islam, 2017. Implementation of on-chip optical interconnect in high speed digital circuit: Two-stage CMOS buffer. Asian J. Sci. Res., 10: 50-55.

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Competing Interest: The authors have declared that no competing interest exists.

Data Availability: All relevant data are within the paper and its supporting information files.

INTRODUCTION

Interconnect is a communication medium to link electronic components or devices in electronic chips. The performance of conventional electrical copper interconnect has degraded substantially in terms of speed, delay, power dissipation and crosstalk noise in accordance with the continuous demand for speedy and highly complex integrated circuits¹. Thus, on-chip Optical Interconnect (OI) has been considered to replace the copper interconnect as an alternative method in integrated circuit technology due to its superior advantages in providing higher bandwidth density, minimizing power consumption, as well as reducing interconnect delays and noise^{2,3}. Figure 1 shows the theoretical block diagram of OI, which contains continuous source (CW), optical waveguide, modulator and photodetector.

This simulation was divided into two-stages. The 1st stage is to design the optical waveguide based on SOI, InGaAsP and polymer and the second stage is to implement the OI in a digital circuit-a, two-stage CMOS buffer. We compare several electrical performances, such as transient input/output and the propagation delay between copper interconnect and the OI for the two-stage CMOS buffer circuit.

MATERIALS AND METHODS

Electrical interconnect in two-stage CMOS buffer: A buffer is used to delay a short period of signal or to amplify a signal and a voltage buffers are widely employed to drive low-impedance load⁵. A two-stage CMOS buffer circuit was simulated with RLC equivalent model for electrical interconnect defined in predictive technology model⁶ using standard 32 nm CMOS technology as shown in Fig. 2.

Optical interconnect in two-stage CMOS buffer: The same circuit was simulated with optical waveguide as the interconnection between stages. A Single Mode Condition (SMC) is important among various optical waveguide devices. A number of researchers have identified the potential of SOI-based⁸, InGaAsP-based and polymer-based^{9,10} waveguides for OI and compatible fabrication process to allow for a complete integration between the CMOS layers and the optical layers.

Figure 3a-c shows the cross section and their design dimensions, while Fig. 3d-f shows the SMC output of each layout design produced by OptiBPM.

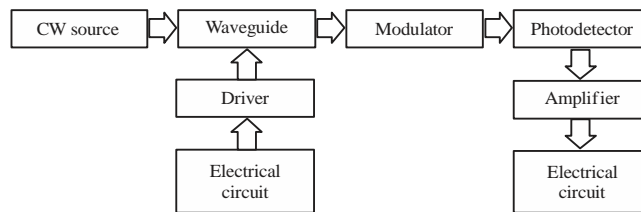


Fig. 1: Optical interconnect link⁴

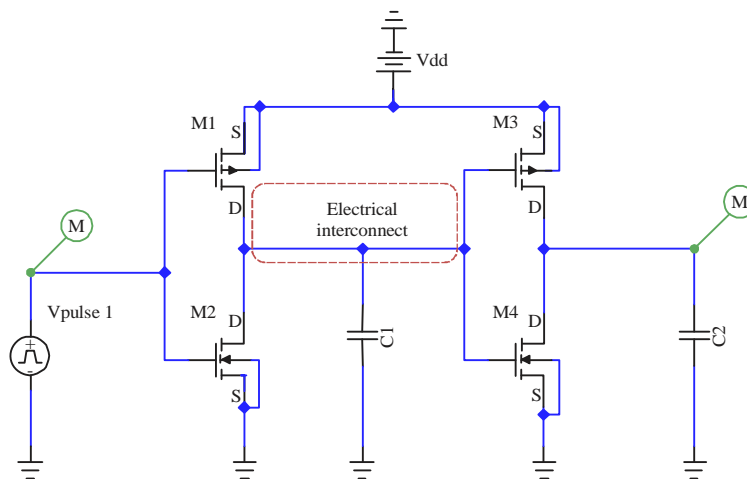


Fig. 2: Two-stage CMOS buffer with electrical interconnect⁷ (using conventional RLC-lumped model)

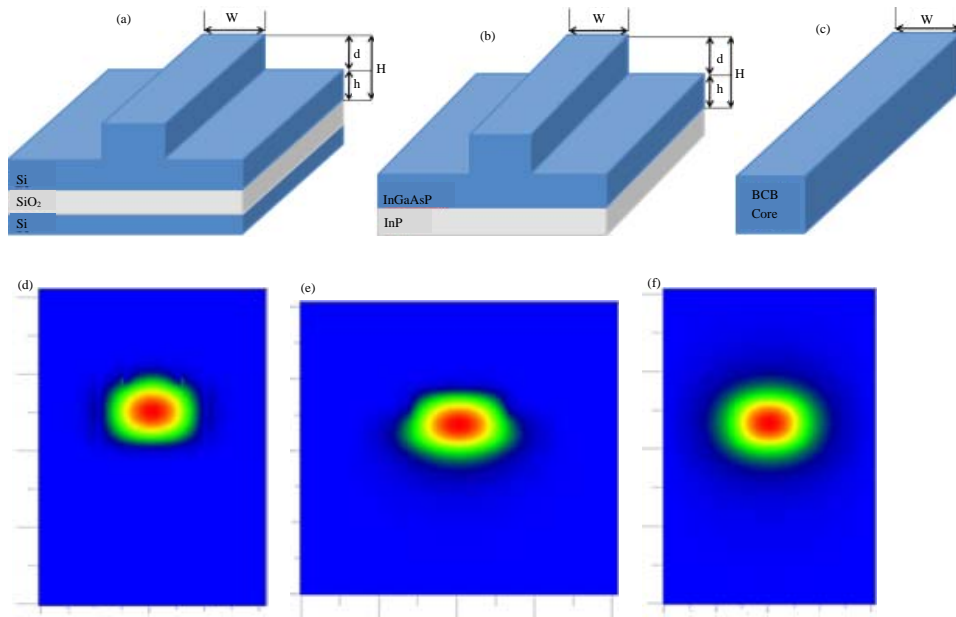


Fig. 3(a-f): Simulation outputs of optical waveguides in OptiBPM, (a) Cross section of SOI waveguide, (b) Cross section of InGaAsP waveguide, (c) Cross section of polymer waveguide, (d) SMC output of SOI waveguide, (e) SMC output of InGaAsP waveguide and (f) SMC output of polymer waveguide

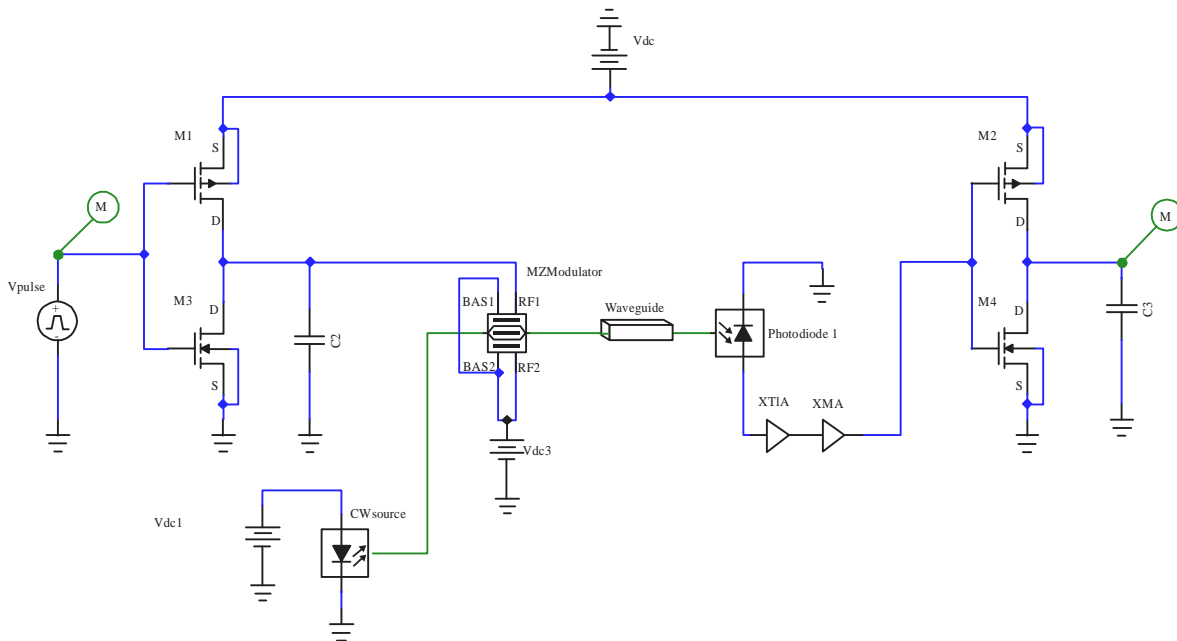


Fig. 4: Two-stage CMOS Buffer with optical interconnect link

Width (W) dimensions of Si, InGaAsP and the polymer were 0.8, 3 and 3 μm , respectively. All waveguide lengths was 100 μm . The height (H) for the Si waveguide was 1 μm . The effective refractive index (n_{eff}) depends on the waveguide material. The n_{eff} for the polymer, InGaAsP and SOI waveguide were 1.542, 3.273 and 3.308, respectively. This

waveguide parameter will be used in the analysis of two-stage CMOS buffer circuit with OI link.

Figure 4 shows the schematic circuit of the two-stage CMOS buffer with OI link. Using OI, the propagation delay of the two-stage CMOS buffer could be decreased.

RESULTS

We have simulated and compared the performance of the copper interconnect versus the OI in terms of transient analysis, propagation delay (τ_P) of the whole circuit and the τ_P of the OI alone. Transient analysis is important to calculate the τ_P of the two-stage CMOS buffer. Figure 5a and b shows the transient input/output of the two-stage CMOS buffer using copper interconnect and SOI waveguide.

The τ_P can be calculated using the Eq. 1:

$$\tau_P = \frac{\tau_{PLH} + \tau_{PHL}}{2} \tag{1}$$

where, τ_{PLH} is the time taken to rise to 50% and τ_{PHL} is the time taken to drop to 50%. The τ_P for the two-stage CMOS buffer was measured by tagging the probe at the input and output stage. The τ_P for the whole circuit using copper interconnect was approximately 0.64 nsec, while the τ_P using OI was approximately 0.1 nsec.

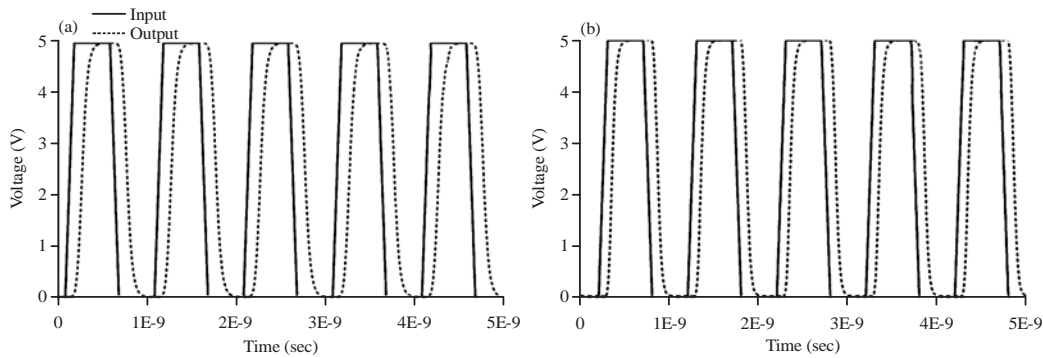


Fig. 5(a-b): Transient input and output of two-stage CMOS buffer, (a) Transient input/output using copper interconnect and (b) Transient input/output using SOI

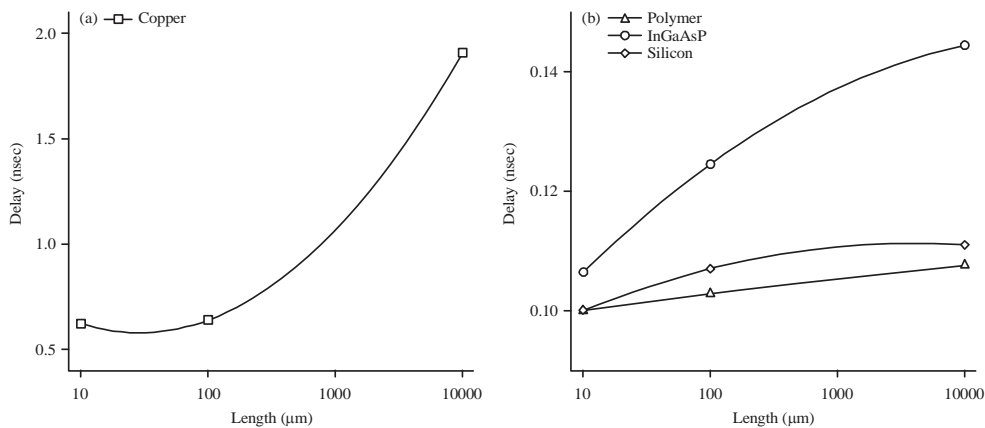


Fig. 6(a-b): Propagation delay for whole circuit versus waveguide length, (a) Circuit propagation delay using copper interconnect and (b) Circuit propagation delay using OI

DISCUSSION

The delay of an optical link τ_{opt} is given¹¹ as in Eq. 2:

$$\tau_{opt} = \tau_{tx} + \tau_{wg} + \tau_{rx} \tag{2}$$

where, τ_{tx} is the delay of the transmitter, τ_{wg} is the delay of the waveguide and τ_{rx} is the receiver delay.

However, the optical interconnect waveguide delay can be examined since their size and propagation delay depend on the waveguide geometry and their refractive index depend on the wavelength of light^{12,13} as shown in Eq. 3:

$$\tau_{wg} = n_{eff} \frac{L}{c} \tag{3}$$

where, n_{eff} is the effective index of the mode in the waveguide medium, c is the speed of light and L is length of waveguide.

Figure 6 compares the τ_P of the two-stage CMOS buffer for the copper interconnect and OI with different

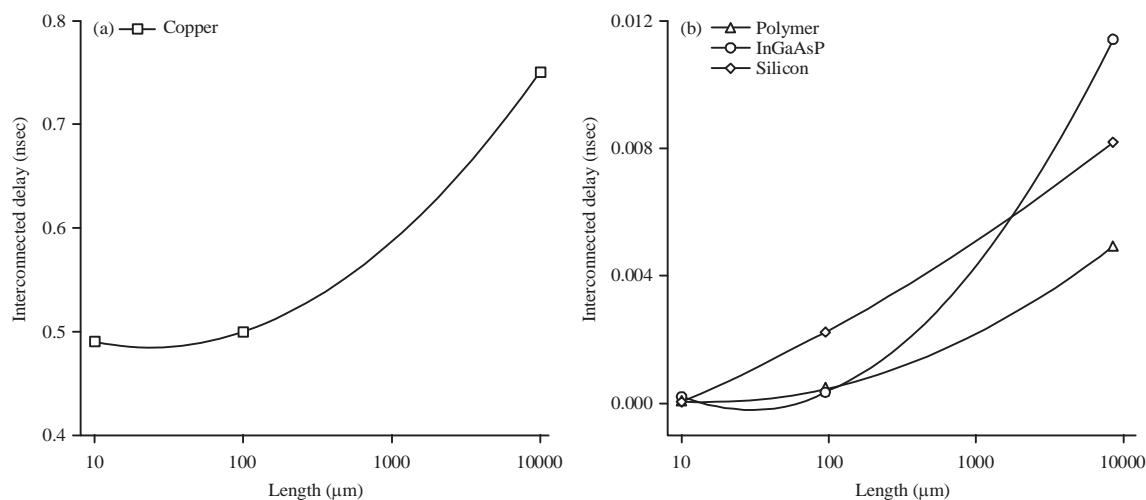


Fig. 7(a-b): Delay of interconnect versus length of waveguide, (a) Interconnect delay of copper interconnect and (b) Interconnect delay of different materials: Polymer, InGaAsP and SOI

waveguide materials using 10, 100 and 10000 μm in length. The τ_P for copper interconnect was much higher compared to the OI.

The τ_P for interconnect link can also be evaluated by tagging the probe before and after the RLC circuit and before and after the OI link. Figure 7a and b plots the τ_P for only the interconnect link.

CONCLUSION

The integration of OI link in the digital electronic circuit has successfully improved the performance of the two-stage CMOS buffer. We have also compared the performances between the copper interconnect with 3 different material of optical waveguide interconnect, such as SOI, InGaAsP and polymer. It can be concluded that the propagation delay has been reduced significantly with OI in two-stage CMOS buffer.

ACKNOWLEDGMENT

This study was assisted by University Kebangsaan Malaysia (grant DPP-2015-059).

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