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Performance Evaluation of a Hiperlan Type 2 Standard Based on Arithmetic Formats

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Abstract: An optimum fixed-point word length to implement the physical layer of Hiperlan type 2 is proposed in this paper. The software based HIPERLAN/2 WLAN standard is implemented based on fixed-point and floating-point arithmetic formats. Extensive simulation technique is used to analyze the effect on performance of different word lengths of fixed point data representation the HIPERLAN/2 system. The results obtain could also be used as a guideline to select the optimum hardware for the systems based on OFDM technique. It is shown that a simple fixed-point based architecture could be used to implement the physical layer of Hiperlan/2 standard. By using the software models the proposed fixed-point architecture's performance is compared to that of a reference complex and accurate floating point based architecture.

Key words: WLAN, OFDM, HIPERLAN, FFT

INTRODUCTION

Wireless Local Area Networks (WLAN's) have attracted considerable interest and attention due to their ability to offer network access anywhere, anytime, at high data rates of up to 54 Mb/s. Several standards have been developed in the 5-GHz band, namely the High Performance Local-Area Networks type 2 (HIPERLAN/2) by European Telecommunications Standards Institute (ETSI) Broadband Radio Access Networks (BRAN), High Speed wireless Access Networks type a (HiSWANa) defined by Mobile Access Communication Systems (MMAC) and 802.11a defined by IEEE[1]. A good overview WLAN's is given in Nicopolitidiset *et al.*[2].

ETSI BRAN project has developed standards and specifications for broadband radio access networks that cover a wide range of applications. The systems covered by BRAN are categorized based on applications are: HIPERLAN/1 a wireless local area network intended to allow high performance wireless networks to be created, without existing wired infrastructure. HIPERLAN/2 intended to provide a short range wireless access to IP, ATM and Universal Mobile Telephony System (UMTS) networks, HIPERACCESS intended to provide outdoor, high speed (25 M bits^{-1} typical data rate) radio access, it provides fixed radio connections at the customer premises and is capable of supporting multimedia applications, HIPERLINK intended to provide point-to-point interconnection at very high data rates, e.g. up to 155 M bits^{-1} over distances up to 150 m[3].

HIPERLAN/2 is intended to provide local wireless access to IP, ATM and UMTS infrastructure networks by both stationary and moving terminals that interact with access points which, in turn, usually are connected to an IP, UMTS or ATM backbone network. A number of these access points will be required to service all but the smallest networks of this kind and therefore the wireless network as a whole will support hand-overs of connections between the access points. Further more, such a wireless access network will be able to provide the Quality of Service (QoS), including required data transfer rates, that users expect from a wired ATM network.

The desired hardware features for HIPERLAN/2 as any other wireless applications are size, power consumption, processing speed and computational accuracy. And these factors are not independent i.e. accuracy depends on the size and processing speed, in order to get accurate results the corresponding hardware size will be bigger and its processing speed will be slower and vice versa[4,5].

Here we have targeted the core orthogonal frequency division multiplexing (OFDM) function of HIPERLAN/2 physical layer as the basis of our analysis to find the optimum fixed point word length. OFDM in HIPERLAN/2 is realized by a complex 64 point fast Fourier transform (FFT)[1]. FFT is a complex function whose implementation parameters i.e. its hardware size, computational accuracy and speed depends on the type of arithmetic format used[6]. Due to non-linearity of the FFT function it is not easy to compute its computational accuracy

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Table 1: Transmission modes and mode dependent parameters

Mode	Modulation	Coding rate R	Nominal bit rate M bits^{-1}	Coded bits per sub-carrier	Coded bits per OFDM symbol	Data bits per OFDM symbol
1	BPSK	½	6	1	48	24
2	BPSK	¾	9	1	48	36
3	QPSK	½	12	2	96	48
4	QPSK	¾	18	2	96	72
5	16QAM	9/16	27	4	192	108
6	16QAM	¾	36	4	192	144
7	64QAM	¾	54	6	288	216

Table 2: Numerical values of DM parameters

Parameter	Value
Sampling Rate (f_s)	20.0 MHz
Useful Symbol Duration (T_U)	3.2 μs
Guard Interval Duration (T_g)	0.8 μs
Total Symbol Duration (T_{Total})	4.0 μs
Number of data sub-carriers (N_D)	48.0
Number of pilot sub-carriers (N_P)	4.0
FFT Size	64.0
Sub-carrier spacing (Δ_f)	0.3125 MHz
Total Bandwidth (B)	16.875 MHz

analytically,therefore simulation or statistical models are used instead.

In this study a simulation based approach is used to evaluate the performance of HIPERLAN/2 standard based on different arithmetic formatted OFDM block. Results obtained are used to propose optimum word length needed to implement Hiperlan/2 standard.

We have designed two software HIPERLAN/2 physical layer models, one based on fixed-point and the other on floating point to simulate the performance of the models on different arithmetic platforms. Fixed-point model is designed to simulate different bit-depths by simply changing the parameter. But user has to prepare/design the input data such that it should not cause overflows at the intermediate stages. This is done to minimize the rounding errors. Floating point based physical layer model is used as a reference.

Simulation models also simulates the indoor wireless channel for performance analysis. Only 1000 Long Protocol Data Unit (PDU) trains[1] are transmitted over the simulated channel to calculate the performance of the models for a specific signal to noise ratio (SNR) because fixed-point computations take very long time.

The HIPERLAN/2 standard: HIPERLAN/2 is a WLAN standard operating in the 5 GHz band. Utilizing a bandwidth of 20 MHz, nominal user data rates ranged between 6 and 54 M bits^{-1} can be supported. The physical layer of HIPERLAN/2 is based on a link OFDM modulation scheme. The Data Link Control (DLC) layer of HIPERLAN/2 is based on a centrally controlled network topology with dynamically assigned medium access based on Time Division Duplex (TDD) and Time Division Multiple Access (TDMA) within a 'MAC frame' with duration of 2 ms. The HIPERLAN/2 standard also defines a number of Convergence Layers (CLs) to interface the DLC to higher level network structures such as TCP/IP, ATM and UMTS. These Convergence Layers ensure that HIPERLAN/2 is suitable for a wide array of WLAN applications from office LANs to wireless home networks to cellular network 'hotspot' coverage.

Physical layer: The HIPERLAN/2 physical layer[1] is based on the use of OFDM. OFDM is used to combat frequency selective fading and to randomise the burst errors caused by a wideband-fading channel. A link adaptive modulation scheme is specified, with a number of transmission 'modes' defined. These physical layer modes employ different coding and modulation schemes to achieve a flexible trade off between SNR requirements and error performance. The seven specified modes in HIPERLAN/2 are defined in Table 1 and are selected by a link adaptation scheme. The exact mechanism of this link adaptation process is not specified in the standard and will thus be determined by individual manufacturer's designs.

Figure 1 shows the reference configuration of the HIPERLAN/2 transmitter. Data for transmission is supplied to the physical layer in the form of an input PDU train. This PDU train is supplied to the physical layer by the DLC. Each PDU consists of either 9 bytes of control data (short PDU) or 54 bytes of 'user' data (Long PDU). The output of the physical layer is a 'physical layer burst' consisting of a preamble followed by the modulated PDU train.

The PDU train is input to a scrambler that prevents long runs of 1s and 0s in the data being input to the remainder of the modulation process.

The scrambled data is input to a convolutional encoder. The encoder consists of a 1/2 rate mother code and subsequent puncturing. The puncturing schemes facilitate the use of the code rates: 1/2, 3/4 and 9/16. Additional puncturing is also used in order to keep an integer number of OFDM symbols with 54 byte PDUs.

The coded data is interleaved in order to prevent error bursts from being input to the convolutional decode process in the receiver.

Table 3: Developed system's key parameters

Mode	Modulation	Coding rate	Viterbi decoder type	Type of PDU	Type of FFT block
3	QPSK	½	Hard-Decision	Long (54 Bytes)	Radix-2 Decimation in Time (4)

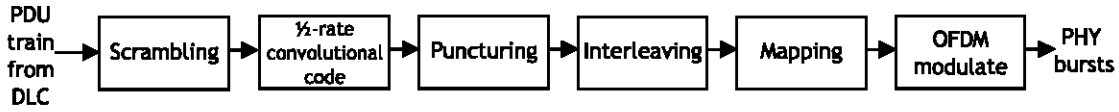

Fig. 1: HIPERLAN/2 PHY layer reference transmitter

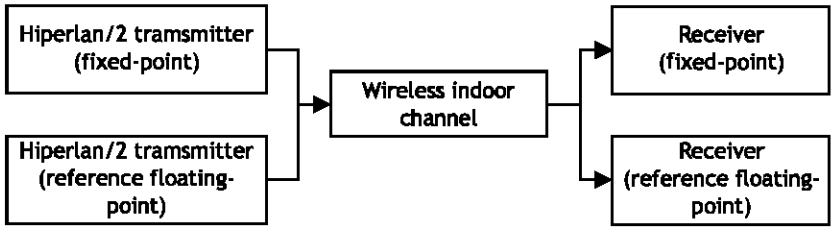

Fig. 2a: Test bed for measuring the performance of a different word length fixed-point based H/2 system

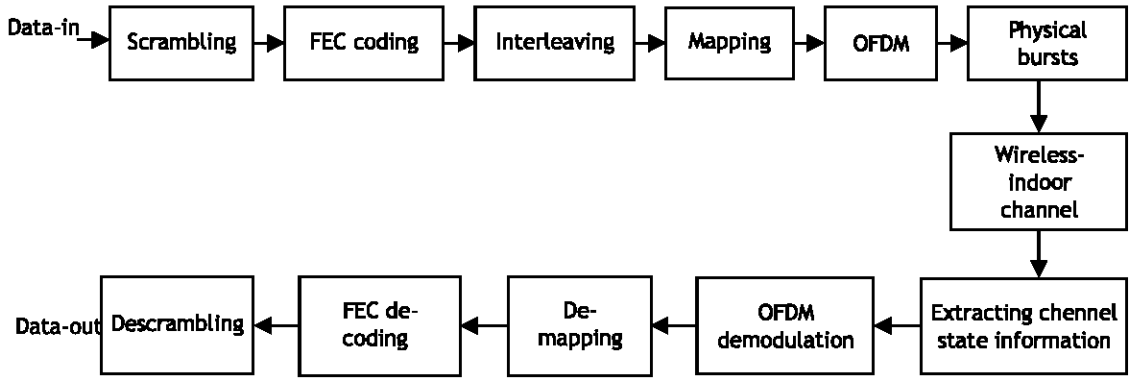

Fig. 2b: Block diagram of the physical layer of Hiperlan/2 based system

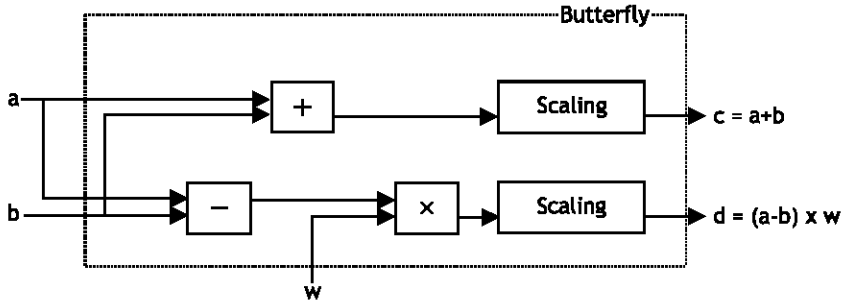

Fig. 3: Block diagram of a butterfly used within FFT

The interleaved data is subsequently mapped to data symbols according to either a BPSK, QPSK, 16-QAM or 64-QAM scheme. The OFDM modulation is implemented by means of an inverse FFT. 48 data symbols and 4 pilots are transmitted in parallel in the form of one OFDM symbol.

Numerical values for the OFDM parameters are given in Table 2. In order to prevent Inter-Symbol Interference (ISI), a guard interval is implemented by means of a cyclic extension. Thus, each OFDM symbol is preceded by a periodic extension of the symbol itself. The total OFDM symbol duration is given by ETSI[1]

$$T_{total}=T_g+T \quad (1)$$

where T_g is the guard interval and T is the useful symbol duration. When the guard interval is longer than the excess delay of the radio channel, ISI is eliminated.

The OFDM receiver essentially performs the reverse operations of the transmitter. However, the receiver is also required to undertake Automatic Gain Control (AGC), time and frequency synchronisation and channel estimation. Training sequences are provided in the preamble for the specific purpose of supporting these functions. Two OFDM symbols are provided in the preamble in order to support the channel estimation process. A priori knowledge of the transmitted preamble signal facilitates the generation of a vector defining the channel estimate, commonly referred to as the Channel State Information (CSI). Decoding of the convolutional code is implemented by means of a Viterbi decoder.

System model/simulation model: Test bed for measuring the performance of fixed-point based H/2 system is shown in Fig. 2a. Where floating point model is used as a reference. Whereas Fig. 2b depicts a block diagram of the physical layer of Hiperlan/2 based system. Systems are modeled using Matlab as a high level language. Key parameters used within the base band systems are summarized in Table 3.

Similar work has also been carried out in Tariq *et al.*[7] where H/2 physical layer is implemented using digital signal processor (DSP). There is one drawback in implementing a system in DSP that is DSP is a general purpose processor and is not optimize for a certain application. That is hardware in case of DSP is fixed and flexibility is achieved using software. It is quite possible by slightly modifying the hardware one can achieve a great improvement in speed and performance, which in case of DSP could not be achieved.

Here we have developed a software based model of a physical layer to study the different architectures. Within the model, data is represented by a fixed-point format and all the computations are based on fixed-point arithmetic as well. Simulation model is developed (i.e. coded) such that it could be implemented into FPGA's or ASIC chip for optimum performance. FPGA is a piece of hardware that could be easily reconfigured. Here one can design his own hardware by simply programming it (www.xilinx.com). Techniques like pipelining and/or parallel processing could be implemented to achieve high data rates as well.

Implementation of a FPGA based solution of H/2 requires the optimum selection of a word length. Here we have used simulation based approach for this purpose. Simulations could be done in two ways, either by coding the system directly in hardware description language (HDL), or by simulating the design using any high level language. We have selected the second option of simulating the original hardware into a high level language, because it is easy and fast way to get the performance of the actual hardware.

Developed reference floating point system model uses Matlab built in floating point data representation to perform computations. While in fixed-point model only OFDM block is fully coded to simulate the fix-point arithmetic format.

Analysis: Fixed-point arithmetic unit is designed in the Matlab to simulate the fixed-point arithmetic processor platform. System is designed such that different bit depths could easily be adjusted simply by changing the variable. User has to adjust the range of input data so that results after computation does not overflow often, which will result in rounding errors. If the input data range is kept very small then it still will generate errors again due to rounding, i.e. small range data will be rounded to zero. Rounding is performed within the FFT stages after every arithmetic operation to cope with overflows.

Block diagram of a single butter fly (BF) used within the FFT Fig. 3. As shown in the Fig. 3, scaling is performed at two places within the BF. Scaling is based on simple right shift i.e. results after multiplication are scaled by dividing it by two. To minimize rounding error the results are only scaled after multiplication and addition. While intermediate results of subtraction are not scaled.

RESULTS AND DISCUSSION

The results show a comparison between fixed-point and floating point based HIPERLAN/2 system. System used for generating results is based on QPSK mode and channel used in simulation is ETSI type A[8] with root mean square (RMS) delay spread of 50 ns.

PDU error rates (PER) results are used in the results instead of BER (Bit Error Rate) because in a Hiperlan/2 system, the required level of packet retransmission is a key parameter, which is dependent on the PER. The number of PDU trains used to measure the PER for a specific SNR were 1000. For the completion of results comparison between BER for different SNR are also included. Fig. 4 shows the comparison between various bit depth fixed point based system and floating point based for several signal to noise ratios.

From Fig. 4 it could be seen that the performance of 16-bit fixed-point architecture is comparable to floating point based highly accurate architecture. It should be

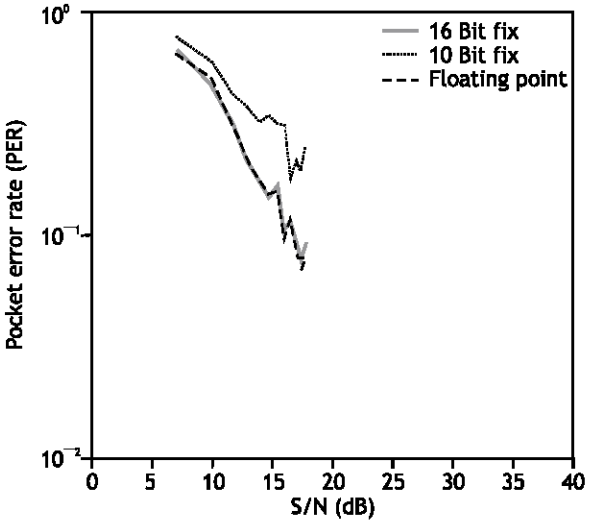

Fig. 4: PER results for 50 ns type A channel and mode 3 for transmission (Hard decision Viterbi decoding and 16 bit OFDM Architecture)

noted that the floating point based hardware is not only bigger in size but also high power consumer and both of these factors are not suitable for wireless applications. Therefore, it is concluded that the 16-bit fixed-point architecture is more suitable to implement the HIPERLAN/2 physical layer.

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