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A Fully Optimized Switched Current Class AB Grounded Gate Memory Cell

M. Fakhfakh, M. Loulou and N. Masmoudi
Laboratoire d'Electronique et des Technologies de l'Information,
National Engineering School of Sfax, Tunisia

Abstract: Optimally designing Switched Current (SI) memory cells is a very tedious process. In addition, it is usually limited to the design of ideal cells. This study we deal with fully optimizing these cells and particularly real cells. Since SI class AB grounded gate memory cells are well known to be improved cells, we applied the proposed heuristic to design these cells. Also, besides maximizing performances and minimizing famous error sources, we focus on optimally sizing transistors forming switches and bias currents. The optimization procedure, developed in C++ software, allows automatic design of the cell. It is also highlighted in the followings. The cell designed with the use of CMOS 0.35 μm process under a single 3.3 V power voltage supply, achieves more than 83.6dB as a dynamic range and reaches less than 3.5 ns as settling time.

Key words: Switched Current (SI), class AB, grounded gate

INTRODUCTION

Switched current (SI) technique is relatively a new analogue sampled data technique that overcomes problems associated with its counterpart; the switched capacitor technique. Indeed, SI memory cells do not require added capacitors and can be integrated into standard CMOS process (Hughes *et al*., 2000). Since their introduction, a wide variety of SI circuit structures have been studied (conventional class A structure, class AB topology, grounded gate lie, etc.) (Hughes *et al*., 2000). In many cases performance limitations of these circuits have been explored (Hughes *et al*., 2000; Toumzou *et al*., 1993). However, design aspect and transistor sizing optimization process have not been enough explored (Toumzou *et al*., 1993). This is mainly due to both complexity of such high performance cells and to tight interaction existing between desired performances and device characteristics.

The objective of this study was to propose a heuristic for optimizing SI memory cells. This optimization procedure was applied for designing fully optimized SI class AB grounded gate cells.

CLASS AB GROUNDED GATE SI MEMORY CELLS

Class A memory cell's driving principle consists of the ability of the intrinsic gate to source capacitance of a MOS transistor to hold on a voltage corresponding to the drain to source current reached at the end of acquisition time. This sets the memory transistor to be driven by the corresponding current (Toumzou *et al*., 1993). Even though this kind of cells does not present any mismatch problem, it's performances are lessened by two handicaps (Toumzou *et al*., 1993; Oliaei and Loumeau, 1996); Firstly, input current range is limited; it can not exceed the quiescent current I_0. Secondly input-output node voltage varies considerably from acquisition to restitution as well as current which affect output current. Grounded gate class AB memory cell, shown on Fig. 1, has remedied to both problems (Toumzou *et al*., 1993; Oliaei and Loumeau, 1996): In the class AB topology, current is memorized thanks to capacitances C_N and C_P of two complementary transistors

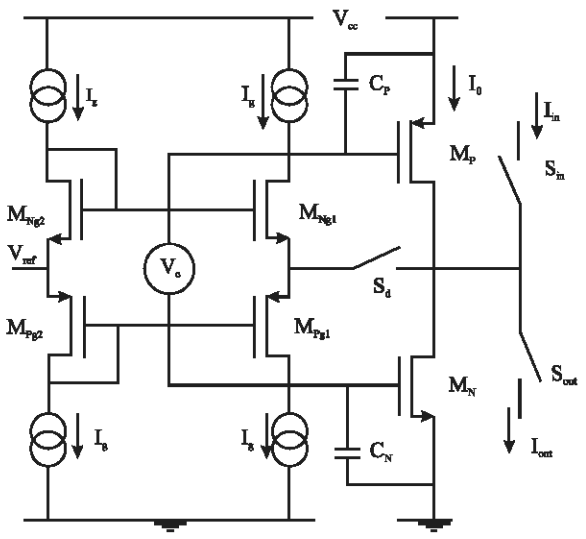

Fig. 1: Ideal grounded gate class AB memory cell. V_c is the floating source and I_g is the voltage follower current conveyor bias current

Corresponding Author: Mourad Fakhfakh, BP 1069 Sfax 3018, Tunisia Tel : +216 98 975 285 Fax: +216 74 247 498

MN and MP, thus, it is proved that input current can be four times higher than I_0. The grounded gate lie, composed of transistors M_{Ng1}, M_{Ng2}, M_{Pg1} and M_{Pg2}, forms a feedback loop which have the effect of holding on the voltage input-output node constant, thus reducing not only the input to output conductance ratio error but also signal dependent charge injection error.

THE ADOPTED HEURISTIC

The heuristic we propose consists of optimizing the cell's performances by transistor sizing (O'Connor and Kaiser, 2000). It is composed of four successive approaches:

Firstly, lower and upper boundaries for each parameter (transistors' geometric dimensions and current conveyor bias current) are determined. These limits are necessary for the optimization algorithm in order to know each parameter swing range useful to restrict calculation time. In fact, this approach consists on building a simplified model for the cell in order to coarsely and rapidly generates a valid range for each parameter, Building mathematical models for the error function degrading the cell's performances, fixing coarsely the tolerated precision ranges for each error and finally calculating swing range boundaries.

Secondly, an Objective Function (OF) is built. It is a weighted sum of error and performance reduced functions. In deed, knowing that these functions have different range values; we modified and presented them in reduced entities. The OF can be written as follows (Fakhfakh *et al.*, 2004):

$$OF = \sum_{i=1}^{N} \gamma_i \left(\frac{Err_i - \min(Err_i)}{Max(Err_i) - \min(Err_i)} \right)^{\omega i} \quad (1)$$

Where, N is the number of error functions, min(Erri) and Max(Erri) represent the minimal and the maximal value of the i^{th} error function, respectively. γi and ωi are weighting coefficients.

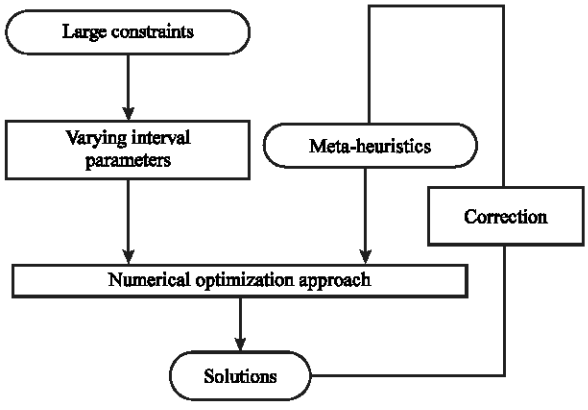

Fig. 2: The proposed heuristic

Thirdly, a diversification procedure has to be done. It is a global stochastic exploration of the research field. It is based on the creation of a data vector for each parameter and the random choice of an examinee row parameter every iteration.

Finally, optimal values are extracted, Simulations are done with these new transistor's dimensions, the new (already fixed) constants are then (re)extracted, the algorithm parameters are so updated, then restart the cycle until optimal values are reached.

We notice that the heuristic is developed with C++ software. We also put the stress on the fact that objective function, to optimize, consists of minimizing input output conductance ratio error, charge injection errors and reduced time response (by minimizing $\left|\xi - \frac{\sqrt{2}}{2}\right|$ and maximizing ω_0) and maximizing SNR. Respective equations can be found by Fakhfakh *et al.* (2004).

Finally, we emphasize the fact that, since the approach is a random one, the C++ algorithm takes less than ten minutes to calculate a hundred times the optimal solutions and it converges at 87%.

OPTIMIZING VOLTAGE AND CURRENT BIAS SOURCES

The cell presented at Fig. 1, is an ideal one. Owing to the algorithm driven methodology for transistor sizing, depicted above, this cell gives very high performances for both precision and settling accuracy (Fakhfakh *et al.*, 2004). However, both switches and bias sources must also be designed using MOS transistors. The real version of the cell is shown in Fig. 3.

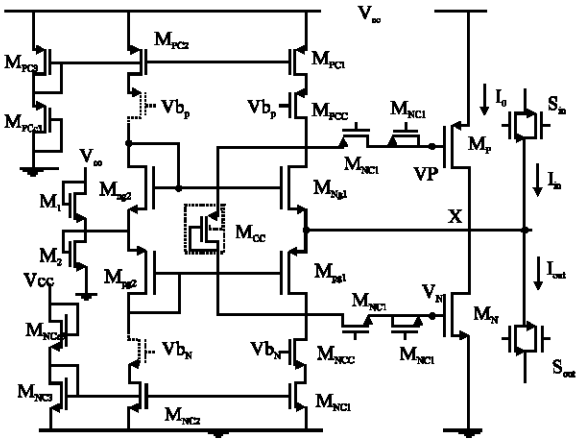

Fig. 3: Real Grounded Gate class AB memory cell

Bias current sources: Let β the transconductance parameter of both NMOS and PMOS memory transistors, V_{TN} and V_{TP} the threshold voltages of these transistors, V_{CC} the power supply voltage, V_{bN} and V_{bP} the bias voltage sources of the current source cascode transistors. Since the input current I_{in} varies between $(-4*I_0)$ and $(4*I_0)$, a constraint is imposed to the M_N gate transistor voltage V_N so that a minimum and a maximum values must be insured in order to guarantee saturation of M_{NC1} and M_{NCC} transistors (idem for V_P tension constraint and saturation of M_{PC1} and M_{PCC} transistors). For this purpose, we prove that expressions (2) and (3) have to be satisfied:

$$2\sqrt{\frac{2I_g}{\beta}} + V_{TN} \le V_{bN} \le V_N + V_{TN} \tag{2}$$

$$V_P - |V_{TP}| \le V_{bP} \le V_{DD} - |V_{TP}| - 2\sqrt{\frac{2I_g}{\beta}} \tag{3}$$

It is also important to notice that these current sources must be cascoded in order to minimize output equivalent conductance and minimize time response. However, only simple cascode configurations can be adopted to make these bias sources. Indeed, using regulated cascode configurations needs a minimal tension V_N equal to $V_{TNg} + \sqrt{\frac{2I_g}{\beta_g}} + \sqrt{\frac{2I_0}{\beta_{MNC1}}}$ in order to insure saturation of transistors forming this current source.

$$\delta V_{MAX} = \frac{\pm 4 I_0}{2\sqrt{2I_0\beta}} \tag{4}$$

$$V_{N0} = \frac{1}{2}\left(V_{CC} + V_{TN} - |V_{TP}| - V_c\right) \tag{5}$$

$$V_{P0} = \frac{1}{2}\left(V_{CC} + V_{TN} - |V_{TP}| + V_c\right) \tag{6}$$

$$I_0 = \frac{\beta}{8}(V_{CC} - V_{TN} - |V_{TP}| - V_c)^2 \tag{7}$$

Where, δV_{MAX} is the maximum voltage swing of input-output node voltage, V_{P0} and V_{N0} are quiescent tensions of respective memory transistors.

From expressions (4,…,7) (Oliaei *et al*., 1997) we can prove that minimal NMOS and PMOS maximal memory transistor voltages can be expressed as follows:

$$V_{N0min} = 2V_{TN} \tag{8}$$

$$V_{P0MAX} = Vcc - 2|V_{TP}| \tag{9}$$

As a conclusion, regulated cascode configurations can not be adopted to bias class AB grounded gate memory cells. Since simple cascode configurations need only a minimum voltage equal to $\sqrt{\frac{2I_0}{\beta_M}} + \sqrt{\frac{2I_0}{\beta_{Tcas}}}$ to saturate its transistors, they can safely be used to bias the considered SI cell.

Finally, from expressions (2) and (3) we conclude that a constraint will be applied to the size M_{NC1}, M_{NC2}, M_{NC3}, M_{NCC}, M_{PC1}, M_{PC2}, M_{PC3} and M_{PCC} transistors. Expressions (10) and (11) illustrate these constraints:

$$\frac{W_{NC}}{L_{NC}} \ge \frac{1}{K_N}\left[\frac{2I_g}{\left(\frac{2n-1}{2}V_{TN}\right)^2}\right] \tag{10}$$

$$\frac{W_{PC}}{L_{PC}} \ge \frac{2I_g}{K_P\left[\frac{V_{CC}\left(1-\frac{1}{n}\right) + V_{TP}\left(1-\frac{2}{n}\right)}{2}\right]^2} \tag{11}$$

Where, n is an added security coefficient which role is to restrict V_{TP} and V_{TN} ranges in order to optimize them and insure transistors saturations.

Bias voltage sources: Floating voltage source V_C insures both biasing and a constant voltage difference between both NMOS and PMOS gate voltages. We prove (Fakhfakh *et al*., 2004) that the optimal value of V_C is equal to 1.31 V. This voltage source will be realized using an isolated diode connected PMOS transistor (Oliaei *et al*., 1997).

The reference voltage source V_{ref} is useful to stabilize input output node voltage variation during switching. We prove that its optimal value is equal to $V_{CC}/2$ (Fakhfakh *et al*., 2004; Loulou *et al*., 2003). It is designed with a voltage divider formed by transistors M_1 and M_2.

Switches: Knowing that at the restitution phase, the cell is always connected to a similar one, the equivalent schema of the consequent circuit can be represented as follows:

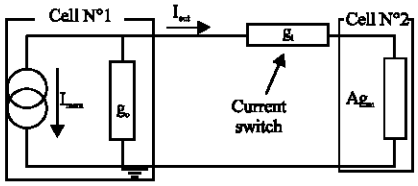

Fig. 4: Equivalent small signals at the restitution phase

where, g_i is the switch current equivalent conductance, $A.g_m$ and g_0 are the cell's input transconductance and output conductance. I_{mem} is the memorized current. And $A = \frac{g_{mNg} + g_{mPg}}{g_{0Ng} + g_{0Pg}}$ g_{mNg}, g_{mPg}, g_{0Ng} and g_{0Pg} are conductances and transconductances of grounded gate NMOS and PMOS transistors, respectively.

So, from Fig. 4 we prove that:

$$\frac{I_{out}}{I_{in}} = -\frac{\frac{g_m g_i}{g_m g_i + g_0(g_m + g_i)}}{\left(1 + \frac{g_0}{Ag_m} + \frac{g_0 V_{x0}}{I_0}\right)} \quad (12)$$

V_{x0} is the x input output voltage.

Consequently current switches have to be chosen in such a way that their equivalent conductance can be neglected when compared to the cell's input transconductance, otherwise accuracy and time response of the cell will be affected.

RESULTS

The optimization program developed in C++, allows us to have optimal values of all transistors forming the studied cell. Besides, it is able to give voltage ranges of bias cascode transistors and geometric dimensions of switches. The so obtained optimally sized cell was simulated with SPECTRE software; obtained results are related here after:

At Fig. 5, is illustrated the variation of errors between I_{in} and I_{out}, with respect to time response for several values of current switch width W. So a compromise between time response and precision must be taken into consideration

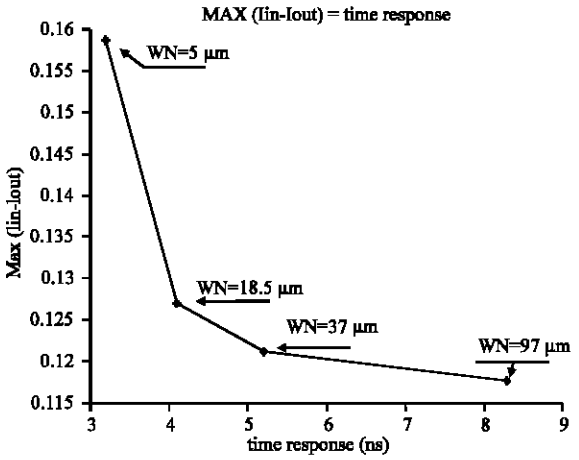

Fig. 5: time_response = f(current switch width). for L = 0.35 µm

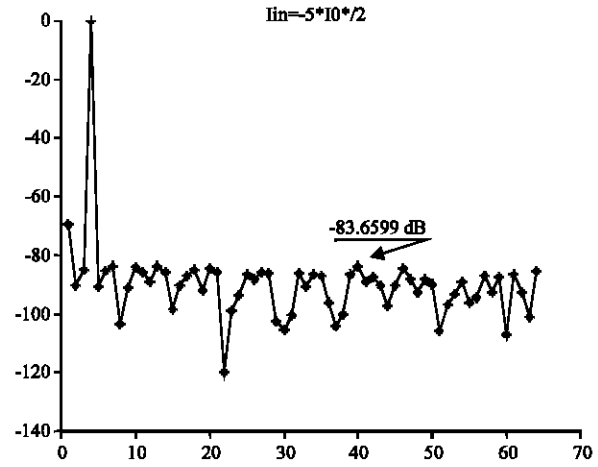

Fig. 6: Output power spectrum of the cell (I_{in}=2.5*I_0)

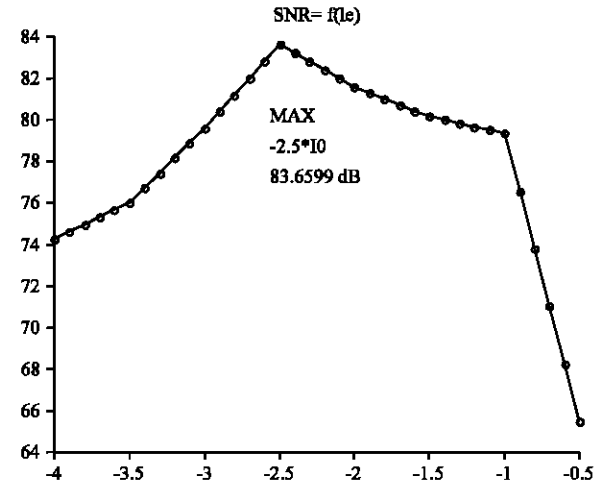

Fig. 7: SNR = f(Iin/I_0)

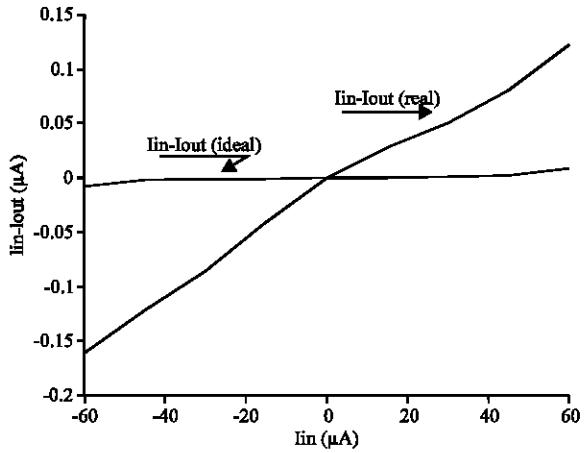

Fig. 8: I_{out} = f(I_{in}): ideal and real cell

Table 1: Simulation conditions

Technology	AMS CMOS 0.35 μm	NMOS memory transistor	57.85/39.95 μm
Power supply voltage (V_{cc})	Single 3.3 V	PMOS memory transistor	95.35/24.25 μm
Floating voltage source (V_c)	1.31 V	NMOS Conveyor transistors	3.9/1.65 μm
Bias current (I_0)	50.63 μA	PMOS Conveyor transistors	6.54/1 μm
Translinear loop bias current	14.25 μA	NMOS cascode transistor	5.8/0.6 μm
Input signal frequency	23.44 kHz	PMOS cascode transistor	9.6/0.35 μm
Sampling frequency	1 MHz		

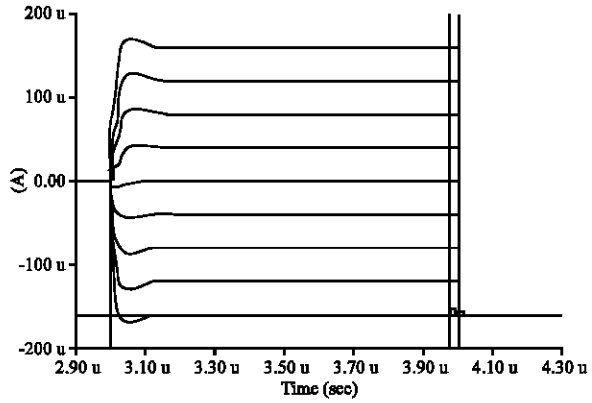

Fig. 9: The cell's output current

when sizing current switches. At Fig. 6 and 7, shown, respectively maximal obtained SNR and variation of with respect to input current ($I_{in}=n*I_0$, $n \in [-4,0]$), maximum obtained SNR is reached when $I_{in}=2.5*I_0$.

Figure 8 shows a comparison between errors ($I_{in}-I_{out}$) for both a class AB grounded gate ideal memory cell (ideal switches and ideal bias sources: Fig. 1) and for a real cell (all components are designed with MOS transistors: Fig. 3).

At Fig. 9 is shown real cell output current. Complementarity between NMOS and PMOS sub-circuits can be clearly seen.

Finally, we give simulation conditions; transistor sizes and bias sources values at Table 1.

CONCLUSIONS

This presented an algorithm driven methodology to optimize SI memory cells. Owing to this meta-heuristic a fully optimized class AB grounded gate memory cell is also depicted. We particularly put the stress on optimally sizing voltage and current switches and on designing both bias voltage and current transistors.

The meta-heuristic and all constraints on each transistor forming the cell were mathematically modelled and developed in C++. Thus this program allowed us to reach high performances in terms of accuracy, SNR and speed for the real cell fully designed by use of MOS transistors.

The obtained results were proved by spice and cadence simulations. With use of 0.35 μm CMOS process, the treated cell reaches a dynamic range more than 83.6 dB. Also this cell reaches less than 3.5 ns as settling time. The proposed optimized cell will be used for designing radio frequency applications, such as switched current sigma-delta converters and programmable filters.

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