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Bus Transactions in Microprocessor-Based Systems Using the Extended Physical Addressing

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Abstract: This research describes the Extended Physical Addressing bus transactions between the microprocessor-based systems and the external peripherals. This addressing technique, based on the use of software/hardware systems and reduced physical addresses, enlarges the interfacing capacity of the microprocessor-based systems and improves the speed of data exchange. The input of our system hardware part will be connected to the system bus. The output, which is a new bus, will be connected to an external device. To accomplish the bus transactions, the hardware part realizes a conversion of system bus data into new bus addresses. Furthermore, the software part ensures the transfer, with distinct addresses, of the simple data and the data that is intended to be converted. The use of this system with two system addresses and N bit data bus gives a new bus with N bit data bus and 2^N physical addressing capacity.

Key words: Interfacing, bus transactions, software/hardware systems, microprocessor-based systems, extended physical addressing

INTRODUCTION

The I/O transactions are generally handled in the form of bytes, words, or double words for the most recent processors (El-Rewini and Abd-El-Barr, 2005). The physical communication between microprocessor-based systems and an external peripheral is ensured by enabling the address decoder as soon as the address of this latter peripheral is available on the system bus (Berger, 2005). Figure 1 presents the peripherals interfacing bloc diagram. This process explains why the installation of expansion cards sometimes causes conflict problems: it is possible that two cards can be assigned the same field of addressing or have overlapping fields (Buchanan, 2000).

The Extended Physical Addressing is an interfacing system which is aimed to reduce the use of physical addresses in microprocessor-based systems. Furthermore, it will improve the data exchange speed. The proposed system combines a software/hardware solution to obtain the above objectives. This solution consists in creating a new bus, made up of a data bus, an address bus and a control bus.

The suggested architecture is composed of both hardware and software parts. The first is made up of a new bus and an interface between the system bus and the new bus. The software part ensures the communication between the microprocessor-based system and our interface.

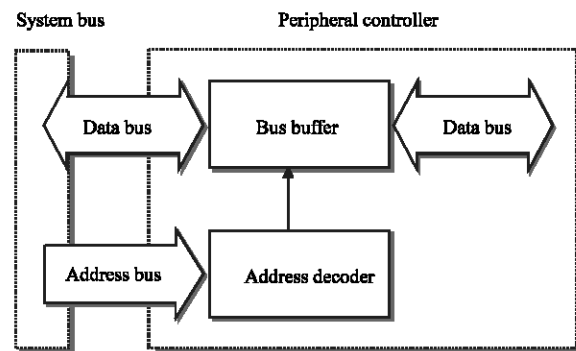


Fig. 1: Peripherals interfacing bloc diagram

A preliminary version of this study was published by Maamoun and Zerari (2001), the programmable logic implementation by Maamoun *et al.* (2006) and the bus transactions are presented in this study. The main technique of this interfacing system has been applied for the implementations of video signal generation as suggested by Maamoun *et al.* (2004a and c).

EXTENDED PHYSICAL ADDRESSING

The Extended Physical Addressing is based on a mixed software/hardware architecture, which increases the hardware addressing capacity of the computers and the microprocessor-based systems. In this system, we have

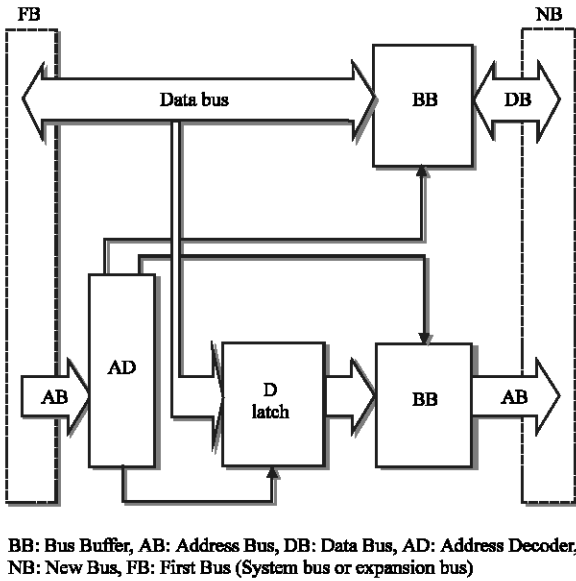


Fig. 2: Extended physical addressing bloc diagram

used some addresses of the microprocessor-based system addressing area to cover a significant external memory capacity.

The Extended Physical Addressing system represents the starting point of the Fast Physical Addressing system (Maamoun *et al.*, 2002), the Accelerated Physical Addressing system (Maamoun *et al.*, 2003) and the Advanced Physical Addressing system (Maamoun *et al.*, 2004b).

Hardware part: The hardware part of this system is made up of a new bus and an interface. This latter is intended for use as an interconnect between the system bus (or I/O expansion bus) and the device that will be addressed by this technique.

The input of the interface of this system will be connected to the microprocessor-based system bus. The output will be connected to an external device, which contains the new data and addresses bus. Figure 2 shows the basic bloc diagram of the hardware part of the Extended Physical Addressing.

In our interfacing, the data bus ensures the transfer of the simple data and the transfer of the data that is intended to be converted into addresses (for the new bus). The software part of our system establishes the transmission of the two types of data in two steps and on distinct addresses, where the address decoder of the Extended Physical Addressing hardware enables the separation between the two data types.

Software part and I/O transactions: This technique can be done in two phases. The software ensures the

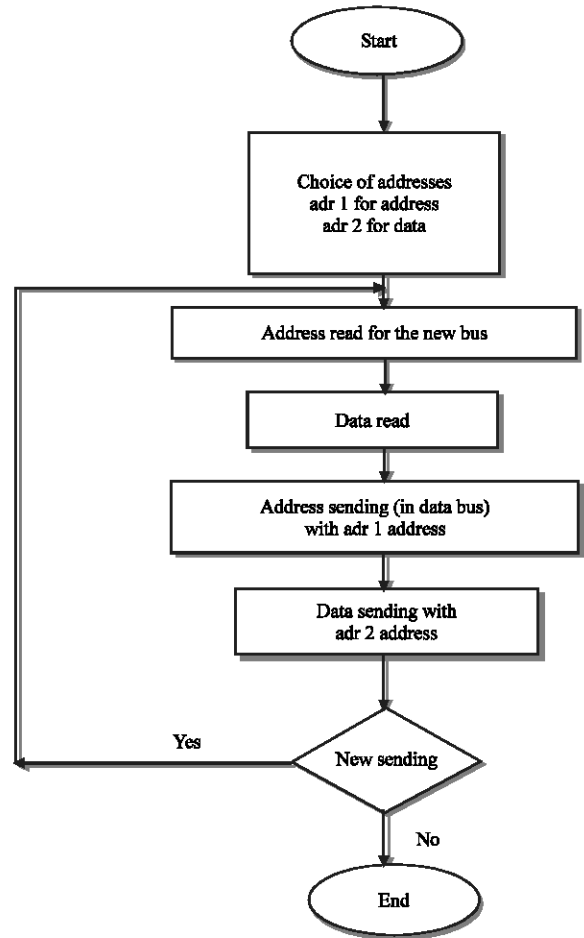


Fig. 3: The extended physical addressing software flow chart

presence of data intended to be present on the new bus as addresses (Fig. 3) the decoder ensures the activation, with adr1, of the D LATCH circuit to record these data and disables the two bus buffers until the second phase. The addresses and data lines of the new bus will be at the high impedance state. In the second phase, the software ensures the presence of the data. Whereas, the two bus buffers are activated by the address decoder with adr2.

The data values on the new bus are identical to the system bus data of the second step (data 1) and the address values are identical to the data of the system bus first step (data 2). Figure 4 presents the basic Extended Physical Addressing I/O transactions. We use two physical addresses, the first one the data/address conversion task and the other for the data transfer.

The addressing capacity of the suggested system is directly related to the data bus size of the system bus or the used expansion bus. The control and the address lines of the first bus are used for the addresses decoding in the

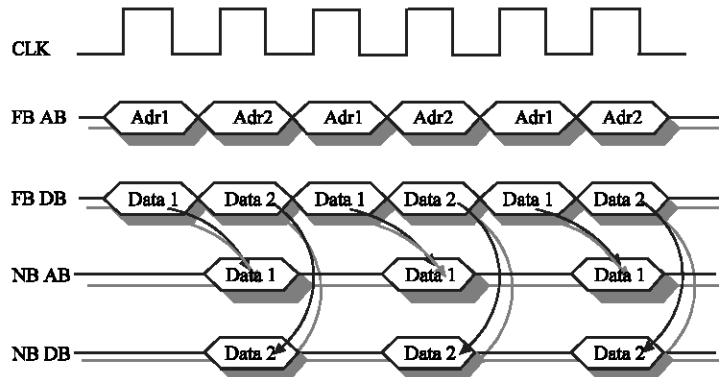


Fig. 4: The basic extended physical addressing I/O transactions

hardware part of our system. The control lines of the new bus will be designed according to two methods. Firstly, the control lines of the system bus will be adapted to produce the new control lines. Secondly, the new control lines will be designed with combinatory logic and according to our specified application.

RESULTS

The proposed architecture enlarges the physical addressing capacity of the microprocessor-based systems. Furthermore, this solution resolves the conflicts problems by the capability of using reduced system physical addresses with an adaptable address decoder.

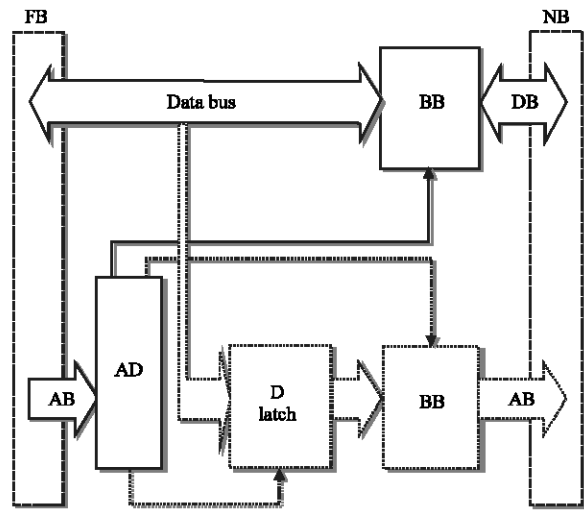
The use of two addresses on an operating system bus with N bit data bus and operating at frequency F gives a new bus with F/2 working frequency, N bit data bus and 2^N physical addressing capacity. Table 1 presents the basic characteristics of the Extended Physical Addressing. If the Extended Physical Addressing system is applied to a bus of 133 MHz and a 32 bit data, the new bus will operate at a maximum frequency of 66.5 MHz, a 32 bit data bus and a 4 Giga addressing capacity.

COMPATIBILITY

The Extended Physical Addressing System is conceived to be compatible with devices working with a parallel communication system (Leibson, 1989) which operates with a data and a control bus (Oklobdzija, 2002). We have seen that the data transfer in our system ensures the activation of the unidirectional buffers of addresses and the bi-directional buffers of the data. This means that the data transfer can be accomplished without sending data which are intended to be converted into addresses (Fig. 5).

Table 1: Extended physical addressing characteristics

System bus data size	No. of used physical address	System bus frequency	New bus data size	New physical addressing capacity	New bus frequency
8 bits	02	F	8 bits	256	F/2
16 bits	02	F	16 bits	64K	F/2
32 bits	02	F	32 bits	4G	F/2



BB: Bus Buffer, AB: Address Bus, DB: Data Bus, AD: Address Decoder, NB: New Bus, FB: First Bus (System bus or expansion bus)

Fig. 5: The extended physical addressing parallel compatibility

We notify that the setting of the new bus address lines in the high impedance state does not affect the data transfer of the new bus.

CONCLUSION

The microprocessor-based system interfacing, in many applications, causes address conflicts or an addressing limitation. In this study, we have presented

the bus transaction of the Extended Physical Addressing. This proposed solution is based on the use of a mixed software/hardware system. This new system presents a solution for improving the physical addressing capacity of the microprocessor-based systems, which is independent of the addresses bus of the system bus. The Hardware part is exposed at the beginning. Thereafter we presented Software part, the I/O transactions and the compatibility with the simple parallel systems.

The above developed study has been applied on the implementation of some prototype cards operating on PC and compatible and has shown its efficiency in terms of addressing capacity and conflict problems elimination. Currently, we are investigating the option of adapting and implementing this system in PCI and PCI-Express bus using CPLD (Xilinx, 2006) and FPGA devices (Xilinx, 2004).

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