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Low Cost Quantum Realization of Reversible Multiplier Circuit

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Abstract: Irreversible logic circuits dissipate heat for every bit of information that is lost. Information is lost when the input vector can not be uniquely recovered from the output vector. Theoretically reversible logic dissipates zero power since the input vector of reversible circuit can be uniquely recovered from the output vector. Reversible computation has applications in digital signal processing, low power CMOS design, DNA computing and quantum computing. This study presents an overview of the well-known reversible gates and discuss about their quantum implementation. A new PFAG gate and its quantum implementation are presented. Finally, this study proposes a novel low cost quantum realization of reversible multiplier circuit and compares its superiority with the existing counterparts.

Key words: Reversible logic gates, reversible logic circuits, garbage outputs, quantum cost, reversible multiplier circuit

INTRODUCTION

Power dissipation is a very important factor in VLSI design. As we pack more and more logic elements into smaller and smaller volumes and clock them higher and higher frequencies, we dissipate more and more heat. This creates at least three problems:

- Energy costs money
- Portable systems exhaust their batteries
- Systems overheat

When a computational system erases a bit of information, it must dissipate $\ln 2 \times kT$ energy, where k is Boltzmann's constant and T is the absolute temperature (Landauer, 1961; Keyes and Landauer, 1970). Today's computers erase a bit of information every time they perform a logic operation. These logic operations are therefore called irreversible. This erasure is done very inefficiently and much more than kT is dissipated for each bit erased.

If the revolution is continued in computer hardware performance we must continue to reduce the energy dissipated by each logic operation. Today, because we are dissipating much more than kT , we can do this by improving conventional methods, i.e., by improving the efficiency with which we erase information. An alternative is to use logic operations that do not erase information. These are called reversible logic operations and according to Bennet (1973) zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design.

Synthesis of reversible logic circuits differs significantly from classical logic circuits in many ways. In reversible circuits there should be no fan-out, that is, each output will be used only once, for each input pattern there should be a unique output pattern and the resulting circuit must be acyclic (Perkowski *et al.*, 2001). Any reversible circuit realizes only the function that is reversible. Garbage is the number of outputs added to make an n -input k -output function, i.e., (n, k) function, reversible. The word constant-input are the inputs added to an (n, k) function to make it reversible. An algorithm is given by Islam (2007) to make an (n, k) function reversible. Any efficient realization of reversible network should minimize the number of reversible gates, garbage outputs and constant inputs. The gate complexity should be kept as low as possible. Finally, the quantum realization cost of it in any nanotechnology should be optimized.

Full-adder is the fundamental building block of many computational units. The compatible adder implementation in quantum technology is must. Any reversible gate that can work singly as a reversible full-adder unit will be beneficial to build other complex circuits in nanotechnology. This study presents a new reversible gate PFAG that can work singly as a reversible full-adder unit. The quantum realization of this reversible full-adder gate is also given. Then a low cost quantum realization of reversible multiplier circuit using PFAG and Peres gate (Peres, 1985) is presented. The objective of this study is that the proposed reversible multiplier circuit is superior to the existing designs in terms of gate count, garbage outputs, constant-inputs and hardware complexity. Moreover, the quantum realization of this multiplier circuit is readily available for use.

MATERIALS AND METHODS

Reversible gate: A gate or a circuit is called reversible if there is a one-to-one correspondence between its input and output assignments. Any reversible circuit realizes only the function that is reversible. There exist many reversible gates in the literature. Among them Feynman gate, FG (Feynman, 1985), Peres gate, PG (Peres, 1985), Toffoli gate, TG (Toffoli, 1980), Fredkin gate, FRG (Fredkin and Toffoli, 1982) and Khan gate, NG (Khan, 2002) are mostly common. Recently TSG gate, TSG (Thapliyal and Srinivas, 2005, 2006), MKG gate (Shams *et al.*, 2008) and HNG gate HNG (Haghparast *et al.*, 2008) has been proposed (Fig. 1-8).

The quantum realizations of all these gates are not available in the literature. Only FG, PG, TG and FRG have been realized in nanotechnology (Perkowski *et al.*, 2003).

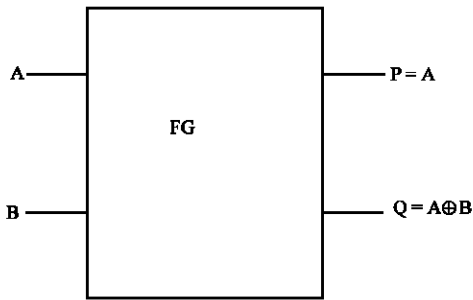


Fig. 1: Feynman gate (Islam and Islam, 2005)

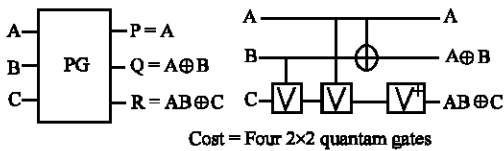


Fig. 2: Peres gate and its quantum realization (Islam and Islam, 2005)

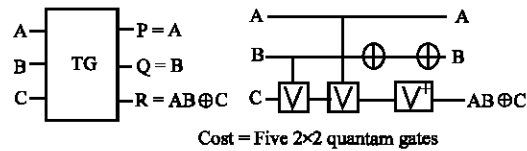


Fig. 3: Toffoli gate (Islam and Islam, 2005)

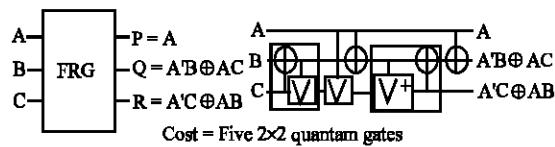


Fig. 4: Fredkin gate (Islam and Islam, 2005)

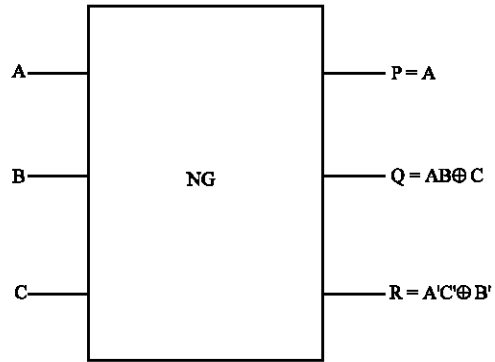


Fig. 5: Khan gate, NG (Khan, 2002)

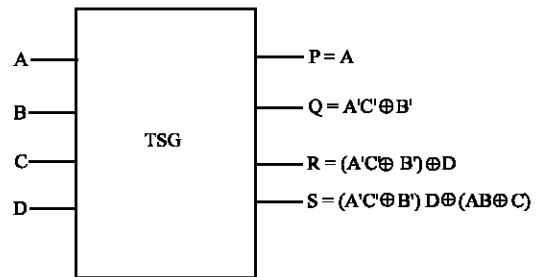


Fig. 6: TSG gate (Thapliyal and Srinivas, 2005, 2006)

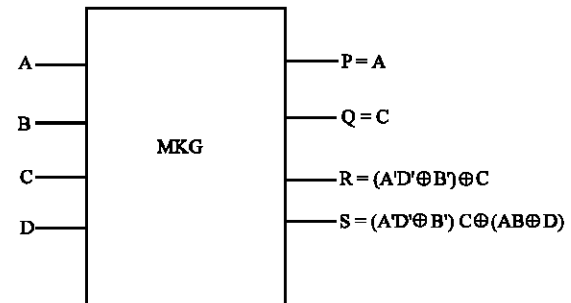


Fig. 7: MKG gate (Shams *et al.*, 2008)

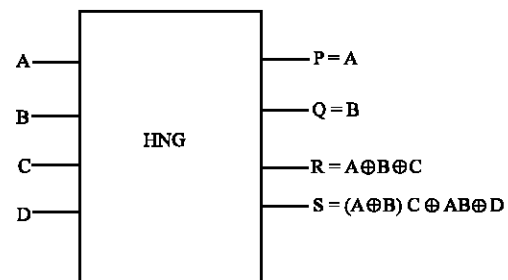


Fig. 8: HNG gate (Haghparast *et al.*, 2008)

The detailed cost of a reversible gate depends on any particular realization of quantum logic. Generally, the cost is calculated as a total sum of 2×2 quantum primitives used. The cost of TG is exactly the same as the cost of FRG and is 5. According to Perkowski *et al.* (2003), the only cheapest quantum realization of a complete (universal) reversible gate is PG and its cost is 4.

The quantum implementation of NG, TSG, MKG and HNG are not available in the literature and their cost is unknown at present.

Reversible full-adder circuit: Full-adder is the fundamental building block of many computational units. The anticipated paradigm shift logic compatible with optical and quantum requires compatible adder implementations. Minimization of reversible full-adder circuits and their implementation issues has been discussed by Khan (2002), Islam *et al.* (2004) and Islam and Islam (2005). Islam *et al.* (2004) and Islam and Islam (2005) showed that a full adder circuit can be realized with at least two garbage outputs and one constant-input. They have realized a full-adder circuit with only two Peres gates and which is optimum in terms of gate count, garbage outputs, constant-input and efficient in terms of quantum cost and that can be technologically mapped.

Reversible full-adder unit: Full-adder circuit that can work singly as a reversible full-adder unit will be beneficial to the quantum realization of other complex systems. There are two reversible full-adder units in the literature, MKG (Shams *et al.*, 2008) and HNG (Haghparast *et al.*, 2008). Though their hardware complexity is known, their quantum realization is not provided by Shams *et al.* (2008) and Haghparast *et al.* (2008).

This study presents a new reversible full-adder unit known as Peres Full-Adder Gate, shortly PFAG, shown in Fig. 9, where each output is annotated with the corresponding logic expression and its quantum implementation is shown in Fig. 10. The corresponding truth table of the PFAG gate is shown in Table 1. For more information about reversible logic gates is

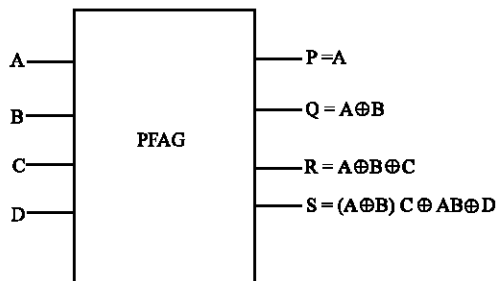


Fig. 9: Reversible PFAG gate

presented by Feynman (1985), Peres (1985), Toffoli (1980), Fredkin and Toffoli (1982), Khan (2002), Thapliyal and Srinivas (2005, 2006), Shams *et al.* (2008), Haghparast *et al.* (2008) and Babu *et al.* (2007).

It can be observed easily that PFAG is reversible, i.e., there is a one-to-one correspondence between its input and output assignments and the input vector can be uniquely recovered from its output vector. Like MKG and HNG, PFAG can work singly as a reversible full adder unit, as shown in Fig. 11. If $I_v = (A, B, C_{in}, 0)$, then the output vector becomes: $O_v = (P = A, Q = A \oplus B, R = \text{Sum}, S = C_{out})$. The proposed reversible full adder circuit uses only one reversible logic gate. It produces only two garbage outputs. It requires only one constant input and it needs only one clock cycle to perform the operations. It can be proved that the proposed reversible full adder is better than the reversible full adder circuits proposed by Thapliyal and Srinivas (2005, 2006), Shams *et al.* (2008) and Haghparast *et al.* (2008) in terms of hardware complexity.

Table 1: Truth table of proposed reversible PFAG gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

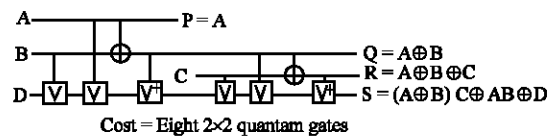


Fig. 10: Quantum realization of PFAG gate

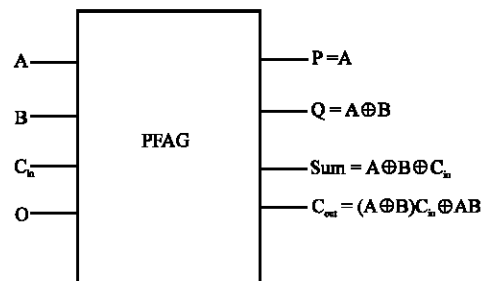


Fig. 11: Reversible PFAG gate as a reversible full adder

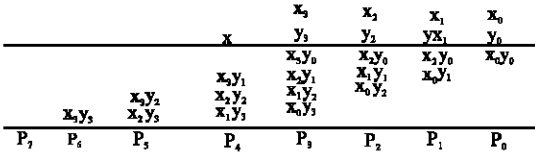


Fig. 12: Partial products in a 4×4 multiplication

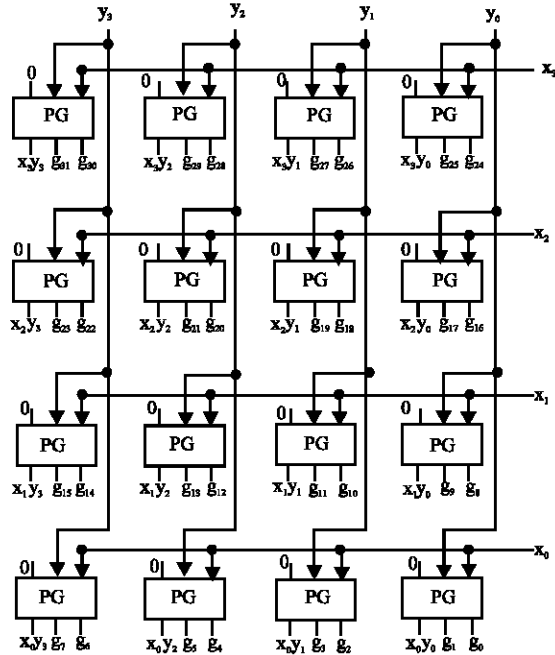


Fig. 13: Reversible partial products generation circuits using Peres gates (Shams *et al.*, 2008)

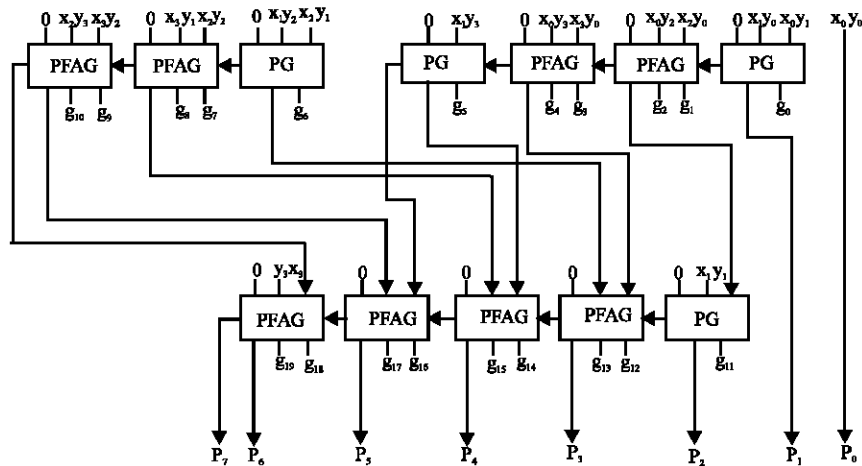


Fig. 14: Proposed 4×4 reversible multiplier circuit using PFAG gates and Peres gates

Let:

α = A two input EXOR gate calculation

β = A two input AND gate calculation

δ = A NOT gate calculation

T = Total logical calculation

For Thapliyal and Srinivas (2005, 2006), $T = 6\alpha + 3\beta + 3\delta$, for Shams *et al.* (2008), $T = 5\alpha + 3\beta + 3\delta$, for (Haghparsat *et al.*, 2008), $T = 5\alpha + 2\beta$ and for PFAG $T = 5\alpha + 2\beta$ (when D is set to zero it requires five two input EXOR gate calculations). Thus, the proposed reversible full adder is better than the reversible full adder circuits in Thapliyal and Srinivas (2005, 2006), Shams *et al.* (2008) and Haghparsat *et al.* (2008) in terms of hardware complexity. In addition of it, its second output can be used as the half adder sum output. This can be advantageous for the adaptation of minimized ESOP functions in reversible cascades (Babu *et al.*, 2007). Not only that, quantum cost of this gate in NMR technology (Perkowski *et al.*, 2003) is 8 which is the lowest as mentioned by Islam and Islam (2005). We used PFAG gates to construct low cost reversible multiplier circuit.

Reversible multiplier circuit using PFAG gates: The operation of the 4×4 multiplier is depicted in Fig. 12. It consists of 16 partial product bits of the form $x_i y_j$.

A reversible 4×4 multiplier circuit has two parts. First, the partial products are generated in parallel using Peres gates (Shams *et al.*, 2008) and shown in Fig. 13. Then, the addition is performed as shown in Fig. 14. The basic cell for such a multiplier is a Full Adder (FA) accepting three bits and one constant input. We use

PFAG gates as reversible full adder which is depicted in Fig. 11. The proposed reversible multiplier circuit uses eight reversible PFAG full adders. In addition, it needs four reversible half adders. It is possible to use PFAG gate as half adder as mentioned earlier in this study, but we use Peres gate as reversible half adder because it has less hardware complexity and quantum cost compared to the PFAG gate (quantum cost of Peres gate is 4 whereas for PFAG it is 8).

RESULTS AND DISCUSSION

Evaluation of the proposed reversible multiplier circuit:

The proposed reversible multiplier circuit is more efficient than the existing circuits presented by Thapliyal and Srinivas (2006), Shams *et al.* (2008) and Haghparast *et al.* (2008). Evaluation of the proposed circuit can be comprehended easily with the help of the comparative results in Table 2.

The only difference between partial products generation block in our design with the existing designs by Thapliyal and Srinivas (2006) is the use of Peres gates instead of Fredkin gates. This structure is proposed by Shams *et al.* (2008) and Haghparast *et al.* (2008). We use it because the Peres gates have less logical calculation and less quantum cost than the Fredkin gates.

Hardware complexity: One of the main factors of a circuit is its hardware complexity. It can be proved that the proposed circuit is better than the existing approaches in terms of hardware complexity. For Thapliyal and Srinivas (2006) the total logical calculation is: $T = 110\alpha + 103\beta + 71\delta$, for Shams *et al.* (2008) the total logical calculation is: $T = 92\alpha + 52\beta + 36\delta$, for Haghparast *et al.* (2008): $T = 80\alpha + 36\beta$ and for present proposed reversible multiplier circuit, the total logical calculation is: $T = 80\alpha + 36\beta$, which is equal to Haghparast *et al.* (2008). Therefore, the hardware complexity of the proposed reversible multiplier circuit is less than Thapliyal and Srinivas (2006) and Shams *et al.* (2008) and equal to Haghparast *et al.* (2008).

Garbage outputs: Garbage output refers to the output of the reversible gate that is not used as a primary output or as input to other gates (Islam and Islam, 2005). One of the

other major constraints in designing a reversible logic circuit is to lessen number of garbage outputs. Present proposed reversible multiplier circuit produces 52 garbage outputs which are equal to the design in Haghparast *et al.* (2008) and minimum, but the design by Shams *et al.* (2008) produces 56 garbage outputs and the design in Thapliyal and Srinivas (2006) produced 58 garbage outputs. So, it can be stated that our design approach is better than all the existing counterparts in terms of number of garbage outputs.

Constant inputs: Number of constant inputs is one of the other main factors in designing a reversible logic circuit. The input that is added to an $n \times k$ function to make it reversible is called constant input (Islam and Islam, 2005). The proposed reversible multiplier circuit requires 28 constant inputs which are equal to the design in Haghparast *et al.* (2008), but the design by Shams *et al.* (2008) requires 32 constant inputs and the design in Thapliyal and Srinivas (2006) requires 34 constant inputs. So, we can state that our design approach is better than all the existing designs in terms of number of constant inputs.

Gate count: Comparing our proposed reversible multiplier circuit with the existing circuits, it is found that the proposed design approach requires 28 reversible logic gates which are equal to Shams *et al.* (2008) and Haghparast *et al.* (2008) but the design by Thapliyal and Srinivas (2006) requires 29 reversible gates. So, the proposed circuit is better than Thapliyal and Srinivas (2006) circuits in terms of number of reversible logic gates, which is one of the other main factors in reversible circuit design (Islam and Islam, 2005).

Quantum costs: The detailed cost of a reversible gate depends on any particular realization of quantum logic. Several reversible gates have been realized in quantum technology. Among which are PG, TG and FRG. The only cheapest universal reversible gate is PG whose quantum cost is less than any other gates in nanotechnology (Perkowski *et al.*, 2003). A reversible full adder unit i.e., PFAG, has been presented using this gate. The quantum cost of this gate is 8 and it is lowest as mentioned by Islam and Islam (2005). The proposed reversible

Table 2: Comparative experimental result of different reversible multiplier circuits

References	No. of gates	No. of garbage outputs	No. of constant inputs	Total logical calculation	Quantum cost
Present Study	20PG+8PFAG =28	52	28	$80\alpha + 36\beta$	144
Haghparast <i>et al.</i> (2008)	20PG+8HNG =28	52	28	$80\alpha + 36\beta$	Unknown
Shams <i>et al.</i> (2008)	16PG+12MKG =28	56	32	$92\alpha + 52\beta + 36\delta$	Unknown
Thapliyal and Srinivas (2006)	16FRG+13TSG =29	58	34	$110\alpha + 103\beta + 71\delta$	Unknown

multiplier circuit has been designed using PFAG gates and Peres gates. The total quantum cost of our design is 144. The existing designs of Thapliyal and Srinivas (2006), Shams *et al.* (2008) and Haghparast *et al.* (2008) have no quantum realization and the realization costs of these designs in any particular technology are unknown.

From the above discussion we can conclude that the proposed reversible multiplier circuit is better than all the existing counterparts. And one of the remarkable features of this circuit is that its quantum realization is given in NMR technology (Perkowski *et al.*, 2003).

CONCLUSION

This study presents a new reversible logic gate PFAG and presents its hardware complexity and quantum implementation. This gate can work singly as a full adder unit and it is efficient in terms of gate count, garbage outputs, constant input and quantum costs. A novel 4×4 reversible multiplier circuit using PFAG gates and Peres gates has also been presented. It has been demonstrated that the proposed 4×4 multiplier circuit is efficient in terms of hardware complexity, gate count, garbage outputs and constant inputs. The remarkable feature of the proposed multiplier circuit is that its quantum realization is readily available for use in NMR technology.

REFERENCES

Babu, H., M. Hasan, M.S. Islam, M.R. Islam, M.R. Karim and A.A. Mahmud, 2007. Generalization of reversible gates to $k \times k$ gates and adaptation of minimized ESOP to reversible cascades. *Dhaka Univ. J. Sci.*, 55: 29-33.

Bennet, C.H., 1973. Logical reversibility of computation. *IBM J. Res. Dev.*, 17: 525-532.

Feynman, R., 1985. Quantum mechanical computers. *Optics News*, 11: 11-20.

Fredkin, E. and T. Toffoli, 1982. Conservative logic. *Int. J. Theor. Phys.*, 21: 219-253.

Haghparast, M., S.J. Jassbi, K. Navi and O. Hashemipour, 2008. Design of a novel reversible multiplier circuit using HNG gate in nanotechnology. *World Applied Sci. J.*, 3: 974-978.

Islam, M.S., M.R. Islam, M.R. Karim, A.A. Mahmud and H.M. Hasan Babu, 2004. Minimization of adder circuits and variable block carry skip logic using reversible gates. *Proceedings of the 7th International Conference on Computer and Information Technology*, December 26-28, Dhaka, Bangladesh, pp: 378-383.

Islam, M.S. and M.R. Islam, 2005. Minimization of reversible adder circuits. *Asian J. Inform. Technol.*, 4: 1146-1151.

Islam, M.S., 2007. BSSSN: Bit string swapping sorting network for reversible logic synthesis. *IBAIS Univ. J. Comput. Sci.*, 1: 94-99.

Keyes, R.W. and R. Landauer, 1970. Minimal energy dissipation in logic. *IBM J. Res. Dev.*, 14: 152-157.

Khan, M.H.A., 2002. Design of full-adder with reversible gates. *Proceedings of the 5th International Conference on Computer and Information Technology*, (ICCIT'2002), Dhaka, Bangladesh, pp: 515-519.

Landauer, R., 1961. Irreversibility and heat generation in the computing process. *IBM J. Res. Dev.*, 5: 183-191.

Peres, A., 1985. Reversible logic and quantum computers. *Phys. Rev. A*, 32: 3266-3276.

Perkowski, M., A. Al-Rabadi, P. Kerntopf, A. Buller and M. Chrzanowska-Jeske *et al.*, 2001. A general decomposition for reversible logic. *Proceedings of RM 2001, (RM'2001)*, Starkville, pp: 119-138.

Perkowski, M. *et al.*, 2003. A hierarchical approach to computer-aided design of quantum circuits. *6th International Symposium on Representations Methodol. Future Computing Technology*, March 2003, Trier, Germany, pp: 201-209.

Shams, M., M. Haghparast and K. Navi, 2008. Novel reversible multiplier circuit in nanotechnology. *World Applied Sci. J.*, 3: 806-810.

Thapliyal, H. and M.B. Srinivas, 2005. Novel reversible TSG gate and its application for designing reversible carry look ahead adder and other adder architectures. *Proceedings of the 10th Asia-Pacific Computer Systems Architecture Conference*, LNCS., 3740, October 24-26, Springer-Verlag, Singapore, pp: 775-786.

Thapliyal, H. and M.B. Srinivas, 2006. Novel reversible multiplier architecture using reversible TSG gate. *IEEE International Conference on Computer Systems and Applications*, March 8, Dubai/Sharjah, UAE., pp: 100-103.

Toffoli, T., 1980. Reversible Computing. *Proceedings of the 7th Colloquium on Automata, Languages and Programming*, LNCS., 85, July 14-18, Springer-Verlag, London, UK., pp: 632-644.