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Overview of Radiation Hardening Techniques for IC Design

Fa-Xin Yu, Jia-Rui Liu, Zheng-Liang Huang, Hao Luo and Zhe-Ming Lu
School of Aeronautics and Astronautics, Zhejiang University, Hangzhou 310027, China

Abstract: With the development of astronautic techniques, the radiation effects on Integrated Circuits (ICs) have been cognized by people. Environments with high levels of ionizing radiation create special design challenges for ICs. To ensure the proper operation of such systems, manufacturers of integrated circuits and sensors intended for the military aerospace markets adopt various methods of radiation hardening. An overview of radiation hardening techniques for IC design is given in this study. First, seven major radiation damage sources, two fundamental damage mechanisms, five sorts of end-user effects and six types of single-event effects are introduced, followed by the brief introduction of radiation hardening techniques. Secondly, typical physical radiation hardening techniques are introduced. Thirdly, typical logical radiation hardening techniques are introduced. Fourthly, we propose our radiation hardening scheme for microwave power amplifier chip design. Here, a Radio-Frequency (RF) Power Amplifier (PA) is a sort of electronic amplifier employed to convert a low-power radio-frequency signal into a larger signal of significant power, typically for driving the antenna of a transmitter. Finally, we concluded the whole study.

Key words: Integrated circuits, radiation effects, radiation hardening techniques, power amplifier, RF power amplifier

INTRODUCTION

Environments with large amount of ionizing radiation create special design challenges for integrated circuits, typically for RF power amplifier chips (Barbara *et al*., 1990). A single charged particle can knock thousands of electrons loose, resulting in electronic noise and signal spikes. In the case of digital circuits, this can lead to results that are inaccurate or unintelligible. It is a particularly serious problem in designing artificial satellites, spacecraft, military aircraft, nuclear power stations and nuclear weapons. Typical sources of exposure of electronics to ionizing radiation are the Van Allen radiation belts for satellites, nuclear reactors in power plants for sensors and control circuits, residual radiation from isotopes in chip packaging materials, cosmic radiation for spacecraft and high-altitude aircraft and nuclear explosions for potentially all military and civilian electronics (Holmes-Siedle and Adams, 2002). Seven familiar sources are: (1) Cosmic rays (Gaisser, 1990). They consist of approximate 85% protons, 14% alpha particles and 1% heavy ions with X-ray radiation. Most effects result from particles with energies between 10^8 and 2×10^{10} eV. The atmosphere filters most of them, so they are mainly considered for spacecraft and high-altitude aircraft. (2) Solar particle events (Lantos and Fuller, 2003). They come from the sun and consist of a large flux of high-energy protons and heavy ions accompanied by X-ray radiation. (3) Van Allen radiation belts (Snyder, 1959). They include electrons and protons trapped in the geomagnetic field. Depending on the actual conditions of the sun and the magnetosphere, the particle flux in the regions farther from the Earth can vary wildly. They mainly affect satellites. (4) Secondary particles (Badhwara *et al*., 1995). They result from interaction of other kinds of radiation with structures around the electronic devices. (5) Nuclear reactors. They produce Gamma radiation and neutron radiation, which can affect sensor and control circuits in nuclear power plants. (6) Nuclear explosions. They produce a short and extremely intense surge through the entire spectrum of electromagnetic radiation, an electromagnetic pulse (EMP), neutron radiation and a flux of both primary and secondary charged particles. In case of a nuclear war they pose a potential concern for all civilian and military electronics. (7) Chip packaging materials (Baumann *et al*., 1995). They are a kind of insidious source of radiation that was found to cause soft errors in new DRAM chips in the 1970s. Traces of radioactive elements in the chip packaging will produce alpha particles, which discharge occasionally some of the capacitors used to store the DRAM data bits. These effects have been reduced today

Corresponding Author: Zhe-Ming Lu, Teaching Building 5, Yuquan Campus, Zhejiang University, 38 ZheDa Road, Hangzhou 310027, P. R. China Tel/Fax: +86-571-87951589

by using purer packaging materials and employing error-correcting codes to detect and often correct DRAM errors.

With the development of astronautic techniques, the radiation effects have been cognized by people. The research about the radiation effects on semiconductors has been carried out since 1960s. Later, the research about the radiation effects on electronic elements and circuits was carried out also. With regard to radiation effects on electronics, two fundamental damage mechanisms (Van Lint *et al*., 1980) can be described as follows. One is called lattice displacement. It is caused by neutrons, protons, alpha particles, heavy ions and very high energy gamma photons. They change the arrangement of the atoms in the crystal lattice, create lasting damages, increase the number of recombination centers, deplete the minority carriers and worsen the analog properties of the affected semiconductor junctions. This damage is especially important for bipolar transistors that depend on minority carriers in their base regions and increased losses caused by recombination will cause loss of the transistor gain. The other is called ionization effects. They are mainly caused by charged particles, including the ones with energy too low to cause lattice effects. They are usually transient, creating glitches and soft errors, but can lead to destruction of the device if they trigger other damage mechanisms. Gradual accumulation of holes in the oxide layer in MOSFET transistors results in performance degradation, up to device failure when the dose is high enough. The effects can vary wildly dependent on the type of radiation, total dose, the radiation flux, combination of types of radiation and even the kind of the device load, which makes thorough testing difficult and time-consuming and require a lot of test samples.

Based on above damage mechanisms, the resultant end-user radiation effects can be characterized into following five groups: (1) Neutron effects (Arimura, 1982). A neutron interacting with the semiconductor lattice will displace its atoms. This leads to an increase in the count of recombination centers and deep-level defects, a decrease in the lifetime of minority carriers, which influences bipolar devices more than CMOS ones. There is also the risk of induced radioactivity caused by neutron activation, which is a major source of noise in high energy astrophysics instruments. Induced radiation, together with residual radiation from impurities in materials, can introduce all sorts of single-event problems during the device's lifetime. GaAs LEDs are very sensitive to neutrons. The lattice damage affects the frequency of crystal oscillators. Kinetic energy effects of charged particles also belong to this category. (2)Total ionizing dose effects (Pease, 2003). It is the cumulative damage of the semiconductor lattice introduced by ionizing radiation over the exposition time. In CMOS devices, the radiation creates electron-hole pairs in the gate insulation layers, which introduce photocurrents during their recombination and the holes trapped in the lattice defects in the insulator create a persistent gate biasing and affect the transistors' threshold voltage, making the N-type MOSFET transistors easier and the P-type ones more difficult to switch on. The accumulated charge can be high enough to keep the transistors permanently open (or closed), leading to device failure. Crystal oscillators are somewhat sensitive to radiation dose, which alters their frequency, but the sensitivity can be greatly reduced by using swept quartz. (3) Transient dose effects (Meulenberg *et al*., 1988). It refers to the short-time high-intensity pulse of radiation, typically occurring during a nuclear explosion. The high radiation flux creates photocurrents in the entire body of the semiconductor, which makes transistors randomly open and alters logical states of flip-flops and memory cells. Permanent damage may occur if the pulse duration lasts too long or if the pulse causes junction damage or causes a latchup. Crystal oscillators may stop oscillating during the flash due to prompt photoconductivity induced in quartz. (4) System-Generated EMP effects (SGEMP) (Higgins *et al*., 1978). They are caused by the radiation flash traveling through the equipment, which causes local ionization and electric currents in the material of the chips, circuit boards, cables and cases. (5) Single-Event Effects (SEE) (Dodd, 2005). They mostly affect digital devices and the following paragraph gives an overview for SEE.

Among above effects, single-event effects (SEE), mostly affecting only digital devices, were not studied extensively until relatively recently. When a high-energy particle travels through a semiconductor, it leaves an ionized track behind. This ionization may introduce a highly localized effect similar to the transient dose one. SEE are important for electronics in satellites, aircraft and other both civilian and military aerospace applications. SEE can be classified into following 6 categories: (1) Single-Event Upsets (SEU) (Kuznetsov and Nymmik, 1996). They are state changes of memory or register bits caused by a single ion interacting with the chip. In some very sensitive devices, a single ion may introduce a Multiple-Bit Upset (MBU) in several adjacent memory cells. SEUs can become Single-Event Functional Interrupts (SEFI) when they upset control circuits, which would then require a reset or a power cycle to recover. (2) Single-Event Latchup (SEL) (Schrimpf *et al*., 2007). It may occur in any chip with a parasitic PNPN structure. A heavy ion or a high-energy proton passing through one of the two inner-transistor junctions can turn on the

thyristor-like structure, which will stay shorted until the device is power-cycled. As the effect can occur between the power source and substrate, destructively high current may be involved and the part may fail to work. (3) Single-Event Transient (SET) (Adell *et al*., 2005). It occurs when the charge collected from an ionization event discharges in the form of a spurious signal traveling through the circuit. In fact, this is the effect of an electrostatic discharge. (4) Single-event snapback (Walsh *et al*., 2001). It is similar to SEL but not requiring the PNPN structure. It can be induced in N-channel MOS transistors switching large currents, when an ion hits near the drain junction and causes avalanche multiplication of the charge carriers. The transistor then opens and stays opened. (5) Single-event induced burnout (SEB) (Albadri *et al*., 2006). It may occurs in power MOSFETs if the substrate right under the source region gets forward-biased and the drain-source voltage is higher than the breakdown voltage of the parasitic structures. The resulting high current and local overheating then may destroy the device. (6) Single-Event Gate Rupture (SEGR) (Badila *et al*., 2001). It was observed in power MOSFETs if a heavy ion hits the gate region while a high voltage is applied to the gate. A local breakdown then occurs in the insulating layer of silicon dioxide, causing local overheat and destruction of the gate region. It can happen even in EEPROM cells during writing or erasing if the cells are subjected to a comparatively high voltage.

To ensure the proper operation of such systems, manufacturers of integrated circuits and sensors intended for the military aerospace markets adopt various methods of radiation hardening. Radiation hardening (Johansson, 1977) is a technique to design and test electronic components and systems to make them resistant to damage or malfunctions caused by ionizing radiation such as particle radiation and high-energy electromagnetic radiation, which would be encountered in the outer space, high-altitude flight, around nuclear reactors, or during nuclear accidents or nuclear warfare. The resulting systems are called to be radiation-hardened or rad-hard. Most radiation-hardened chips are based on their commercial equivalents, with some manufacturing and design variations that reduce the susceptibility to interference from electromagnetic radiation. Due to the extensive development and testing required to design a radiation-tolerant microelectronic chip, radiation-hardened chips tend to lag behind the cutting-edge of developments.

Since, the early 1980s, the Defense Advanced Research Projects Agency (DARPA) of America has started the research on digital radiation hardening techniques for digital GaAs circuits (Naber, 1995). At the same time, the Department of Defense (DoD) of America also proposed a project to design microwave/millimeter wave single-chip integrated circuits in order to develop GaAs microwave circuits and this project was supported by the Strategic Defense Initiative (SDI) plan, which mainly aims at the application of elements in the outer space. Therefore, with the rapid development of GaAs integrated circuits, the research on total ionizing dose effects and neutron effects has been deeply researched. GaAs has some electronic properties which are superior to those of silicon. It has a higher saturated electron velocity and higher electron mobility, allowing transistors made from it to function at frequencies in excess of 250 GHz. Another advantage of GaAs is that it has a wide bandgap, which means that it is highly resistive to ionization effects. Combined with the high dielectric constant, this property makes GaAs a very good electrical substrate and unlike Si provides natural isolation between devices and circuits. Thus, as a wide direct band gap material with high breakdown voltage and resulting resistance to radiation damage, GaAs is an excellent material for space and optical windows in high power applications. Currently, aiming at various radiation effects, people mainly provide solutions in improving material performance and element structure. For example, we can adopt GaAs process because it can reduce the total ionizing dose effects. Alternatively, we can adopt the HBT (Heterojunction Bipolar Transistor) process (Torvik *et al*., 2000) because its special structure avoids the production of parasitical BJT (Bipolar Junction Transistor) and makes the work area be far from the surface of elements and thus it can resist to much more cosmic radiation. Basically speaking, the radiation hardening techniques can be classified into two categories, i.e., physical solutions and logical solutions. In the remainder of this study, we will overview these two kinds of hardening techniques separately and then propose our radiation hardening scheme in power amplification chip design.

PHYSICAL RADIATION-HARDENING TECHNIQUES

Physical radiation-hardening techniques use various physical means, such as using insulating substrates, utilizing bipolar integrated circuits, adopting radiation-tolerant SRAM, etc., to realize the hardening purpose.

Insulating substrates: Hardened chips are often manufactured on insulating substrates instead of the usual semiconductor wafers. Silicon on Insulator (SOI) and Silicon on Sapphire (SOS) are commonly adopted.

Silicon on Insulator (SOI) technique (Simoen *et al*., 2007) adopts a layered silicon-insulator-silicon substrate instead of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance and thereby improve its performance. The differences between SOI-based devices and conventional silicon-built devices lie in that the silicon junction is above an electrical insulator. The first industrial implementation of SOI was announced by IBM in August 1998. The benefits of the SOI technique compared to conventional silicon processing include: (1) Lower parasitic capacitance due to isolation from the bulk silicon. (2) Resistance to latchup due to complete isolation of the n-and p-well structures. From a manufacturing viewpoint, SOI substrates are compatible with most conventional processes. The primary barrier to SOI implementation is the drastic increase in substrate cost, which contributes an estimated 10-15% increase to total manufacturing costs.

Silicon on Sapphire (SOS) (Roig *et al*., 2004) is a hetero-epitaxial process for integrated circuit manufacturing consisting of a thin layer of silicon grown on a sapphire wafer. SOS is part of the Silicon on Insulator (SOI) family of CMOS technologies. The SOS is mainly used in aerospace and military applications because of its inherent resistance to radiation. The first advantage of sapphire lies in that it is an excellent electrical insulator, preventing stray currents caused by radiation from spreading to nearby circuit elements. The second advantage of silicon on sapphire over exotic technologies is that it is manufactured in the same factories that produce common bulk silicon wafers. A further advantage is that, because of its better performance, it can be manufactured in a less advanced factory than similar devices in bulk silicon. Where silicon on sapphire has disadvantages over bulk silicon is that it is by nature a more complex process. Sapphire substrates are expensive. SOS has seen little commercial use to date because of difficulties in fabricating the very small transistors used in modern high-density applications. They are physically heavy, causing problems with manufacturing machines not designed for their mass.

With regards to radiation tolerance, while normal commercial-grade chips can withstand between 5 and 10 krad, space-grade SOI and SOS chips can survive doses many orders of magnitude greater. At one time many 4000 series chips were available in radiation-hardened versions.

Bipolar integrated circuits: Bipolar integrated circuits contain Bipolar Junction Transistors (BJT) as their principle elements. A Bipolar Junction Transistor (BJT) is a three-terminal electronic device constructed of doped semiconductor material and may be used in amplifying or switching applications. Bipolar transistors are so named because their operation involves both electrons and holes. Charge flow in a BJT is due to bidirectional diffusion of charge carriers across a junction between two regions of different charge concentrations. This mode of operation is contrasted with unipolar transistors, such as field-effect transistors, in which only one carrier type is involved in charge flow due to drift. By design, most of the BJT collector current is due to the flow of charges injected from a high-concentration emitter into the base where they are minority carriers that diffuse toward the collector and so BJTs are classified as minority-carrier devices. A new silicon power device concept based on the Super Junction (SJ) principle for power electronics in a broad spectrum of consumer, industrial and other energy conversion applications is presented by Bauer (2004). This new concept can help to sustain the trend towards ultra low loss switching the past, present and future dominant driving force in the development of silicon high power switches. The Super Junction Bipolar Transistor (SJBT) shares many similarities with the super junction MOSFET. After several decades of development, the GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) has emerged as a high performance, low cost and manufacturable device. Not only does it exhibit excellent noise properties, but it is also the premier power device for frequencies ranging from low microwaves through millimeter waves. Accordingly, it is the ideal device for applications that require high performance, including digital point-to-point radio, future cellular, LMDS and satellite communication. Based on this consideration, a 4 W K-band AlGaAs/InGaAs/GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) Monolithic Microwave Integrated Circuit (MMIC) high Power Amplifier (PA) was reported by the authors of this study (Huang *et al*., 2009).

With regards to radiation tolerance, bipolar integrated circuits generally have higher radiation tolerance than CMOS circuits. It was reported that the low-power Schottky (LS) 5400 series can withstand 1000 krad and many ECL devices can withstand 10 000 krad.

Radiation-tolerant sram: To tolerate radiation, capacitor-based DRAM is often replaced by more rugged (but larger and more expensive) SRAM. A SRAM device used mainly in the read state such as configuration RAM in an FPGA can be hardened against radiation effects to a very high level by adding a large value resistor. A SRAM device used mainly in the read state is usually written only once on power-up to define the function of

the integrated circuit and in most applications it is never changed after power up. Recently, He *et al*. (2008) presented the practical issues encountered in designing SRAM cell design on partially depleted SOI, including the effects of floating-body potential and parasitic bipolar. It also discussed the characteristics of Single-Event Upsets (SEU) hardening and total-dose radiation hardening of SOI SRAM.

Wide band-gap substrate: It can give higher tolerance to deep-level defects by using wide band-gap substrate (Szmidt, 1999). The magnitude of the coulombic potential determines the bandgap of a material and the size of atoms and electronegativities are two factors that determine the bandgap. Materials with small atoms and strong, electronegative atomic bonds are associated with wide bandgaps. Wide Band Gap Semiconductors such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have emerged as one of the most promising materials for future electronic components. They offer tremendous advantages in terms of power capability (DC and microwave), radiation insensitivity, high temperature and high frequency operation, optical properties and even low noise capability. Therefore, wide band gap components are strategically important for the development of next generation spaceborne systems. Although, impressive results have already been demonstrated, a large amount of research and development work still remains to be carried out. In particular, improvements are needed in the quality of the basic crystal materials through to fabrication of complete devices with enhanced performance and reliability. Further research work is required to better understand the semiconductor physics, to improve materials growth and to optimize device performance. In addition, work is also needed to develop advanced packaging techniques and to understand the benefits offered to space systems by undertaking detailed application assessment.

Shielding the package against radioactivity: Obviously, this is an intuitional scheme to reduce exposure of the bare device. Recently, Miller *et al*. (2009) studied the lunar soil as shielding against space radiation. The measurements and model calculations indicated that a modest amount of lunar soil affords substantial protection against primary Galactic Cosmic Radiation (GCR) nuclei and Solar Particle Event (SPE), with only modest residual dose from surviving charged fragments of the heavy beams. Cherng *et al*. (2007) studied two representative spacecraft-shielding materials: aluminum representing low/medium-Z material and tungsten representing high-Z material. Calculation results indicate that, for the radiation attenuation required for typical electronics used in a Jupiter mission, the low-Z material and the low/high-Z combination are a less-efficient shield per the same areal mass than the high-Z material in the Jovian radiation environment. When massive shielding >10 g cm^{-2} is required to protect very radiation-sensitive electronics, then the low- /high-Z combination is a better shield per the same areal mass.

Shielding the chips by using depleted boron: The depleted boron consists only of isotope boron-11. Cosmic radiation will produce secondary neutrons if it hits spacecraft structures; and neutrons cause fission in Boron-10 if it is present in the spacecraft's semiconductors, producing a gamma ray, an alpha particle and a lithium ion. The resultant fission products may then dump charge into nearby semiconductor chip structures, causing data loss (bit flipping, or single event upset). In radiation hardened semiconductor designs, one countermeasure is to use depleted boron which is greatly enriched in Boron-11 and contains almost no Boron-10. Boron-11 is largely immune to radiation damage and it is a by-product of the nuclear industry. In general, the depleted boron is used in the borophosilicate glass passivation layer to protect the chips. Here, borophosphosilicate glass, commonly known as BPSG, is a type of silicate glass that includes additives of both boron and phosphorus (Kern and Smeltzer, 1986).

LOGICAL RADIATION-HARDENING TECHNIQUES

Logical radiation-hardening techniques adopt various logical means, such as using error correcting memory, utilizing redundant elements, adopting a watchdog timer etc., to realize the hardening purpose. Finally, the reliability evaluation problem is introduced.

Error correcting memory: In general, DRAM memory can afford increased protection against soft errors based on error correcting codes. The error-correcting memory, known as ECC (Error Correcting Codes) or EDAC (Error Detection and Correction)-protected memory, is especially suitable for high fault-tolerant applications, such as servers, as well as deep-space applications due to cosmic radiation. It utilizes extra parity bits to check for and possibly correct corrupted data. Since, radiation effects may destroy the memory content even if the system is not accessing the RAM, a so-called scrubber circuit should be used to continuously sweep the RAM. Typically, the following three steps are involved:

Step 1: Reading out the data
Step 2: Checking the parity for data errors
Step 3: Writing back any corrections to the RAM

Traditional error-correcting memory controllers adopt Hamming codes, although, some may use triple modular redundancy (TMD). Interleaving allows us to distribute the effect of a single cosmic ray that potentially upsets multiple physically neighboring bits over multiple words by associating neighboring bits to different words. As long as a Single Event Upset (SEU) is not larger than the error threshold in any particular word between accesses, it can be corrected and the illusion of an error-free memory system can be maintained.

Error-correcting schemes have been widely applied in both memory architectures and communication beginning with Von Neumann's seminal work on repetition codes. However, state-of-the-art CMOS and disk technologies have very small error rates that may be only in order of one in a billion and thus rigorous error correction is not always necessary. Recently, Jeffery *et al.* (2004) proposed a 3-level error correcting memory architecture for nanoscale memory utilizing single- or double-error correcting codes. For high error rates, however, stronger and multiple error correcting codes such as BCH codes are required for nano-scale devices (Sun and Zhang, 2006). Ou and Yang (2004) proposed hardware design for the decoding and encoding routines of Hamming codes, where the memory reliability is increased at the cost of only 5ns delay in the memory access time. Although, Hamming codes are capable of correcting a single error in the block of physical bits used in the encoding, they become less productive for high error rates. In practical applications, the BCH (250, 32, 45) code can provide 99.9956% correctness at 10% bit error rate in memory, but 1 byte error in every 711 bytes is expected to be defective. In general, if we only use error correcting codes, we will need very strong and complex error correction codes resulting in large overhead in area and latency and thus we will lose all the benefits of using nanoscale memory.

According to above description, besides active error correction through encoding, we require using defect maps to store the locations of the faulty bits in memory devices (Vollrath *et al.*, 2001). For reconfigurable architectures, tile-based memory units have been proposed by storing the defect map in a distributed fashion (He *et al.*, 2005; Ziegler and Stan, 2003). However, the drawback of using defect maps in the bit-level lies in that the storage overhead is generally very high. To reduce the size of the required defect map, Tahoori proposed a defect unaware design flow (Tahoori, 2005) that identifies universal defect free subsets within the partially defective chips, while Wang *et al.* (2006) proposed the use of bloom filters for storing defect maps in nanoscale devices. However, hashing for every bit is computationally expensive and may significantly increase the number of memory access times. Therefore, Sun and Zhang (2006) proposed the use of CMOS memory for storing metadata to identify good parts of the memory based on two schemes:

- A two level hierarchy of CMOS and nano-device memory
- A bootstrapping technique to store the reliable block information in some good part of the non-reliable memory and storing this index in the reliable CMOS

We should note that the amount of memory to store the ranges increases with the sparseness of faulty memory bits. It can be shown that when the error rate is close to 10%, the number of entries in the list is very large.

In a word, error correcting codes reduce the defect rate of memory at the cost of additional computation and redundancy. For example, strong error correcting codes (e.g., BCH (250, 32, 45)) are computationally expensive. The encoding and decoding delay is very high. In fact, we can use less complex codes such as concatenation of Hamming and TMR (Triple Modular Redundancy) to produce 90% correct blocks in presence of 10% bit error rate.

Redundant elements: In engineering, redundancy is the duplication of critical components of a system so as to enhance system reliability, typically in the case of a backup or fail-safe. In many safety-critical systems, e.g., fly-by-wire and hydraulic systems in aircraft, some parts of the control system should be triplicated. An error in one component can then be out-voted by the other two. In a triply redundant system, its three sub components must fail before the system fails. Since, each one seldom fails and is expected to fail independently, the probability that all three fail is calculated to be extremely small. Redundancy is also known as the term majority voting systems (Srihari, 1982) or voting logic. More generally, there are four major forms of redundancy as follows:

- Hardware redundancy, such as DMR (Dual Modular Redundancy) and TMR
- Information redundancy, such as error detection and correction methods
- Time redundancy (Lisnianski *et al.*, 2000), including transient fault detection methods such as alternate logic
- Software redundancy, such as N-version programming (Goseva-Popstojanova and Grnarov, 1993)

Redundant elements can be used at the system level or the circuit level. At the system level, three separate microprocessor boards may independently compute an answer to a calculation and compare their answers. Any system that produces a minority result will recalculate. Logic may be added to shut down the board occurring repeated errors. At the circuit level, a single bit may be replaced with three bits and separate voting logic for each bit to continuously determine its result. However, this strategy will increase the area of a chip design by a factor of 5, so it must be reserved for smaller designs. But it has the secondary advantage that it is also fail-safe in real time. In the event of a single-bit failure, the voting logic will continue to produce the correct result without resorting to a watchdog timer. System-level voting between three separate processor systems will generally need to use some circuit-level voting logic to perform the votes between the three processor systems.

Recently, Nepal *et al*. (2006) introduced a new redundancy element, the MRF reinforce, which achieves significant immunity to single-event upsets and noise. Myers and Rauzy (2008) studied the assessment of the reliability of redundant systems with imperfect fault coverage. They termed fault coverage as the ability of a system to isolate and correctly accommodate failures of redundant elements. For highly reliable systems, such as avionic and space systems, fault coverage is in general imperfect and has a significant impact on system reliability. They reviewed different models of imperfect fault coverage and proposed efficient algorithms to assess them separately. Gonzalez and Mazumder (2000) presented a survey of circuit implementations of redundant arithmetic algorithms in three main groups:

Group 1: Conventional binary logic circuits, which encode the multivalued digits of redundant arithmetic into two or more binary digital signals
Group 2: Current-mode multiple-valued logic circuits, which directly represent multivalued redundant digits using non-binary digital current signals
Group 3: Heterostructure and quantum electronic circuits, intended for very compact designs capable of operating at extremely high speeds

For each of the circuits, the operating principle was described and the main advantages and disadvantages of the approach were discussed and compared.

Watchdog timers: A watchdog timer can be employed to perform a hard reset of a system unless some sequence is performed that generally indicates the system is alive, such as a write operation from an onboard processor. During normal operations, software schedules a write to the watchdog timer at regular intervals to prevent the timer from running out. If the radiation causes the processor to operate incorrectly, it is unlikely that the software will work correctly enough to clear the watchdog timer. The watchdog eventually times out and forces a hard reset to the system. This is considered as a last resort to other methods of radiation hardening.

Recently, El-Attar and Fahmy (2007) studied the ability of different watchdog timer systems to recover the system from failure and a new improved watchdog timer system design was introduced. They first introduced standard watchdog timers and windowed watchdog timers and then proposed their sequenced watchdog timers. A standard watchdog timer in its simplest form is a monostable timer. When the timer reaches its maximum value it changes its logical state. The system must reset the timer before it reaches maturity. If the system fails to reset the timer an action is taken whether to change the state of an output or to immediately restart the system. In order to solve the problem of fast watchdog resets, the windowed watchdog timer adopt a new supervisory system based on two timers instead of one. The first Timer has a timeout of T1 and the second timer has a timeout of T3. The ClearWDT instruction must be executed within a time window of (T3-T1) to reset both timers, where T3>T1. The sequenced watchdog timer is an improved design of the windowed watchdog timer. It requires minor modifications to the ClearDWT instruction. The ClearDWT instruction is originally an inherent, which means it does not require and operand to be executed. The instruction is modified to include an operand. Once the Opcode is Fetched and decoded, the control unit resets the Windowed watchdog timer. If a slow or fast resets occur the watchdog immediately resets the system. If the ClearDWT opcode is executed within the safe window then the operand is compared to the value of the sequenced timer register. If the value matches, then the system is operating properly. If the value does not match then a faulty reset occurred within the safe window of the watchdog timer. The sequenced watchdog timer then resets the whole system.

Reliability evaluation: It should be noticed that, in addition to above hardening techniques, how to test the reliability of the integrated circuit is also a very important topic. Recently, a novel approach for MMIC (Monolithic Microwave Integrated Circuits) reliability testing based on Weibull distribution (Huang *et al*., 2009b) was proposed by the authors of this study. We also proposed a methodology to predict the GaAs MMICs reliability by combining empirical and statistical methods based on

zero-failure GaAs MMICs life testing data (Huang *et al*., 2009a). Besides, we investigated the effect of accelerated factors on MMICs degradation and make a comparison between the Weibull and lognormal distributions. The method has been used in the reliability evaluation of GaAs MMICs successfully.

PROPOSED RADIATION-HARDENING TECHNIQUES FOR MICROWAVE POWER AMPLIFIER CHIP DESIGN

Background: An amplifier is one of the most common electrical elements in any circuit system. The requirements for amplification are as varied as the systems where they are applied. Amplifiers are available in various forms ranging from minuscule ICs to the largest high-power transmitter amplifiers. An RF power amplifier (Grebennikov, 2005) is a sort of electronic amplifier employed to convert a low-power radio-frequency signal into a larger signal with significant power typically in order to drive the antenna of a transmitter. It is usually optimized to have high efficiency, high output power compression, good return loss on the input and output, good gain and optimal heat dissipation. As a high-power device with large gain, it provides large output signal power while requiring very small amount of RF power and it is commonly available from any commercial signal generator. Therefore, the power amplifier is normally known as the RF source or sometimes the Transmitter. Microwave power amplifiers can be utilized in testing applications ranging from passive elements such as antennas to active devices such as limiter diodes or MMIC based power amplifiers. Furthermore, some other applications include testing requirements where a relatively large amount of RF power is necessary for overcoming system losses to a radiating element, or where there is a system requirement to radiate a Device-Under-Test (DUT) with an intense electromagnetic field.

As a key link for wireless applications, solid-state active power amplifiers have been widely used in satellite communication, radar, electronic warfare, satellite navigation and weapon guidance systems. Due to the harsh requirements and the complexity of the transmission environment in wireless communication, the design of microwave power amplifiers almost becomes one of the most difficult functional units in the front of an RF transceiver system and its linearity, output power and efficiency greatly affect the signal quality, communication distance and communication time of the wireless communication system. Among these systems, because of the adverse external environment, aerospace applications not only impose higher more stringent requirements upon the performance of solid-state active power amplifier but also bring greater challenges for its design.

All the countries in the world (particularly the US and Japan) pay much attention to solid-state active power amplification chip design and manufacturing technology and they have developed many new products, such as the entire microwave system integrated in a single chip with a diameter of few centimeters. This chip has been substituted for the earlier microwave hardware chassis. This new microwave system on chip has greatly improved the performance of microwave systems and promotes the development of communication technology, radar technology and aerospace technology. In 1996, the Department of Defense of USA announced three national defense science and technology strategy files, i.e., Joint Warfighting Science and Technology Plan (JWSTP), Defense Technology Area Plan (DTAP), Basic Research Plan (BRP), which were modified in 1997. With regard to the microwave and millimeter wave circuit design, they planned that in the late 1990s to the early 21st century they would focus on the research and development of millimeter-wave/microwave monolithic circuits, high-temperature and high-power circuits and multi-module circuits, whose core is the heterojunction devices and circuits. One of the prominent properties of microwave component is small volume and weight. The development of Monolithic Microwave Integrated Circuits (MMICs) also speeds up the millimeter wave instrument size and weight reduction, higher reliability. This also brings more rigorous requirements for microwave component thermal design. Recently, the authors of this study proposed a microwave component thermal design method based on microstructure heat transfer (Yu *et al*., 2010b).

Among various solid-state power amplifier chip production technologies, Heterojunction Bipolar Transistor (HBT) becomes one of the most popular power chip technologies due to its high efficiency, large gain, good linearity and high power density. So far, HBT has been paid widespread attention and has been made great progress. The HBTs made from a variety of materials continue to emerge and their performance is unceasingly improved. Currently available and abuilding global networks based on Low Earth Orbit (LEO) communication satellites have a rising demand for PAs used in interstellar communication. To achieve high reliability and miniaturization purposes, it is necessary to solidify the existing Traveling Wave Tubes (TWT) and the HBT with high power density is suitable for high-power requirements. At present, the demand of applying HBTs in L ~ C bands is growing and the HBT has become the best candidate to substitute the former power traveling

wave tubes in L~ C bands due to its high power density, high efficiency and high linearity characteristics. To improve the linearity, recently, an adaptive linearization bias technique (Yu *et al*., 2010a) for microwave solid-state active power amplifier design was proposed by the authors of this study. Although, a single-chip radio-frequency integrated circuit cannot output large power due to current restrictions on the production process and also cannot provide comparable power level as TWT, it is a feasible solution to combine them with the circuit or array synthesis technology. For aerospace applications of solid-state active power amplifier chip, during the chip design, we should meet the power targets as well as considering the specific characteristics of aerospace applications in addition to performing complex trade-off among the key performance such as efficiency, power and reliability.

Radiation is an important reason to cause anomalies or failures of spacecraft's electronic equipments and it is reported that about 40% of the faults come from space radiation. Therefore, radiation hardening technology is the key technology to keep aerospace electronic equipments operating with long life and high reliability and it is the research focus and hot in the field of astronautic electronics. According to the number of particles causing damage, radiation effects can be divided into: the effect caused by Single-Particle Events (SEE) and the cumulative effect such as Total Ionizing Dose (TID) and Displacement Damage (DD).

In the radiation hardening design, our solution is to obtain relatively high resistance to total ionizing dose effects based on derating design and fabrication process line selection. When a large number of cosmic particles enter into the chip substrate, a large amount of ionization will be produced, but the chip performance will remain stable and no deterioration will occur. Secondly, relatively high resistance to burnout caused by the particle radiation can be obtained, i.e., the chip will not be burned out even if the parasitic effect has been inspired by high energy particles or a large disturbance of electrical properties has occurred. Thirdly, the resistance to displacement damage to a certain degree can be obtained, i.e., even if a considerable amount of particle radiation has changed the circuit performance, the chip will still be able to work stably and reliably in the space environment with minor injuries. In allusion to various damage mechanisms, we mainly take following two measures:

Microelectronic radiation-hardening: When traditional MOS or bipolar elements are injected with high-energy particles, they will interact with the oxide (SiO_2) and will be ionized, resulting in a large number of electron-hole pairs, which have two motion trends, i.e., recombination and drift. If there is no external electric field, the recombination trend is stronger. If there is electric field, the electron and hole will move to opposite directions along the electric field, the electron can quickly leave the oxide due to its transfer rate is very high, resulting in the accumulation of holes within the oxide, forming a gate oxide hole capture. The greater the electric field strength is, the higher electron mobility is and the stronger the gate oxide capture is. That is why the TID damage with electronic components is severer than that without electrical components. Gate oxide and interface capture generate the parasitic electric field in the device work area, resulting in the drift of threshold voltage V_{th} and the propagation delay T_{pd}, the increase of static current Icc, as well as the reduction of the magnification coefficient of the transistor. When the damage exceeds a certain threshold, the elements will fail to work.

With respect to material selection, we notice that GaAs is a kind of III-V semiconductors with high speed, high frequency, high temperature resistance, low noise and light and so on. Compared with Si, GaAs has many advantages in the physical nature, particularly the high electron mobility (8500 cm/V•s) and large band gap (1.424 eV), which make GaAs devices not only be able to work at a high temperature but also possess high radiation hardness. Many studies have verified that the GaAs material has good particle detection performance and good resistance to γ-ray induced damage.

In the design of microelectronic devices within the circuit, we adopt high radiation-tolerant devices to improve the radiation resistance of outside circuits. HBT occupies a unique and important position in high-speed, large dynamic range, low harmonic distortion and low phase noise circuits. It uses wide-band emitter and allows high-doped base region, which can achieve high cutoff frequency, high gain, high efficiency and high linearity and high breakdown voltage (10-15 V), while its excellent radiation-tolerant performance is very suitable for space power amplifier applications. Compared with the radiation tolerance of the field-effect transistors MESFET and HEMT, HBT has the following advantages: (1) It has high breakdown voltage. The HBT collector has wide band-gap materials, we can get high breakdown voltage through the design of collector thickness and doping concentration, resulting in large output power. And, the reverse breakdown voltage of collector junction (BC junction) that determines the breakdown voltage of HBT depends on the epitaxial material and it is less susceptible to the process. (2) it has low leakage current. (3) the turn-on voltage of HBT is determined by the intrinsic energy gap of the epitaxial material and has nothing to do with the

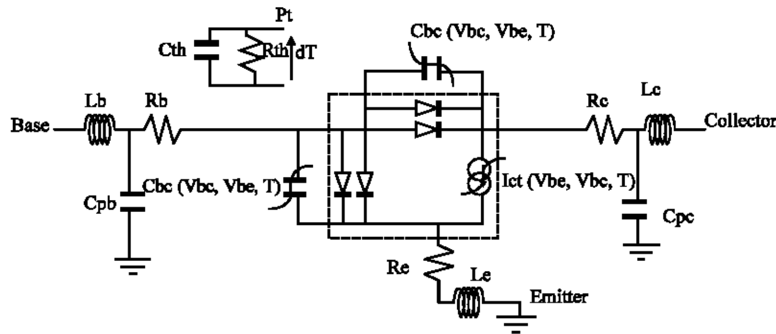

Fig. 1: Improved tube core structure

process and it has good reproducibility. (4) it can avoid the back gate effect. In a word, it is because of the high breakdown voltage of GaAs HBT, its low leakage current and its vertical structure that it can avoid the back gate effect and it has high radiation hardness to space environment.

With regard to the process, we cooperate with foreign fabrication manufacturers to modify the process according to special requirements of radiation hardening. We alleviate the radiation effects by reducing parasitic device parameters as much as possible, e.g., adjusting the doping concentration of GaAs to release TID effects. We also adjust the structural layout to reduce parasitic devices to ease radiation effects and thus slow the TID damage.

In addition, we modify the original tube core model by adding a thermal model as shown in Fig. 1. We perform the accurate simulation to investigate the performance change due to the radiation under the actual conditions, so as to optimize the circuit later and improve the manufacturability and reliability of the chip.

Radiation-tolerant circuit design: Radiation-tolerant circuit design covers the entire process of circuit design, analysis and simulation, including failure link analysis, tolerance design, derating design methods that aim to find and predict the weak links in damage, adopt hardening or tolerance design, so as to improve the capacity of the circuit against radiation.

Failure link analysis: By analyzing the changes in damage parameters and the impact on other parts, we find the key link or weak link, which is the foundation of derating design and tolerance design.

Derating design: By deliberately reducing the heat and electronic stresses imposed on electrical components, we reduce the radiation failure rate of components. We reasonably design the bias circuit and choose the work point, so as to let the circuit work with a relatively reliable voltage and thus effectively reduce the possibility of burnout due to cosmic particles. We adopt multi-tube parallel structure and preserve appropriate power redundancy to cope with the circuit disturbance caused by cosmic particles.

Tolerance design: With regard to the cumulated damage such as TID and displacement damage, their radiation damage behaves the drift of circuit parameters such as the transistor amplification rate and reverse breakdown voltage. If the circuit parameters are set incorrectly, once the parameters drift because of radiation, the system will not work. Thus, based on the parameter drift rule, we perform the tolerance design for device parameters, so as to make the device reliably work with minor injuries. We can add the appropriate feedback and adopt a stable structure and select the appropriate operating point to make the DC operating point be in the secure area, so as to get greater tolerance capability.

Through the radiation hardening design, the result shows that the resistance of our chip to neutron radiation is larger than 10^{15} n cm^{-2}, while the resistance to ionizing radiation is larger than 10^{7}rad and the resistance to transient radiation is larger than 10^{9}rad sec^{-1}.

CONCLUSIONS

In this study, we overview physical and logical radiation hardening techniques and propose some effective solutions in our power amplification chip design to resist the radiation. Typical physical radiation-hardening techniques are using insulating substrates, utilizing bipolar integrated circuits, adopting radiation-tolerant SRAM. Typical logical radiation-hardening techniques are using error correcting memory, utilizing redundant elements, adopting a watchdog timer. In the radiation hardening design for power amplification chips, our solution is to obtain relatively high resistance

to total ionizing dose effects based on derating design and fabrication process line selection. We adopt the GaAs HBT process because of the high breakdown voltage of GaAs HBT, its low leakage current and its vertical structure and it can avoid the back gate effect and it has high radiation hardness to space environment. We alleviate the radiation effects by reducing parasitic device parameters as much as possible and we adjust the structural layout to reduce parasitic devices to ease radiation effects and thus slow the TID damage. In radiation-tolerant circuit design, we perform failure link analysis, tolerance design, derating design methods to improve the capacity of the circuit against radiation.

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