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The Design of a Matched Filter based on Time Division Multiplex

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Abstract: The acquisition of Pseudo-Noise (PN) code is one of the essential technologies in Direct Sequence Spread Spectrum (DS/SS) communication. Conventional Parallel Matched Filter (CPMF) features in high acquisition speed but it will consume a large amount of hardware resource in the case of long PN code. This paper focuses on reducing the hardware consumption and proposes a novel matched filter architecture: Time Division Multiplex Matched Filter (TDMMF). With identical processing gain as CPMF, TDMMF can save the hardware consumption by 50, 75% and even more through reusing the shift registers, multipliers and accumulators. This makes the proposed TDMMF suitable for high speed acquisition of long PN code.

Key words: Direct sequence spread spectrum communication, PN code acquisition, time division multiplex matched filter, field programmable gate array (FPGA)

INTRODUCTION

Direct Sequence Spread Spectrum (DS/SS) technology provides significant advantage in the aspects of strong anti-jamming capability, low probability of intercept, multiple-access operation and so on (Zhi *et al*., 2009; Chen *et al*., 2010), making it widely used for military and civilian (Wu *et al*., 2010; Tong *et al*., 2011), such as Global Position System (GPS) and the third-generation cellular systems (Shahid *et al*., 2008). However, in order to take full advantage of DS/SS, the receiver must first synchronize the received and local Pseudo-Noise (PN) code properly (Porcello, 2011), because the misalignment will make the subsequent dispreading and demodulation stages impossible to implement. Therefore, PN code acquisition serves as the crucial stage in DS/SS receiver and a number of methods have been proposed such as Serial Search Acquisition (Van Der Meer and Liyana-Pathirana, 2003), Sequential Estimation Acquisition (El-Agooz *et al*., 2007), Parallel Matched Filter Acquisition (Tan, 2005) and so on. Among the conventional methods, Conventional Parallel Matched Filter (CPMF) is considered to be the fastest acquisition way at the expense of large hardware consumption. Especially in the situation of long PN code, the huge hardware cost makes it impractical to implement (Lin *et al*., 1996). Concentrated on this disadvantage of CPMF, the paper presents a novel matched filter architecture based on time division multiplex. In the proposed Time Division Multiplex Matched Filter (TDMMF), calculation of local sequence and received signals correlation is implemented in several segments by the same registers, multipliers and accumulators at different time. The previous segmented correlation is stored in FIFO and adds to the last segmentation, forming the output of TDMMF. Because of the reuse of logical resource, the total hardware consumption will be dramatically cut down compared with CPMF.

Conventional parallel matched filter: Guan and Chen (2005) have presented the scheme of CPMF. Without loss of generality, the length of PN code is 255 and the incoming data width is 12 bits with one sample per chip. The incoming signal is firstly shifted into the input registers and multiplied with the local PN code. The output of CPMF R(i) can be expressed as:

$$R(i) = \sum_{m=1}^{255} C_m d_{i+m} \quad (1)$$

where, C_m is the local PN sequence coefficient; d_{i+1}, d_{i+2}, …, d_{i+255} are the incoming signal stored in the input shift registers. The output is then compared with a threshold to determine whether the incoming sequence has matched the local one which takes one PN period at most.

The CPMF above takes 255×12 = 3060 registers and 255 multipliers. The logical resource consumption will increased dramatically as the length of local sequence coefficient increases. Accordingly the length of PN code and thus the spread spectrum gain will be greatly constrained. Therefore, reducing the hardware cost serves as the critical point in implementation of match filter.

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Table 1: Data change in TDMMF

i	Data in shift registers (left⇨right)	Data in FIFO (left⇨right)	Reg1	Reg2	Filter output
0	$d_{128},d_{127},\ldots,d_1$	$R_1(0), R_1(-1),\ldots,R_1(-127)$	$R_1(-128)$	$R_2(0)$	R(-128)
1	$d_{129},d_{128},\ldots,d_2$	$R_1(1), R_1(0),\ldots,R_1(-126)$	$R_1(-127)$	$R_2(1)$	R(-127)
…	…	…	…	…	…
126	$d_{254},d_{253},\ldots,d_{127}$	$R_1(126),R_1(125),\ldots,R_1(-1)$	$R_1(-2)$	$R_2(126)$	R(-2)
127	$d_{255},d_{254},\ldots,d_{128}$	$R_1(127),R_1(126),\ldots,R_1(0)$	$R_1(-1)$	$R_2(127)$	R(-1)

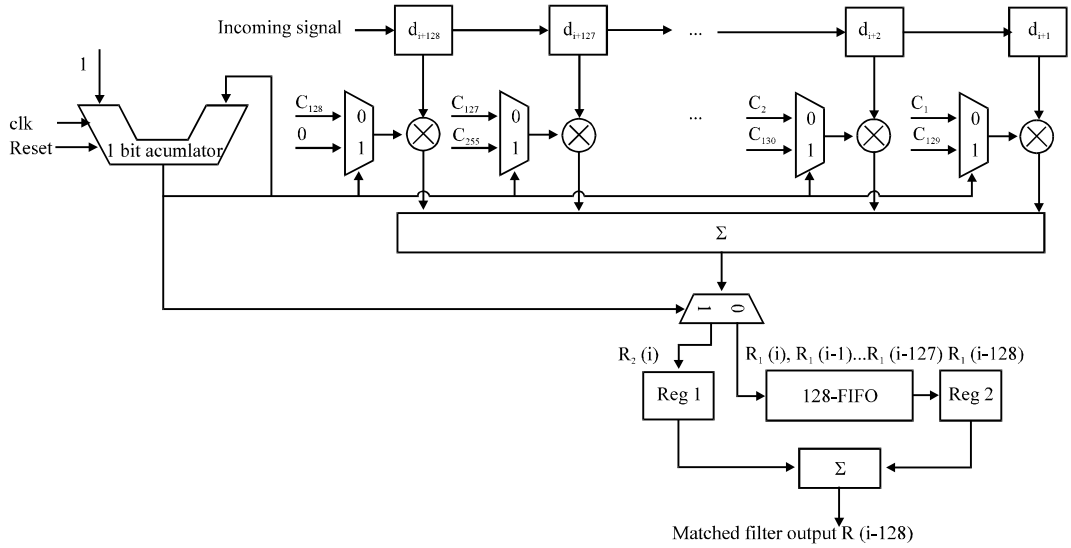

Fig. 1: The scheme of basic TDMMF

Basic TDMMF architecture: With the same notation of the last Section, the correlation of the incoming and locally generated PN sequences R(i) can be divided into two segments, as show in Eq. 2:

$$R(i)=\sum_{m=1}^{255}C_m d_{i+m}=\sum_{m=1}^{128}C_m d_{i+m}+\sum_{m=129}^{255}C_m d_{i+m} \quad (2)$$

Let us introduce the quantities $R_1(i)$ and $R_2(i)$ to represent the two segments as shown in Eq. 3 and 4:

$$R_1(i)=\sum_{m=1}^{128}C_m d_{i+m} \quad (3)$$

$$R_2(i)=\sum_{m=1}^{127}C_{m+128}\, d_{i+m} \quad (4)$$

For the first 128 incoming data, $R_1(i)$ represents the correlation of $d_{i+1}, d_{i+2}, \ldots, d_{i+128}$ and $C_1, C_2, \ldots, C_{128}$ while $R_2(i)$ the correlation of $d_{i+1}, d_{i+2}, \ldots, d_{i+127}$ and $C_{129}, C_{130}, \ldots, C_{255}$.

Therefore, R(i) can be re-expressed as the sum of $R_1(i)$ and $R_2(i+128)$,as shown in Eq. 5:

$$R(i)=\sum_{m=1}^{128}C_m d_{i+m}+\sum_{m=1}^{127}C_{m+128}d_{i+m+128}=R_1(i)+R_2(i+128) \quad (5)$$

The scheme of the basic TDMMF is shown in Fig. 1. The length of the input shift registers is 128, one half of the PN code period. The clock of TDMMF is clk, whose frequency is twice of the incoming data rate. It needs two clks to calculate the correlation of the input 255 data and the local PN code. At the first clk, it calculates the correlation of $d_{i+1}, d_{i+2}, \ldots, d_{i+128}$ and $C_1, C_2, \ldots, C_{128}$ which is $R_1(i)$ and pushes it into a 128-FIFO. At the same time, the FIFO pops the previous stored correlation $R_1(i-128)$ out from its head to the register Reg2. Meanwhile, the taps change from $C_1, C_2, \ldots, C_{128}$, to $C_{129}, C_{130}, \ldots, C_{255}, 0$. At the second clk, it calculates the correlation of $d_{i+1}, d_{i+2}, \ldots, d_{i+127}, d_{i+128}$ and $C_{129}, C_{130}, \ldots, C_{255}, 0$ which is $R_2(i)$ and puts it into register Reg1. Similarly, the taps also change from $C_{129}, C_{130}, \ldots C_{255}, 0$ to $C_1, C_2 \ldots, C_{128}$ simultaneously. Consequently, the sum of Reg1 and Reg2 makes up the correlation of $d_{i-128}, d_{i-126}, \ldots, d_{i+127}$ and $C_1, C_2, \ldots, C_{255}$ which is R(i-128). Table 1 shows the data change in TCMMF. From the Table we can see that the FIFO acts as a shifter while Reg1 and Reg2 store the 2 segmented correlation, respectively.

Hardware consumption of TDMMF in Fig. 1 is analyzed as follows. The input shift registers takes 12×128 = 1536 registers while the correlation implementation take 128 multipliers. Furthermore, the FIFO depth is 128 with data width of 19 bits, making it consuming 128×19 = 2432bits RAM. In general, the total

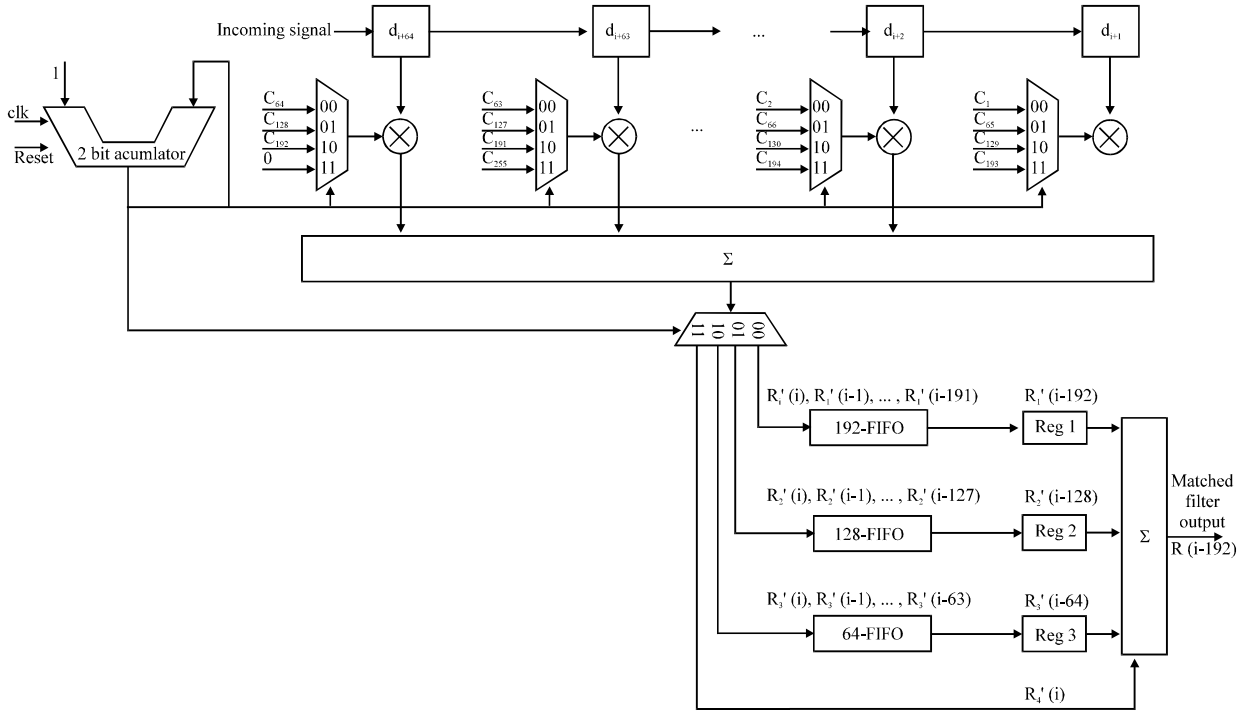

Fig. 2: The scheme of advanced TDMMF

hardware cost is reduced by one half compared with CPMF.

However, TDMMF has its limitation. Because of the multiplex of the logical resource, TCMMF has to be implemented with twice the frequency of CPMF. Accordingly, the speed requirement of the implemented device will be higher.

Advanced TDMMF architecture: TDMMF can be further exploited to achieve a larger reduction in hardware consumption. Similar with the Basic TDMMF architecture, the correlation R(i) can be further divided into four segments, as show in Eq. 6:

$$R(i)=\sum_{m=1}^{255}C_m d_{i+m}=\sum_{m=1}^{64}C_m d_{i+m}+\sum_{m=65}^{128}C_m d_{i+m}+\sum_{m=129}^{192}C_m d_{i+m}+\sum_{m=193}^{255}C_m d_{i+m} \quad (6)$$

Accordingly, the local PN code can also be divided into four segments: C_1, C_2, …, C_{64}; C_{65}, C_{66}, …, C_{128}; C_{129}, C_{130}, …, C_{192} and C_{193}, C_{194}, …, C_{255}. Define the correlations of the input 64 data d_{i+1}, d_{i+2}, … , d_{i+64} and the four segments are $R'_1(i)$, $R'_2(i)$, $R'_3(i)$ and $R'_4(i)$ respectively, as shown in Eq. 7-10:

$$R'_1(i)=\sum_{m=1}^{64}C_m d_{i+m} \quad (7)$$

$$R'_2(i)=\sum_{m=1}^{64}C_{m+64} d_{i+m} \quad (8)$$

$$R'_3(i)=\sum_{m=1}^{64}C_{m+128} d_{i+m} \quad (9)$$

$$R'_4(i)=\sum_{m=1}^{63}C_{m+192} d_{i+m} \quad (10)$$

Therefore, The correlation R(i) can be expressed as the sum of $R'_1(i)$, $R'_2(i+64)$, $R'_3(i+128)$ and $R'_4(i+192)$, as shown in Eq. 11:

$$R(i)=\sum_{m=1}^{64}C_m d_{i+m}+\sum_{m=1}^{64}C_{m+64} d_{i+m+64}+\sum_{m=1}^{64}C_{m+128} d_{i+m+128}+\sum_{m=1}^{63}C_{m+192} d_{i+m+192}$$
$$=R'_1(i)+R'_2(i+64)+R'_3(i+128)+R'_4(i+192) \quad (11)$$

Based on Eq. 11, the scheme of Advanced TDMMF is shown in Fig. 2. The input register length is 1/4 of the PN code period and the clock frequency is four times of the incoming data rate. In the consecutive 3 clks, the TDMMF calculates $R'_1(i)$, $R'_2(i)$ $R'_3(i)$ and pushes them into 3 FIFOs respectively. At the same, the 3 FIFOs pop out the data out from their heads to the registers Reg1, Reg2 and Reg3, respectively. Because the 3 FIFOs' depth

Table 2: The comparison of logical resource used between CPMF and TDMMF

Resource used /total resource	CPMF	TDMMF
Registers	5397/48352	2776/48352
Combined logic	4472/48352	2799/48352
RAM	0/2544192	2432/2544192

are 192, 128 and 64, the data in Reg1, Reg2 and Reg3 will be $R'_1(i-192)$, $R'_2(i-128)$ and $R'_3(i-64)$ respectively. At the fourth clk, $R'_4(i)$ is obtained and added with Reg1, Reg2 and Reg3, serving as the output of TDMMF.

The advanced TDMMF takes 12×64 = 768 registers, 64 multipliers. The total FIFO length is 192+128+64 = 384 with the data width of 18 bits, making it consuming 384×18 = 6912 bits RAM. Generally, the total hardware consumption is reduced by 75% compared with CPMF.

Test in FPGA: Based on Altera Stratix II FPGA EP2S60F1020C5, the CPMF and proposed TDMMF in Fig. 1 are designed by Very-High-Speed Integrated Circuit Hardware Description Language (VHDL). Table 2 shows the logical resources usage of the two approaches after the logic synthesis by Quartus II 8.1 which demonstrates that the TDMMF can save the registers and combined logic consumption by 50%. Despite of the consumption of RAM which far surpasses the registers and combined logic in quantity (Altera Company, 2007), the total hardware cost has dramatically reduced.

CONCLUSIONS

The study has presented a novel matched filter architecture based on the analysis of CPMF. Concentrated on the large hardware consumption of CPMF, the proposed TDMMF has employed the method of time division multiplex to reuse the logical resource, leading the chip area to be apparently cut down. Basic and advanced scheme of TDMMF has been developed in this paper which can achieve 50 and 75% reduction in hardware consumption, respectively. In addition, synthesis on FPGA has confirmed that TDMMF outperforms CPMF in hardware cost. Finally, the advantage of TDMMF will be more significant for long PN code acquisition, making it more suitable for DS/SS system.

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