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New Low-leakage Flip-flops with Power-gating Scheme for Ultra-low Power Systems

[1]Jianping Hu, [2]Xiaoying Yu and [2]Jindan Chen
[1]Ningbo University, China
[2]Faculty of Information Science and Technology, Ningbo University, China

Abstract: With the growing uses of portable computers, energy-efficient designs have become more and more important for computer hardware. This study presents new low leakage power flip-flops with power-gating scheme for ultra-low power systems. The proposed flip-flops are realized based on CMOS ratioed latches with the master-slave structure. Dual-threshold CMOS (DTCMOS) and channel length biasing techniques are used for the flip-flops with power-gating scheme to reduce leakage power dissipations. All circuits are verified with HSPICE simulations by using the BSIM4 predictive models at a 45 nm CMOS process. The results showed that the proposed low leakage ratioed flip-flop realized with the integrated leakage reduction techniques achieves large leakage savings compared with the transmission-gate flip-flop.

Key words: Digital integrated circuits, power-gating flip-flops, DTCMOS, channel length biasing, energy efficient design

INTRODUCTION

With the growing uses of portable computers, energy-efficient designs have become more and more important (Kim *et al*., 2003). In nanometer CMOS digital circuits, power dissipation consists of dynamic and static components. Before the CMOS technology is scaled into deep sub-micro processes, the dynamic energy loss has always dominated total power dissipations, while leakage power dissipation is little and often neglected (Rabaey, 1996). Continued technology scaling reduces area and delay of circuits at the expense of degradation in leakage power dissipation (Roy *et al*., 2003). The leakage dissipation caused by leakage currents catches up with the dynamic power consumption gradually and it is becoming an important factor in low-power computer hardware (Fallah and Pedram, 2005).

There are several leakage sources in nanometer CMOS processes: sub-threshold leakage current due to very low threshold voltage (V_{TH}), gate leakage current due to very thin gate oxide (T_{OX}) and band-to-band tunneling leakage current due to heavily-doped halo (Roy *et al*., 2003). As the threshold voltage scales down, sub-threshold leakage current increases exponentially, so that sub-threshold leakage currents have become the main sources of power dissipations in recent nanometer CMOS processes. Several leakage reduction techniques, such as DTCMOS (Dual Threshold CMOS), MTCMOS (Multi-Threshold CMOS) power-gating technique, stacking transistor techniques, VTCMOS (Variable Threshold CMOS) and IVC (Input Vector Control) have been proposed in recent years and achieved considerable energy savings for portable computers (Fallah and Pedram, 2005).

Flip-flops are essential element of digital systems. In this study, new low leakage power flip-flops with power-gating scheme are proposed for ultra-low power systems. The proposed flip-flops are realized based on CMOS ratioed latches with the master-slave structure. Dual-threshold CMOS (DTCMOS) and channel length biasing leakage techniques are used for the flip-flops to reduce leakage power dissipations. All circuits are verified with HSPICE simulations by using the BSIM4 predictive models at a 45 nm CMOS process. The simulation results show that the proposed flip-flop achieves considerable leakage reductions compared to the transmission-gate flip-flop.

LEAKAGE POWER REDUCTION TECHNIQUES FOR FLIP-FLOPS

The sub-threshold current of MOS transistors I_{sub} occurs due to minority carrier move by diffusion along the surface below the channel, when the gate voltage is below the threshold voltage. It is the dominant contributor to the total leakage current at nanometer CMOS process. I_{sub} can be written as (Roy *et al*., 2003):

Corresponding Author: Jianping Hu, Ningbo University, China

$$I_{sub} = \frac{W}{L}\mu V_T^2 C_{sth} \exp\left(\frac{V_{GS} - V_{th} + \eta V_{DS}}{nV_T}\right)\left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (1)$$

where, W and L denote transistor width and length, μ denotes carrier mobility, $V_T = kT/q$ (~26mV) is thermal voltage at temperature T, $C_{sth} = C_{dep}+C_{it}$ denotes the summation of depletion region capacitance and interface trap capacitance both per unit area of the MOS gate, V_{GS} and V_{DS} are gate-source voltage and drain-source voltage, V_{th} is threshold voltage, η is Drain-Induced Barrier Lowering (DIBL) coefficient and $n = 1+ C_{sth}/C_{ox}$ is slope shape factor, where, C_{ox} is gate input capacitance per unit area of the MOS gate.

From Eq. 1, the sub-threshold leakage current increases exponentially with threshold voltage (V_{th}). For a typical technology with a sub-threshold slope of 100 mV/decade, each 100 mv reduction in V_{th} will cause an order of magnitude increase in leakage currents. Therefore, increasing the threshold voltage can reduce leakage dissipations. Several leakage reduction technologies, such as MTCMOS power-gating techniques, DTCMOS, and gate-length biasing have been applied to low-power flip-flops by increasing the threshold voltage (Kao and Chandrakasan, 2001; Seomun *et al*., 2007; Zhang *et al*., 2011; Gupta *et al*., 2006).

Power-gating techniques: The MTCMOS power-gating technique is an attractive leakage reduction technique especially in the computer system where the circuit spends the majority of the time in a standby state. Power-gating technique uses High-Threshold Voltage (HTV) gating transistors to reduce the leakage current in sleep mode and Low-Threshold Voltage (LTV) transistors to keep fast performance in active mode.

In active mode, the HTV gating transistors are turned on, and the virtual power line is slightly less than the supply voltage due to the IR drop across the gating transistors. This reduction leads to an increase in logic delay. Therefore sizes of gating transistors need to be optimized.

In sleep mode, the gating transistors are turned off and determine the overall leakage current. HTV transistors lead to an exponential decrease in sub-threshold leakage current with increased V_{th}.

The MTCMOS power-gating approach is easy realized in combinatorial circuits. For traditional CMOS flip-flops, all data stored in the circuit will be irreversibly lost when the power supply is turned off. Therefore, the MTCMOS technology is difficultly applied to flip-flops directly. MTCMOS Flip-flops use usually data-retention techniques with extra circuits to store values during sleep mode (Kao and Chandrakasan, 2001).

DTCMOS techniques: Assuming symmetrical PMOS and NMOS, the delay of an inverter can be written as (Rabaey, 1996):

$$t_d = KC_L V_{dd} / (V_{dd} - V_{th})^a \quad (2)$$

where, K is a delay fitting parameter, C_L is load capacitance, V_{dd} is supply voltage and a is velocity saturation parameter about 1 to 2.

From Eq. 2, the delay of a circuit is proportional to the threshold voltage (V_{th}), while the sub-threshold leakage current is exponentially proportional to the threshold voltage according to Eq. 1. Therefore, the dual-threshold CMOS technique can be used for the flip-flops to reduce leakage power. In DTCMOS flip-flops, some transistors on non-critical paths use Gneral-treshold Voltage (GTV) devices to reduce their leakage currents, while the other transistors on critical paths use Low-Threshold Voltage (LTV) devices to maintain the performance (Zhang *et al*., 2011). The DTCMOS flip-flops can attain leakage dissipation savings without additional dynamic power and silicon area.

Channel length biasing: For short channel transistors, with increasing of the gate length, the threshold voltage increases, so that the leakage power decreases exponentially and delay increases linearly (Gupta *et al*., 2006). Therefore, it is possible to slightly increase the gate length to take advantage of the exponential leakage reduction, while the performance is impaired only linearly. In a 130-nm industrial process, it is reported that an 8 nm increase in gate length yields 30% decrease in leakage with a 5% increase in delay for a minimum size inverter (Gupta *et al*., 2006). The channel length biasing increases the channel length of transistors to alter the threshold voltage and reduces leakage exponentially in both active and standby modes, while delay increases linearly with increasing gate length. Based on this principle, the gate-length biasing technique for flip-flops has been reported.

Compared with other techniques, channel length biasing reduces leakage currents without additional manufacturing cost. However, considering the balance of the leakage power consumption and delay, the reduction magnitude of the leakage dissipations is limited. In another word, in order to reduce effectively leakage dissipations, the gate-length biasing flip-flop would cause a large delay penalty.

LOW LEAKAGE FLIP-FLOPS

Flip-flops are critical components in digital systems that contribute an appreciable proportion of the total

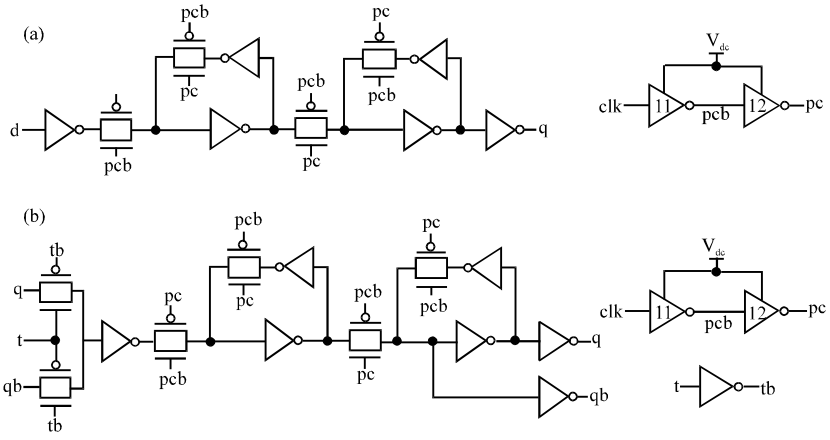

Fig. 1(a-b): Transmission-gate flip-flop (TG FF): (a) D flip-flop and (b) T flip-flop

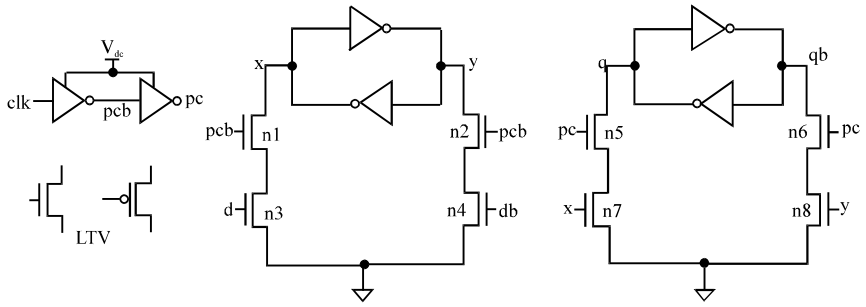

Fig. 2: CMOS ratioed D flip-flop

leakage dissipation. The delay of the flip-flops is also an important parameters associated with performance of the digital systems. There are three important timing parameters associated with a flip-flop: setup time (T_{D-C}), hold time (T_{hold}) and propagation delay (T_{C-Q}). The input (D) must valid before the clock triggering edge and T_{D-C} is the time difference between input (D) and clock. T_{hold} is the time that the input (D) must remain valid after the clock edge. T_{C-Q} is the time difference between the output (Q) and the clock edge. Assuming T_{hold} is met, the delay of a flip-flop can be expressed as the time difference between input (D) and output (Q):

$$T_{D-Q} = \max(T_{D-C\ LH} + T_{C-Q\ LH}, T_{D-C\ HL} + T_{C-Q\ HL}) \quad (3)$$

where, $T_{D-C\ LH}$ and $T_{D-C\ HL}$ are low-to-high transition and high-to-low transitions time, and $T_{C-Q\ LH}$ and $T_{C-Q\ HL}$ are low-to-high and high-to-low propagation delay, respectively.

Another important metric is the power dissipation that includes three components: the internal power dissipation (P_{Vdd}), the clock driving power dissipation (P_{Vdc}) and the data driving power dissipation (P_{Vdi}). P_{Vdd} is the energy consumed for switching internal nodes and driving the output load capacitances of the flip-flop. P_{Vd} and P_{Vdi} are consumed by the clock and input data to drive the load on the clock and data inputs, respectively. All of these power dissipations include dynamic and leakage power.

The typical transmission-gate flip-flop (TG FF) is shown in Fig. 1 which is extensively used in sequential circuits because of its simple structure with reliable performance. Therefore, it is taken as a benchmark circuit for comparing performances with the proposed flip-flops.

A ratioed CMOS D flip-flop is shown in Fig. 2. In order to reduce leakage power of the flip-flop, a low leakage power CMOS ratioed (LLR) D flip-flop is proposed in this study, as shown in Fig. 3. The structure of the LLR latch is similar to the ratioed CMOS latch shown in Fig. 2 which consists of a cross-coupled inverter pair, evaluation transistors (n7, n8) to driving the latch from one state to another. Dual-threshold CMOS (DTCMOS) and channel length biasing techniques with power gating are used to reduce leakage power of the latch. A High-Threshold Voltage (HTV) gating transistor (p1) is inserted to cut the path from V_{dd} to ground in sleep mode, thus reduces the sub-threshold leakage current efficiently. The clamp transistors (n1 and n2) prevent the outputs from floating which use General-Threshold

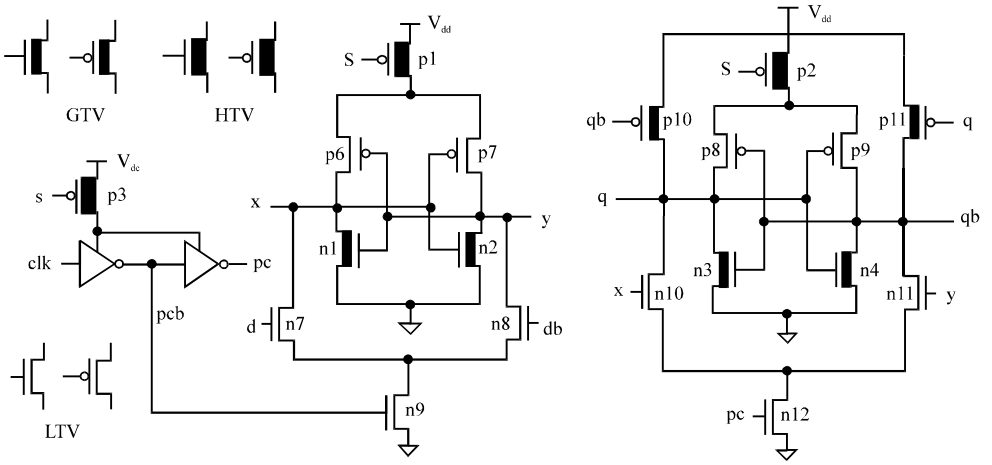

Fig. 3: Low leakage ratioed D flip-flop (LLR D FF)

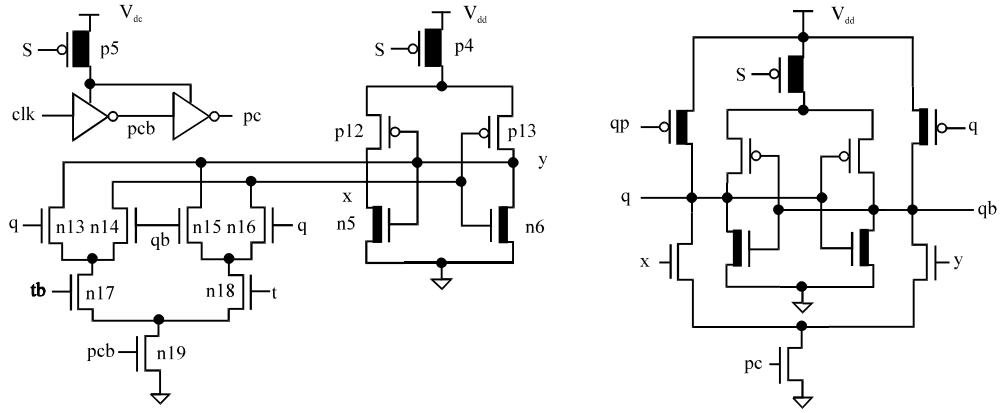

Fig. 4: Low leakage ratioed T flip-flop (LLR T FF)

Voltage (GTV) transistor to reduce leakage dissipation since they are in the non-critical path. The other transistors use Low-Threshold Voltage (LTV) device to keep performance, since they are in the critical path.

Figure 3 shows the low leakage power CMOS ratioed flip-flop based on the low leakage ratioed latches with the master-slave structure. The LLR D flip-flop consists two identical cascaded latches operating on complementary clocks. The inverters for driving clock inputs are also power-gated by inserting a HTV transistor to reduce leakage power in sleep mode. The hold transistors (p10 and p11) are paralleled to store values during sleep mode in the slave latch which use General-threshold Voltage (GTV) transistor to reduce leakage dissipation since they are in the non-critical path. With three extra transistors and various leakage reduction techniques, LLR D flip-flops can reach low leakage power dissipations.

The low leakage power CMOS ratioed T flip-flop can also be realized, as shown in Fig. 4. It consists of the cascaded LLR T latch and LLR D latch. The LLR T latch is similar to the D latch, only the input D is replaced with the input T with the XOR/XNOR of T and Q, as shown in Fig. 4. The LLR flip-flops are differential, complementary data inputs and outputs, while the TG flip-flop requires inverters to provide complementary inputs and outputs.

EXPERIMENTAL RESULTS

HSPICE simulations have been carried out for the proposed two low leakage flip-flops. All circuits are simulated with HSPICE at a NCSU PDK 45 nm technology (Zhao and Cao, 2006). In order to simulate the work environment of the flip-flops, the testing platform is shown in Fig. 5.

The delay and power dissipation of the circuits in the black box are tested. In order to assure the fairness of the comparisons, the four inverters are paralleled after all outputs to act as load capacitances and the same input is

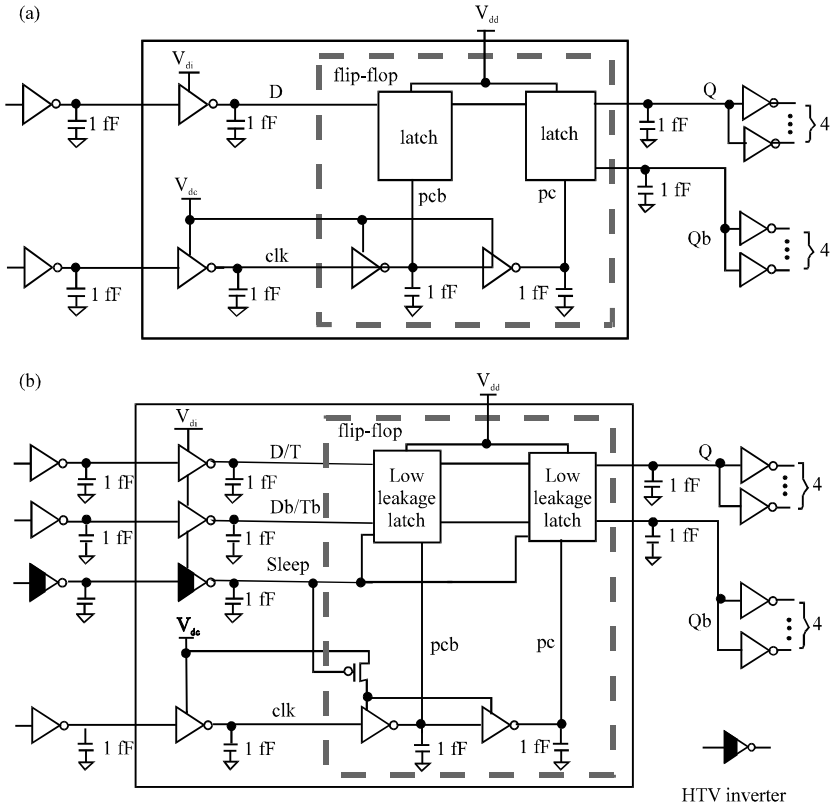

Fig. 5(a-b): Testing platform of the flip-flops; (a) TG filp-flop test circuit and (b) Low leakage D and T filp-flop test circut

given to these circuits. The different power supplies are offered to the flip-flops to test the P_{Vdd}, P_{Vdc} and P_{Vdi}, respectively.

A size optimization considering function and power has been carried out for the two flip-flops. In the TG FF, the minimum channel length of all the transistors is taken as L = 2γ = 0.05 μm and the sizes of all the PMOS and NMOS transistors are $W_P/L_P = 6\gamma/2\gamma$ and $W_N/L_N = 3\gamma/2\gamma$, respectively. The transistors sizes of the LLR flip-flops are shown in Table 1.

As shown Table 1, in the low leakage latch, all LTV transistors use the channel length biasing with a 10% increase. The channel length biasing reduces leakage exponentially in both of active and standby mode, while delay increases linearly.

Zero bias threshold voltage of the LTV transistors, GTV transistors and HTV transistors are shown in Table 2. The parameter of HTV transistor is nearly 1.8 times of LTV transistors.

Timing parameters, leakage power dissipation in sleep mode and active mode, total power consumptions of the LLR flip-flop have been compared with the TG flip-flop.

Table 1: Width length ratios of transistors in the LLR Flip-Flops

Transistors	P1-P5	P6-P13, N7-N12	N1-N6	N13-N19	N20-N27
W/L	24λ/2λ	6λ/2.1λ	3λ/2λ	9λ/2.1λ	6λ/2λ

Table 2: Zero bias threshold voltage of LTV and HTV transistors in the LLR Flip-Flops

	NMOS			PMOS		
Transistors	LTV	GTV	HTV	LTV	GTV	HTV
Vth0 (V)	0.471	0.677	0.853	-0.423	-0.622	-0.771

Timing parameter: Timing parameters of CMOS ratioed, TG and LLR flip-flops are shown in Table 3. The delay of the LLR D flip-flop is nearly 1.5 times of TG flip-flop due to using HTV gating transistor.

Leakage dissipations: Figure 6 shows the leakage power dissipations of the two flip-flops for different inputs in active mode and sleep mode. The leakage power dissipations of the D flip-flops are compared in Fig. 6a. Due to adopting leakage reduction techniques, the total average leakage power dissipation of the LLR D flip-flop can save 11.45% in active mode compared with the CMOS ratioed D flip-flop and can save 25.79% in sleep mode compared with the TG D flip-flop.

Table 3: Timing parameter comparisons of the flip-flops

		D flip-flops		T flip-flops	
Timing parameter	CMOS ratioed D FF	LLR D FF	TG D FF	LLR T FF	TG T FF
Rise (ps)	110.0	117.9	72.68	132.8	81.52
Fall (ps)	89.782	114.9	43.56	142.1	48.80
Delay (ps)	135.8	181.6	116.20	226.0	112.00

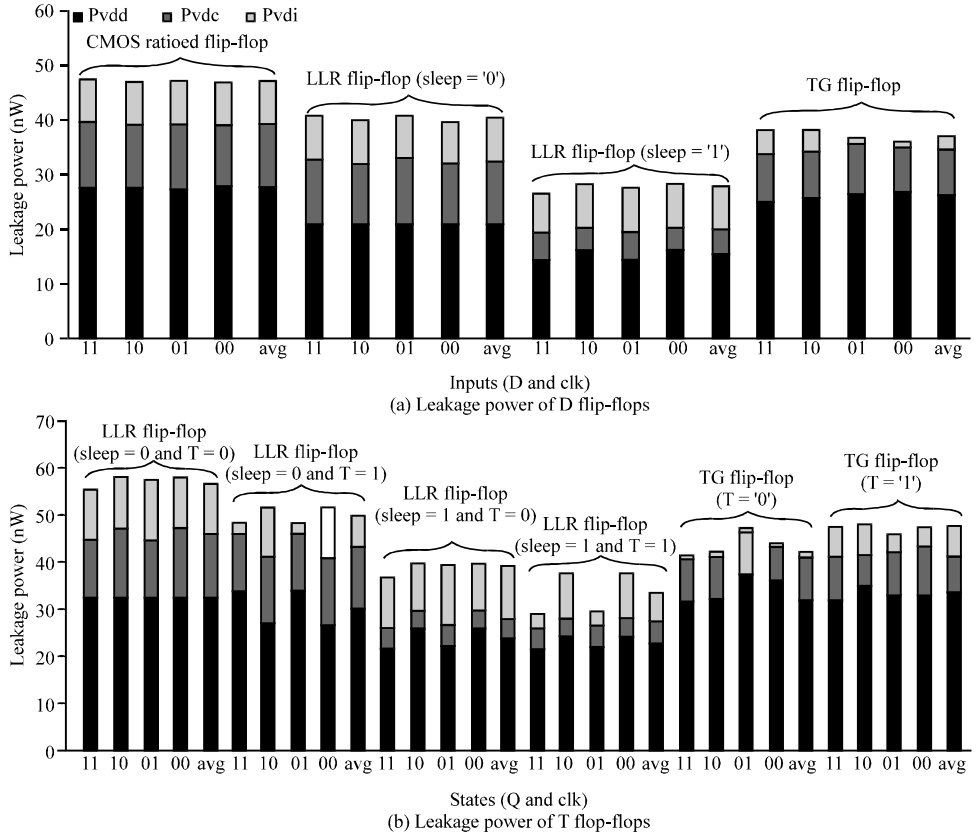

Fig. 6(a-b): Leakage power dissipations of the TG and LLR flip-flops for different inputs at 10MHz

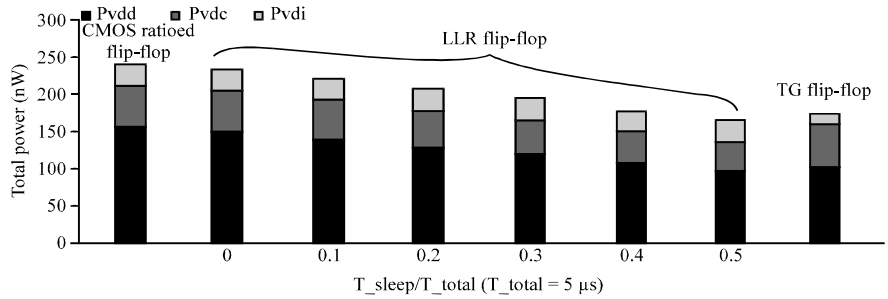

Fig. 7: Total power dissipations of the TG and LLR D flip-flops for different activities at 10MHz

Figure 6b shows the leakage power dissipation comparisons of the T flip-flops. For the LLR T flip-flop, the average leakage power dissipation in sleep mode can save 32.02% compared with in active mode and 19.15% compared with the TG T flip-flop.

Total power dissipations: The total power dissipations of the D and T flip-flops are shown in Fig. 7 and 8 for various activities, respectively. They are simulated for the total time (T-total = 5us) by varying the sleep time (T-sleep) from 0 to 2.5 us with 0.5 us steps. The cycle of input D is

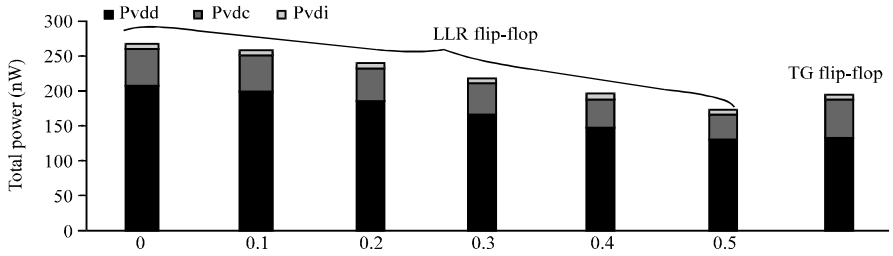

Fig. 8: Total power dissipations of the TG and LLR T flip-flops for different activities at 10MHz

twice of the cycle of input clk in the D flip-flop, while the input T keeps high in the T flip-flop.

The LLR flip-flop can save more total power dissipation where the system spends the majority of the time in sleep mode. Compared with the TG flip-flop, the LLR D and T flip-flop can save 5.04 and 10.57% total power dissipation, respectively when T-sleep is half of the T-total.

CONCLUSIONS

This study focuses on low leakage flip-flops. Dual-threshold CMOS (DTCMOS) and channel length biasing leakage reduction techniques are used for the flip-flops with power-gating scheme to reduce leakage power dissipations. Compared with the TG D flip-flop, due to adopting leakage reduction techniques, the total average leakage power dissipation of the LLR D flip-flop can save 11.45% in active mode compared with the CMOS ratioed D flip-flop and can save 25.79% in sleep mode compared with the TG D flip-flop. For the LLR T flip-flop, the leakage power dissipation of 19.15% can be saved in sleep mode compared with the TG one. Compared with the TG flip-flop, the LLR D and T flip-flops can save 5.04 and 10.57% of total power dissipations respectively when sleep time is half of total time. The proposed leakage power flip-flops can be used for ultra-low power applications.

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