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An Isolated Bridgeless Power Factor Correction Rectifier Based on SEPIC Topology

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Abstract: The conventional Power Factor Correction (PFC) rectifier based on BOOST topology is used only for the step-up output and has more conduction loss because of its dependency on the line power rectifier bridge. Present study has proposed a novel PFC rectifier based on Single-ended Primary Inductance Converter (SEPIC) and it presents the following desirable characteristics: (1) it works as an automatic voltage follower and theoretical power factor is unity; (2) no rectifier bridge results in less conduction loss and (3) the galvanic isolation and the current continuum bring the Electromagnetic-interface (EMI) low. Present study analyzes the operation of the propose rectifier working in Discontinuous Mode (DCM) in detail, the equations for the characteristic analysis and design are derived, as well as the large-signal model is given. The simulation results are presented to demonstrate the feasibility of the proposed technique.

Key words: Bridgeless rectifier, power factor correction (PFC), single-ended primary inductance converter (SEPIC), discontinuous mode (DCM)

INTRODUCTION

Both BOOST and BUCK topologies can be used as PFC rectifier and Yang *et al.* (2010) presents a detailed performance comparison between boost and buck type PFC. BOOST type PFC presents better current continuum and so it is used as PFC rectifier widely, however, the circuit decides that the output voltage must be higher than the input voltage which confines its use to high voltage applications or a DC/DC converter should be followed after PFC converter for low output voltage applications. Thus, recently many papers present research about SEPIC and CUK type PFC rectifiers because that their output can be not only step-up but also step-down, De Vicuna *et al.* (1989), Wong and Man (2010) and Simonetti *et al.* (1997) make a deep research about SEPIC and CUK topology. Except that, as PFC rectifier they also have such desirable characteristics: restraining the inrush current when starting, less ripple in the input current, low EMI and so on (Ismail, 2009).

The conventional PFC rectifier is shown as Fig. 1a and it is made up of rectifier bridge and DC-DC converter. It brings more loss because of more semiconductors in the flow of current, so bridgeless PFC rectifier is studied. Dual converters are mostly utilized as the bridgeless solution and work by turns as the input voltage alters between the positive voltage and the negative voltage. The dual BOOST topology is the most often used at present and Huber *et al.* (2008) presents a detail analysis and a comparison of various bridgeless rectifiers based on the BOOST topology which are shown in Fig. 1b-f. The MOSFET S_1 and the MOSFET S_2 conduct alternatively as the input voltage pole alters and at last positive voltage outputs. However, the circuit shown in the Fig. 1b presents high EMI performance because of floating of the input voltage. The EMI performance gets improved with two extra diodes and an extra inductor but it brings more loss. As shown in the Fig. 1c, the circuit gets low EMI by integrating the low recovery diodes and the fast recovery diodes and at the same time the same control signal can be used for the two MOSFETs to simply the control circuit. The circuit shown in the Fig. 1e works only in DCM or Critical Current Mode (CRM). The circuit shown in the Fig. 1f is used rarely because of the complexity of the circuit. However, all the circuit mentioned above get better performances than the conventional rectifier shown in the Fig. 1a but they cannot get rid of the limitation of the BOOST topology.

As SEPIC type PFC rectifier has many good performances, Ismail (2009), Sahid and Yatim (2011) and Sahid and Yatim (2010) present a deep research about bridgeless PFC rectifier integrated by dual SEPIC topologies. Ismail (2009) proposes a circuit as shown in the Fig. 2a and the components L_1, Q_1, D_{q2}, C_1, L_2, D_{O1} and C_{O1} compose a SEPIC circuit during the positive input, as well as the components L_1, Q_2, D_{q1}, C_2, L_3, D_{O2} and C_{O2} compose a SEPIC circuit during the negative input. The voltage drop between the voltage of C_{O1} and C_{O2} gives the output voltage and the capacitors C_{O1} and C_{O2} are charged only in a half line period and discharged in another half line period, so it needs a bulk capacitor to reduce output voltage fluctuation.

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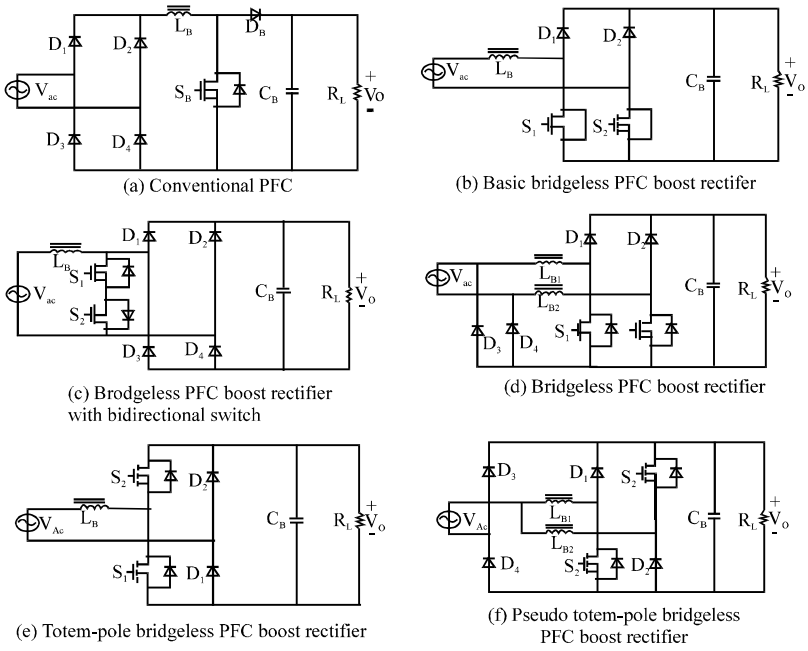


Fig. 1(a-f): Boost type PFC rectifier

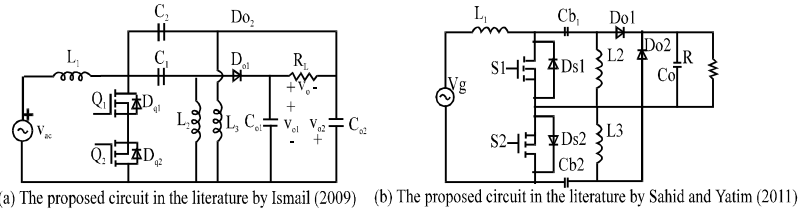


Fig. 2(a-b): Briggeless PFC rectifier based on SEPIC

Sahid and Yatim (2011) proposes a circuit as shown in the Fig. 2b and the components L_1, S_1, D_{S2}, C_{b1}, L_2, D_{O1} and C_O compose a SEPIC circuit during the positive input, as well as the components L_1, S_2, D_{S1}, C_{b2}, L_3, D_{O2} and C_O compose a SEPIC circuit during the negative input. The voltage of the capacitor CO gives the output voltage and such circuit can use less bulk capacitor but will produce high EMI. The literature (Sahid and Yatim, 2010) proposes an isolated bridgeless PFC circuit based on Fig. 2b.

Present study proposed a new bridgeless PFC rectifier based on the SEPIC topology, shown as the Fig. 3 and except that all the desirable performance of the bridgeless SEPIC PFC rectifier, this circuit has also such desirable characteristics: (1) less component compared with the circuits proposed in the literatures (Ismail, 2009; Sahid and Yatim, 2011, 2010);(2) lower EMI compared with the circuits proposed in the literatures (Sahid and Yatim, 2011, 2010) and (3) galvanic isolation between the input and the output.

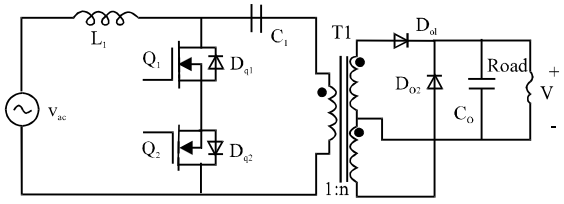
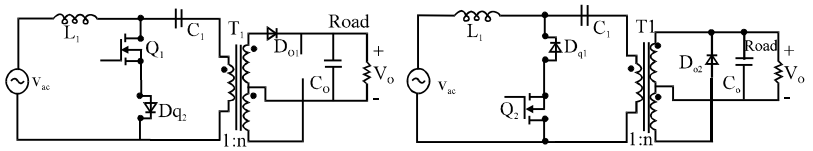


Fig. 3: The proposed bridgeless rectifier

Operating principles of the proposed rectifier: The proposed PFC rectifier is shown as Fig. 3. The theoretical analysis of the rectifier is made during one switching period in a positive half-period of the input voltage under the flowing assumptions:

- All the components are ideal that the efficiency is 100%
- The input voltage is considered constant during one switching period because the switching frequency is much higher than the ac line frequency



(a) Operation of the proposed circuit during ac positive line cycle

(b) Operation of the proposed circuit during ac negative line cycle

Fig. 4(a-b): Operation of the proposed circuit

- All the capacitors are big enough such that switching ripples can be negligible
- The turns ratio of the transformer, n< V_O/V_P, V_P is the peak value of the input voltage, so that the diode switch off during the MOSFET conducts

As shown in the Fig. 4a, during positive ac line cycle the MOSFET and diode, Q_1-D_{q2}, conduct and the diode D_{O2} switches off. As shown in the Fig. 4b, during negative ac line cycle the MOSFET and diode, Q_2-D_{q1}, conduct and the diode D_{O1} switches off. Because the MOSFETs Q_1 and Q_2 are in series with different direction, the MOSFETs can be driven with the same signal and only one works. The proposed circuit operates in DCM which means that during one switching period there three stages:

- Stage 1[0-dT_S]

This stage is the time, t_{on}, when the MOSFET conducts. Before that the MOSFET and the diode all switch off and the inductor L_1, the capacitor C_1, the primary inductor Lp of the transformer T_1 and the input source v_{ac} compose a current loop and the current is the freewheeling current, i_{fw}. The capacitor C_O is discharged by the load resistor. Assuming that the MOSFET switches on at the time zero, now the operation of the proposed circuit is shown as Fig. 5a. The diodes at secondary side of the transformer switch off and the primary winding presents a pure inductor, Lp. Thus, such circuit works with three current loops: the input source and the capacitor, C1, charge inductors, L1 and Lp, separately and the capacitor is discharged by the load continuously. The currents flow through the inductors as shown in the Fig. 6 during the ton. The inductor currents are defined as:

$$i_{L1} = i_{fw} + \frac{v_{ac}}{L_1} t \quad (1)$$

$$i_{Lp} = -i_{fw} + \frac{v_{ac}}{L_p} t \quad (2)$$

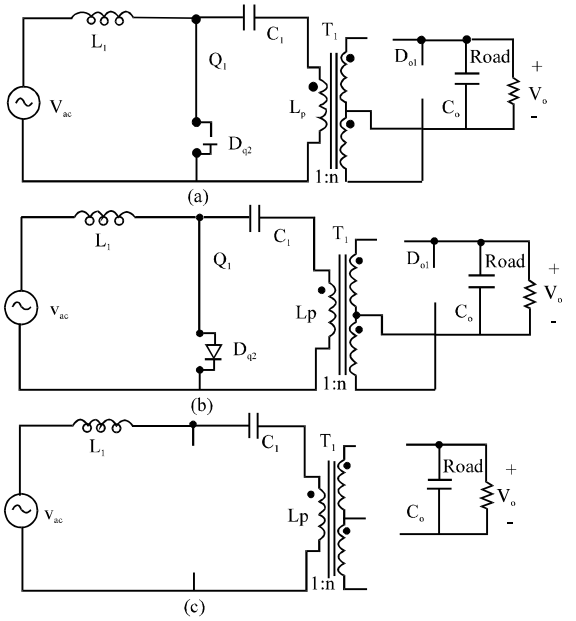


Fig. 5(a-c): Operation of the proposed circuit in the stage 1

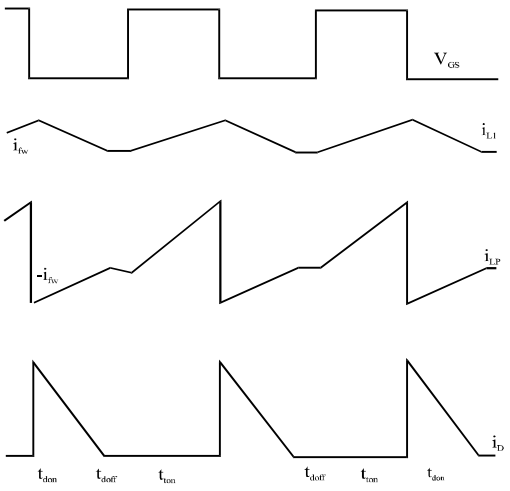


Fig. 6: The currentwaveform

The MOSFET current is defined as:

$$i_Q = i_{L1} + i_{Lp} = \frac{v_{ac}}{L_p}t + \frac{v_{ac}}{L_1}t = \frac{v_{ac}t}{L_{eq}} \quad (3)$$

where:

$$L_{eq} = \frac{L_1 \times L_P}{L_1 + L_P}$$

- Stage 2[t_{don}]

This stage is the time, t_{don}, when the second side diode conducts and the MOSFET switches off. The operation is shown as Fig. 5b. Now the inductor currents begin to decrease as shown in the Fig. 6 during the time, t_{don}. The power stored in the inductors is transferred to the capacitor CO and load through the transformer and the diode, DO1, thus, the current through the DO1 is the sum of the currents coupled with the inductor power. The inductor currents are defined as:

$$i_{L1} = -i_{Lp} = i_{fw} + \frac{v_{ac}}{L_1}dT_S - \frac{V_O}{nL_1}t \quad (4)$$

The current produced by the power stored by the primary inductor current, Lp, during the time, t_{on}, is defined as:

$$i_D' = -\frac{1}{n}i_{fw} + \frac{v_{ac}}{nL_p}dT_S - \frac{V_O}{n^2L_p}t \quad (5)$$

So the diode current:

$$i_D = i_D' + \frac{i_{L1}}{n} = \frac{v_{ac}}{nL_{eq}}dT_S - \frac{V_O}{n^2L_{eq}}t \quad (6)$$

The diode current decreases and it reaches 0 when this stage finishes. So substituting Eq. 6 into $i_D = 0$ gives:

$$t_{don} = \frac{nv_{ac}}{V_O}dT_S \quad (7)$$

- Stage 3[t_{off}]

The MOSFET and the diode all switch off and the inductor L_1, the capacitor C_1, the primary inductor Lp of the transformer T_1 and the input source v_{ac} compose a current loop and the current is the freewheeling current, i_{fw}. The capacitor C_O is discharged by the load resistor. This stage lasts:

$$t_{off} = T_s - dT_s - t_{don} \quad (8)$$

ANALYSIS AND MODELING OF THE PROPOSE RECTIFIER

The average current of the diode during a switching period: According to Eq. 6 and 7, the average current of diode is given in a switching period:

$$I_{do,avg} = \frac{1}{2}\bullet\frac{v_{ac}}{nL_{eq}}dT_S\bullet\frac{nv_{ac}}{V_O}dT_S\bullet\frac{1}{T_S} = \frac{v_{ac}^2}{2L_{eq}V_O}d^2T_S \quad (9)$$

The average input current during a switching period: The average input current is that flowing through the inductor L1 during a switching period. According to the Eq. 1, 4 and 7, the average input current is given:

$$\begin{aligned} I_{in,avg} = I_{L1,avg} &= i_{fw} + \frac{1}{2}\bullet\frac{v_{ac}}{L_1}dT_S \\ &\bullet\left(dT_S + \frac{nv_{ac}}{V_O}dT_S\right)\bullet\frac{1}{T_S} = i_{fw} + \frac{1}{2}\left(1 + \frac{nv_{ac}}{V_O}\right)\frac{v_{ac}}{L_1}d^2T_S \end{aligned} \quad (10)$$

The output power equals to the input power under the assumption of the ideal components which means that

$$v_{ac}\bullet I_{in,avg} = V_O\bullet I_{do,avg} \quad (11)$$

Substituting Eq. 9 and 10 into Eq. 11, the freewheeling current is given:

$$i_{fw} = \frac{v_{ac}}{2L_p}d^2T_S - \frac{1}{2}\frac{nv_{ac}^2}{L_1V_O}d^2T_S \quad (12)$$

Substituting Eq. 12 into Eq. 10:

$$I_{in,avg} = I_{L1,avg} = \frac{d^2T_S}{2L_{eq}}v_{ac} \quad (13)$$

The input resistance is given:

$$R_{eq} = \frac{2L_{eq}}{d^2T_S} \quad (14)$$

It is shown that the input current follows the input voltage automatically in the proposed circuit from the Eq. 13 and the power factor is unity in the theory.

The voltage conversion ratio: The Eq. 9 can be derived as the following:

$$I_{do,avg} = \frac{v_{ac}^2}{2L_{eq}V_O} d^2T_S = \frac{V_p^2 d^2 T_S}{2L_{eq}V_O}\sin^2(\omega t) = \frac{V_p^2 d^2 T_S}{4L_{eq}V_O} - \frac{V_p^2 d^2 T_S}{4L_{eq}V_O}\cos(2\omega t) \quad (15)$$

where $v_{ac} = V_p \sin \omega t$, ω is the angular frequency of input voltage.

From the Eq. 15 the DC value and the AC value of the diode current are given:

$$I_{dodc} = \frac{V_p^2 d^2 T_S}{4L_{eq}V_O} \quad (16)$$

$$I_{doac} = -\frac{V_p^2 d^2 T_S}{4L_{eq}V_O}\cos(2\omega t)) \quad (17)$$

Because of the integral of the capacitor C_O, the power transferred to the load is produced by the DC value of the diode current. So:

$$I_{dodc} = \frac{V_p^2 d^2 T_S}{4L_{eq}V_O} = \frac{V_O}{R_{load}} \quad (18)$$

From Eq. 14 and 18, we can get:

$$M = \frac{V_o}{V_p} = \sqrt{\frac{d^2 T_S R_{load}}{4L_{eq}}} = \sqrt{\frac{R_{load}}{2R_{eq}}} \quad (19)$$

$$d = \sqrt{\frac{4L_{eq}M^2}{T_S R_{load}}} = 2M\sqrt{\frac{L_{eq}}{T_S R_{load}}} \quad (20)$$

$$L_{eq} = \frac{d^2 R_{load}}{4f_S M^2} \quad (21)$$

Boundary between DCM AND CCM: Figure 7 shows that the boundary of DCM and CCM is that t_{off} reaches zero, so if the proposed circuit works in DCM the following equation should be satisfied:

$$dT_s + t_{don} = dT_s + \frac{nv_{ac}}{V_O} dT_S < T_S \Rightarrow d < \frac{M}{M + n\sin\omega t} \quad (22)$$

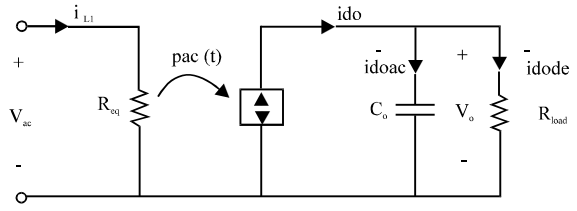


Fig. 7: Large-single model of the proposed circuit

Thus, if the proposed circuit works in DCM all the time the following equation should be satisfied:

$$d < \frac{M}{M+n} \quad (23)$$

Large-signal model: According to the Eq. 9, 10, 14-16 and 17, the large-signal model of the proposed circuit can be got (Ismail, 2009). It is shown as Fig. 6.

DESIGN PROCEDURE AND SIMULATION

According to the specification, a simplified design procedure is presented in this section. Suppose that the specifications of the power stage are given in the Table 1.

From aforementioned equation and assumption that the efficiency is 100%, the critical components are calculated as following.

The voltage conversion ratio M is:

$$M = \frac{V_o}{V_p} = \frac{200}{\sqrt{2}220} = 0.645$$

According to:

$$n < \frac{V_O}{V_P},$$

turns ratio of the transformer is chosen: 1:n = 2:1;

The resistance of the load is:

$$R_{load} = \frac{V_O^2}{P} = \frac{200^2}{120} = 333\Omega$$

According to the Eq. 23:

$$d < \frac{M}{M+n} = \frac{0.645}{0.645+0.5} = 0.56$$

To assure DCM operation, the following value is chosen: d = 0.5;

According to the Eq. 21:

$$L_{eq} = \frac{0.5^2 \times 333}{4\times10^5 \times 0.645^2} = 500uH$$

Table 1: The specification of the power circuit

Input voltage	Input voltage frequency	Output voltage	Output power	Maximum input current ripple	Switching frequency	Output voltage ripple
$220V_{rms}$	50Hz	$200V_{dc}$	120W	20% of $I_{in,avg}$	100KHz	±1% of V_O

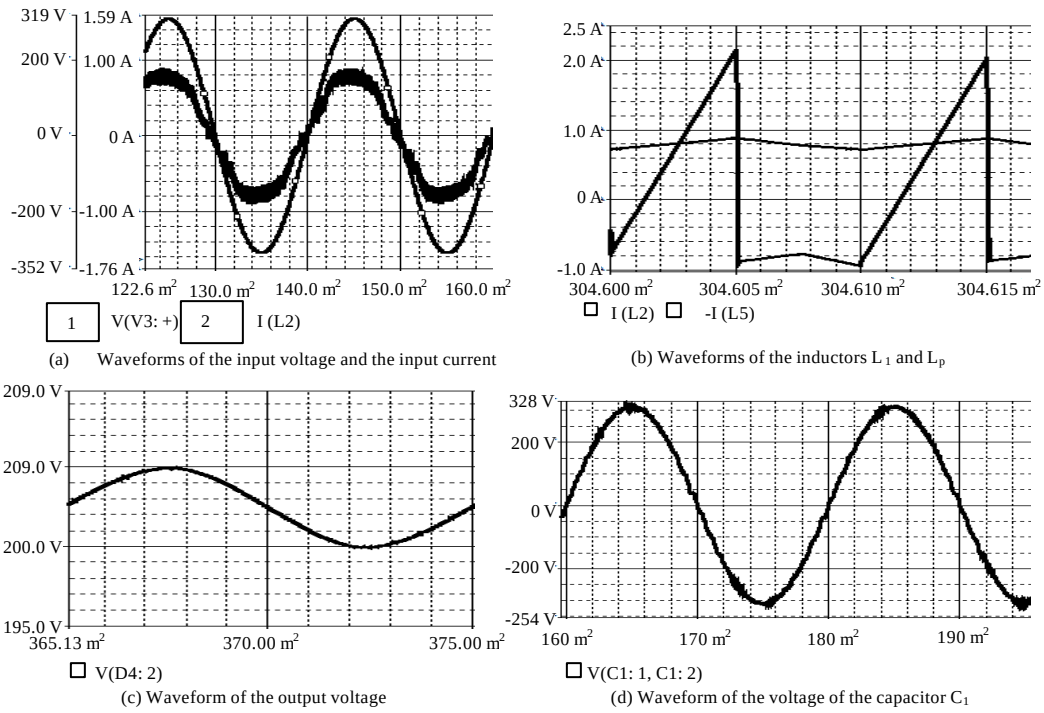


Fig. 8(a-d): Simulation result

Input current ripple:

$$\Delta i_{L1} = 20\% \times \frac{V_P}{R_{eq}} = 20\% \times \frac{V_P d^2 T_S}{2L_{eq}} = 0.2 \times \frac{311 \times 0.5^2 \times 10^{-5}}{2 \times 0.5 \times 10^{-3}} = 0.16A$$

According to the Eq. 1:

$$L_1 = \frac{V_p}{\Delta i_{L1}} dT_S = \frac{220\sqrt{2}}{0.16} \times 0.5 \times 10^{-5} = 9.75mH$$

Thus:

$$L_p = \frac{L_1 \bullet L_{eq}}{L_1 - L_{eq}} = \frac{9.72 \times 0.5}{9.72 - 0.5} = 527uH$$

A low-frequency oscillation will occur if the capacitance of the coupling capacitor C_1 is too large. Otherwise, the voltage of the capacitor cannot follow the input voltage (Simonetti *et al*., 1997). Thus, through simulation, the capacitor C_1 is chosen to be 1 μF.

Figure 8 presents the simulation results. Figure 8a shows the waveforms of the input voltage and the input current and by the waveforms it is verified that the input current follows the input voltage automatically and the input current has good continuous performance when the proposed circuit works in DCM. Figure 8b shows the waveforms of the inductors L1 and Lp, and it can be seen that the input current ripples are less than 0.16A. Figure 8c shows the waveforms of output voltage and it is seen that there are voltage fluctuation with the 100 Hz frequency because of the limitation of the practical capacitor C_O. As shown in Fig. 8d, the waveforms of the voltage of the coupling capacitor C_1 shows that it nearly follows the input voltage.

CONCLUSION

This study proposes an isolated bridgeless PFC rectifier based on the SEPIC topology and it has the simpleness and isolation performance compared with conventional bridgeless SEPIC type PFC circuits. A detail analysis is given and the theoretical analysis is verified through simulation. The analysis and simulation results illuminate that the proposed circuit is a perfect PFC rectifier with the desirable characters that input current naturally follows the input voltage and the theoretical power factor is one.

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