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Adiabatic Computing for CMOS Integrated Circuits with Dual-threshold CMOS and Gate-length Biasing Techniques

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Abstract: Energy dissipation has become a major consideration concern in portable computers. With sizes of MOS transistors scaling down in nanometer CMOS circuits, the leakage dissipation catches up with the dynamic power consumption gradually and it is becoming an important factor for computer hardware. In present study, an improved effective charge recovery logic (I-ECRL) is proposed. In order to reduce sub-threshold leakage dissipations, adiabatic computing with dual-threshold CMOS (DTCMOS) and gate-length biasing techniques are used for I-ECLR circuits. The I-ECRL flip-flops are also presented. An ISCAS s27 benchmark circuit from the ISCAS85 benchmark set is verified. All circuits are simulated with HSPICE using a NCSU 45 nm process. Results show that both leakage and dynamic dissipations of the I-ECRL circuits with dual-threshold CMOS and gate-length biasing techniques are reduced greatly compared with the conventional CMOS circuits.

Key words: Adiabatic computing, low leakage design for computer hardware, nanometer circuit

INTRODUCTION

With technology improvement, power dissipation in computer hardware has become one of the most important factors. It is well known that the short-circuit dissipations, leakage dissipations and dynamic switching power dissipations are three main components of power consumptions in CMOS chips (Fallah and Pedram, 2005). In previous studies of low-power integrated circuits, the dynamic power consumption is the most concern. Adiabatic computing (also known as charge recovery logic) utilizes AC power clock to recover effectively the charge delivered by the clock instead of being dissipated to the ground. In order to reduce dynamic power consumption, many new logic circuits based on adiabatic computing, such as Complementary Pass-transistor Adiabatic Logic (CPAL) (Hu *et al*., 2005), Clocked Adiabatic Logic (CAL) (Maksimovic *et al*., 2000), Effective Charge Recovery Logic (ECRL) (Moon and Jeong, 1996) have been proposed. They all obtained significant dynamic energy dissipations savings by recycling the energy stored in circuit nodes.

With the feature size continuing to reduce, the leakage dissipation caused by leakage catches up with the dynamic power consumption gradually (Fallah and Pedram, 2005). There are several leakage sources in nanometer CMOS processes: Sub-threshold leakage current, gate leakage current and band-to-band tunneling leakage current (Agarwal *et al*., 2004). Sub-threshold leakage currents are the main sources of static power consumptions in recent nanometer CMOS processes (Agarwal *et al*., 2004). Several leakage reduction techniques, such as Dual-Threshold CMOS (DTCMOS), Multi-Threshold CMOS (MTCMOS) power-gating technique, stacking transistor techniques, Variable Threshold CMOS (VTCMOS) and Input Vector Control (IVC) have been proposed to reduce sub-threshold leakage (Abdullah *et al*., 2004; Kim *et al*., 2007; Gupta *et al*., 2006).

The dynamic power dissipation of adiabatic logic circuits can be reduced effectively by using adiabatic computing for node capacitances. However, the previously proposed leakage reduction techniques focus mainly on conventional CMOS circuits. In adiabatic circuits, there also exist leakage dissipations similar to the traditional CMOS circuits (Zhang *et al*., 2010). To the best of our knowledge, the logic circuits based on adiabatic computing with DTCMOS and gate-length biasing techniques have not been presented. In present study, an improved Effective Charge Recovery Logic (I-ECRL) based on adiabatic computing with dual-threshold CMOS (DTCMOS) and gate-length biasing techniques is proposed. In the I-ECRL circuits, combinational logic blocks are supplied by a single-phase power clock, while flip-flops are driven with two-phase non-overlap power clocks. In order to reduce sub-threshold leakage dissipations, DTCMOS and gate-length biasing technique are used for the I-ECLR circuits. The I-ECRL flip-flops are also presented. An ISCAS s27 benchmark circuit using DTCMOS and gate-length biasing techniques is verified.

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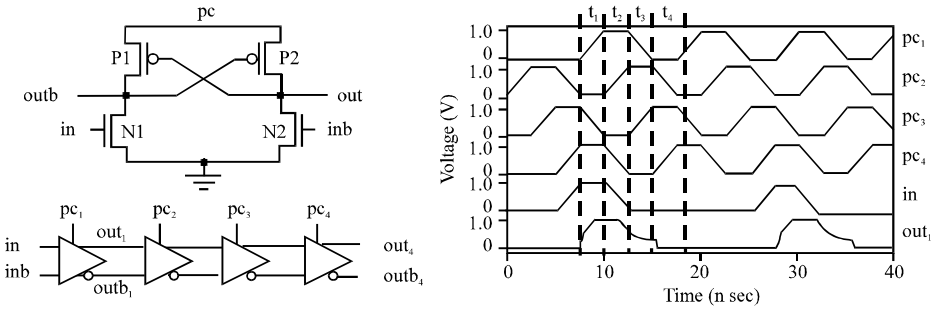

Fig. 1: ECRL buffer/inverter and its four-phase power clocks

REVIEW OF ECRL CIRCUITS

The schematic of the basic Efficient Charge Recovery Logic (ECRL) buffer/inverter is shown in Fig. 1 (Moon and Jeong, 1996). An ECRL circuit consists of PMOS loads and NMOS pull-down transistors. The cross-coupled PMOS transistors are used for pre-charge and evaluation. The ECRL uses four-phase power clocks to recover the charge delivered by the power clock. Each clock is followed by the next clock with a 90° phase lag. For the purpose of discussion here, the power clocks use trapezoidal waveforms.

The operation of the ECRL circuits can be divided four processes: evaluation (t_1), hold (t_2), recovery (t_3) and wait phases (t_4). For convenience, we assume (in) is at high and (inb) is at low at the beginning of a cycle (Fig. 1) and so that (outb) is clamped to GND. During the evaluation phase, as the clock pc_1 goes up, the output out goes high via P1 by the rising pc_1. When pc_1 reaches V_{DD}, the outputs hold valid logic levels. These values are maintained during the hold phase and used as inputs for evaluation of the next stage. After the hold phase, pc_1 falls down to a ground level and out node returns its energy to pc_1, so that the delivered charge is recovered. Thus, the power clock pc_1 acts as both a clock and power supply. Wait phase is inserted for clock symmetry. In this phase, valid inputs are prepared in the previous stage. When the previous stage is in the hold phase, the next stage must evaluate logic value in the evaluation phase.

IMPROVED ECRL CIRCUITS BASED ON ADIABATIC COMPUTING

The ECRL circuits use four-phase power clocks. The problems of multi-phase clocking charge recovery circuits include clock skew, complicated power-clock tree and multiple power-clock generators that increase energy dissipation (Maksimovic *et al*., 2000). Moreover, in order to maintain pipeline operation, some buffers must be inserted in ECRL circuits which result in extra area overhead and increase the complexity of the layout place and route. In this section, an improved Effective Charge Recovery Logic (I-ECRL) is proposed and flip-flops based on I-ECRL are also presented.

The structure of improved ECRL circuits (Fig. 2a) and their power clocks are shown in Fig. 2b. In the I-ECRL circuits, combinational logic blocks are supplied by a single-phase power clock, while flip-flops are driven with two-phase non-overlap power clocks, as shown in Fig. 2a. These power clocks can easily be generated by a simple power-clock generator (Maksimovic and Oklobdzija, 1995).

Figure 3 shows the I-ECRL buffer/inverter and simulated waveforms. The schematic of the I-ECRL circuit is the same as ECRL. All combinational logic blocks of the I-ECRL circuits are driven by a single-phase power clock which is unlike as the basic ECRL ones. For the purpose of discussion here, the single-phase power clock uses triangular waveforms.

The operation of the I-ECRL can be divided two processes: Evaluation (t_1) and recovery (t_2). For convenience, we assume in is at high and inb is at low (Fig. 3). During evaluation phase, outb is clamped to GND. As clk_1 goes up, the output out goes high via P1 by the rising pc_1. When pc_1 reaches V_{DD}, the outputs are used as inputs for evaluation of next stage. During the recovery phase, pc_1 falls down to a ground level and out node returns its energy to pc_1, so that the delivered charge is recovered.

The I-ECRL combinational logic gates can be realized by using NMOS function blocks to replace the input NMOS (N1 and N2) of the I-ECRL buffer/inverter. The two-input AND/NAND, OR/NOR, multiplexer and XOR/XNOR gates based on I-ECRL are shown in Fig. 4.

Flip-flops are important elements in digital circuits. In the adiabatic circuits, when power clocks fall from the peak voltage to ground, the output signals are set to zero level, thus a signal is stored difficultly. In the ECRL circuits, the four-phase clocking scheme is used.

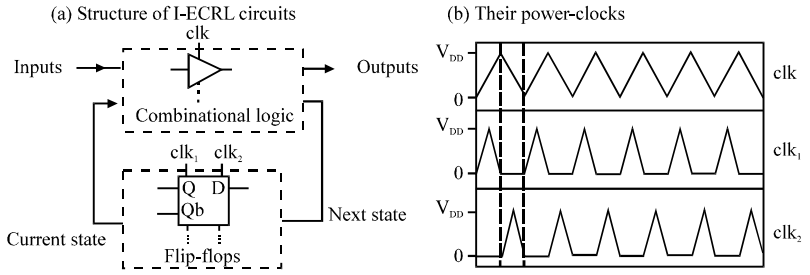

Fig. 2 (a-b): Structure of improved ECRL circuits and their power clocks

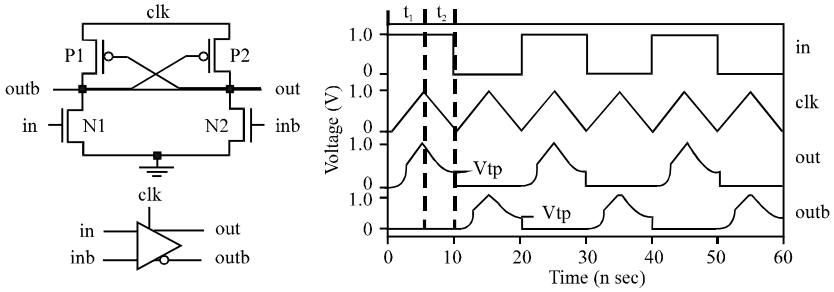

Fig. 3: I-ECRL buffer/inverter and simulated waveforms

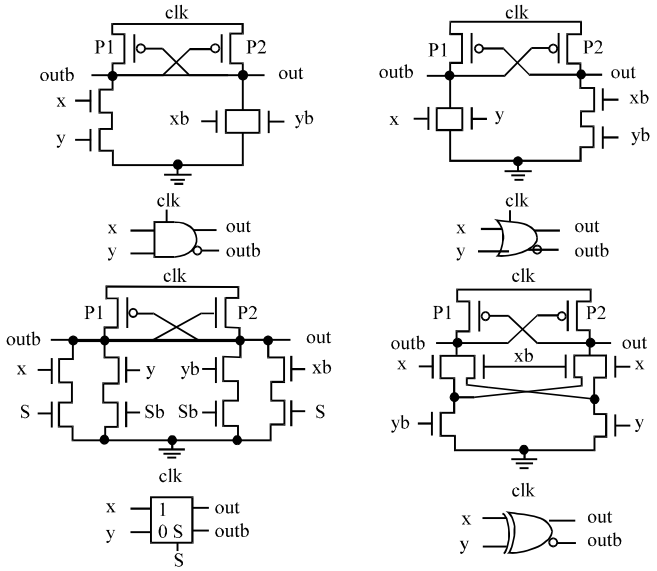

Fig. 4: AND/NAND, OR/NOR, multiplexer and XOR/XNOR gates based on I-ECRL

Therefore, the input in is just shifted to the output out_4 through the four-stage buffer chain by one clock period (Fig. 1) and thus the flip-flop based on ECRL was structured using a four-stage buffer chain (Moon and Jeong, 1996).

In the I-ECRL circuits (Fig. 3), during the recovery phase, as the voltage of the power clock clk approaches V_{tp} (threshold voltage of PMOS transistors), the PMOS transistor P2 gets turned off and the recovery path to the power clock is disconnected. When the power-clock clk is set to low level, a level of V_{tp} is stored at out node of the I-ECRL circuit. Based on this principle, the D flip-flop using I-ECRL circuits can be realized by two-stage I-ECRL buffer chain, as shown in Fig. 5.

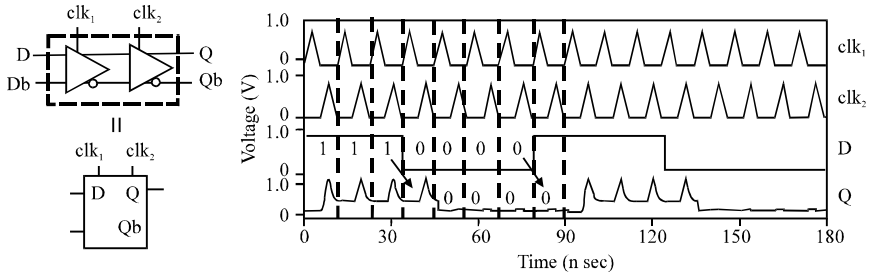

Fig. 5: D flip-flop based on I-ECRL and simulated waveforms

Simulated waveforms for the I-ECRL flip-flop are also shown in Fig. 5. The input D is just shifted to the output Q through the two-stage buffer chain by one clock period, as shown in Fig. 5. Obviously, I-ECRL flip-flop uses less transistor count than ECRL one.

LEAKAGE REDUCTIONS OF I-ECRL CIRCUITS

Power dissipation is a key factor of limiting circuit performances. In previous studies, the dynamic power consumption is the most concern and leakage dissipation is often neglected. However, with the feature size of integrated circuits continuing to reduce, the leakage dissipation caused by leakage currents catches up with the dynamic power consumption gradually and it is becoming an important factor in low-power design. Although, the dynamic energy consumption of the adiabatic circuit is lower than conventional CMOS ones, its leakage energy consumption is still worth to attention.

For short channel transistors, with increasing of the gate length, the threshold voltage increases, so that the leakage power decreases exponentially and delay increases linearly. Therefore, it is possible to slightly increase the gate length to take advantage of the exponential leakage reduction, while the performance is impaired only linearly. Therefore, increasing gate lengths slightly can decrease leakage dissipation effetely, while circuit performance only has little effect. In a 130 nm industrial process, it is reported that an 8 nm increase in gate length yields 30% decrease in leakage with a 5% increase in delay for a minimum size inverter (Gupta *et al*., 2006). Based on this principle, the gate-length biasing technique for I-ECRL basic gates can be realized, as shown in Fig. 6. The gate length of the PMOS transistors (P1, P2) is designed with larger sizes.

The sub-threshold leakage current increases exponentially with threshold voltage (Agarwal *et al*., 2004). For a typical technology with a sub-threshold slope

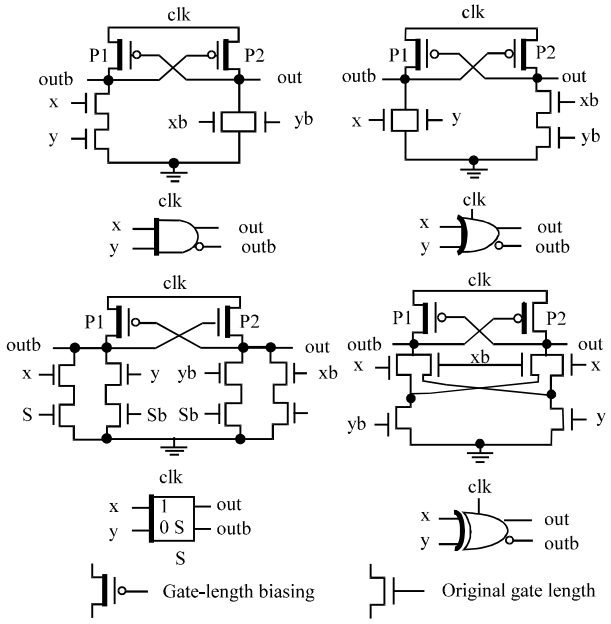

Fig. 6: AND/NAND, OR/NOR, multiplexer and XOR/XNOR gates based on I-ECRL with gate-length biasing

of 100 mV/decade, each 100 mv reduction in V_t will cause an order of magnitude increase in leakage currents. Therefore, increasing the threshold voltage can reduce leakage dissipations. The dual-threshold CMOS technique uses high-V_t devices to reduce leakage currents, while low-V_t devices are used to obtain high performance (Fallah and Pedram, 2005). Therefore, critical and non-critical regions must be identified.

The DTCMOS for the I-ECRL basic gates can be realized, as shown in Fig. 7. In order to reduce sub-threshold leakage currents via the power clock, the PMOS transistors (P1, P2) use high-V_t devices. These DTCMOS gates can be used in non-critical regions of a circuit to reduce sub-threshold leakage dissipations.

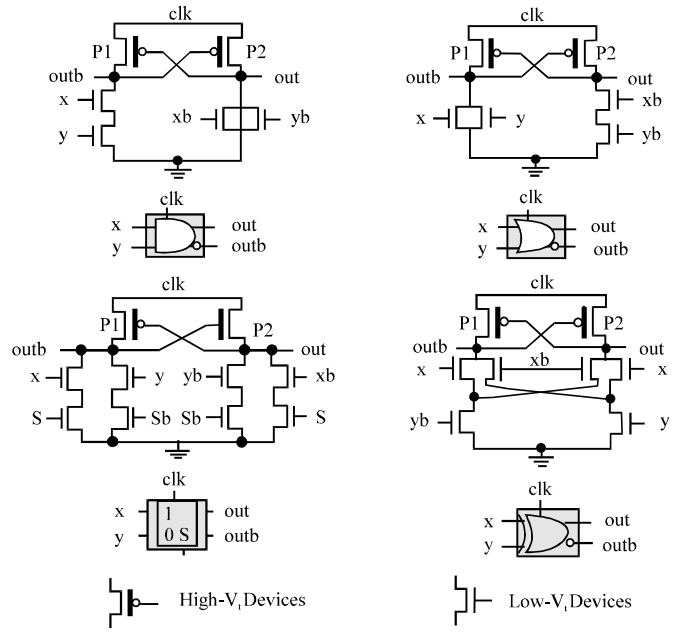

Fig. 7: AND/NAND, OR/NOR, multiplexer and XOR/XNOR gates based on I-ECRL using DTCMOS

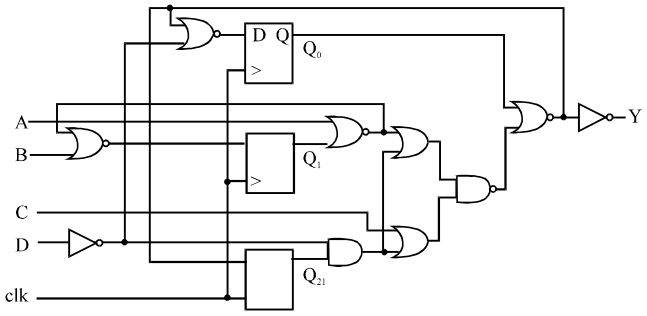

Fig. 8: Sequential benchmark s27 of ISCAS'89 based on conventional CMOS

ENERGY CONSUMPTION COMPARISONS

Here, the energy dissipations of basic I-ECRL and I-ECRL using DTCMOS and gate-length biasing techniques are compared with conventional CMOS logic circuits. All circuits are simulated with HSPICE using a NCSU 45 nm technology (Zhao and Cao, 2006). The peak-peak voltage (V_{DD}) of I-ECRL circuits are taken with 1.0V. Taken as an example, An ISCAS s27 benchmark circuit from ISCAS'89 is verified. The schematic of s27 benchmark circuit based on conventional CMOS is shown in Fig. 8. In conventional s27 implementation, all gates are realized with complementary static CMOS logic and flip-flop is realized with conventional CMOS transmission gate.

Basic I-ECRL circuits: The energy dissipations of the D flip-flop based on I-ECRL have been compared with conventional one based on CMOS transmission gate and is tabulated in Table 1. The I-ECRL flip-flop attains 77.5 to 85.9% energy savings compared with the one using the conventional logic. The energy dissipations of the I-ECRL flop-flop are greatly reduced compared with the conventional implementation because its dynamic power dissipation can be reduced effectively by recycling the energy of node capacitances. Moreover, the transistor count of the I-ECRL flip-flop is much less than conventional CMOS transmission one, so that the I-ECRL flip-flop dissipates less energy.

Based on the adiabatic D flip-flop and gates, complex adiabatic sequential circuits can also be realized. Figure 9 shows the schematic of the s27 based on I-ECRL circuits.

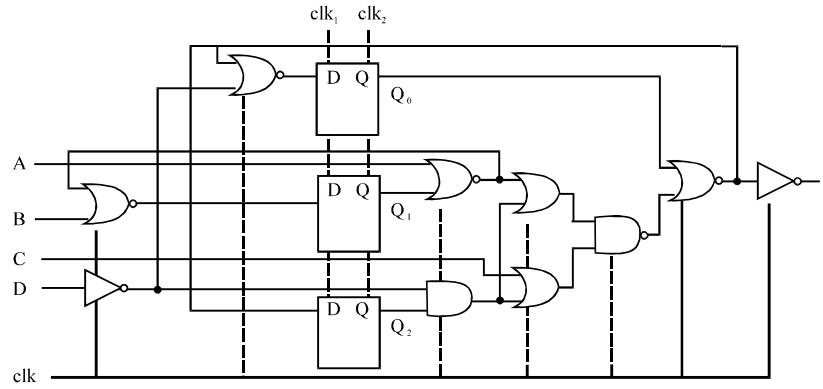

Fig. 9: Sequential benchmark s27 based on I-ECRL circuits

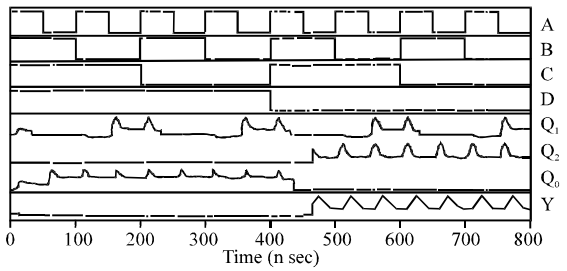

Fig. 10: Simulated waveforms of sequential benchmark s27 based on I-ECRL

Table 1: Energy consumption comparisons of the flip-flop based on I-ECRL and conventional CMOS

	Energy consumption per cycle (fJ)		
Frequency (MHz)	Conventional CMOS	I-ECRL	Saving rate (%)
5	37.50	8.44	77.5
10	19.38	4.75	75.5
20	11.25	2.28	79.7
40	7.50	1.22	83.7
60	6.00	0.88	85.3
100	4.69	0.63	85.9

Table 2: Energy consumption comparisons of the s27 based on I-ECRL and conventional CMOS

	Energy consumption per cycle (fJ)		
Frequency (MHz)	Conventional CMOS	I-ECRL	Saving rate (%)
5	121.88	53.75	55.9
10	62.50	27.50	56.0
20	35.31	14.06	60.2
40	24.33	7.18	70.5
60	18.44	4.88	73.5
100	14.38	---	---

Simulated waveforms for the benchmark s27 based on I-ECRL are shown in Fig. 10.

Table 2 shows the total energy losses of the s27 based on conventional CMOS and I-ECRL. Simulation results show that the I-ECRL s27 attains 55.9 to 73.5% energy savings compared with the one based on the conventional CMOS logic. Compared with the conventional CMOS one, the I-ECRL circuits attains large energy savings, because the dynamic energy dissipations of the I-ECRL circuits are reduced greatly by recovering effectively the charge of the circuit odes.

I-ECRL circuits with gate-length biasing and DTCMOS techniques: The leakage currents are highly relates with the threshold voltage of MOS devices. For short channel transistors, the threshold voltage increases with increasing of the gate length. Therefore, both dual-threshold CMOS and gate-length biasing can reduce leakage dissipations. These two techniques are used for the sequential benchmark s27 based on I-ECRL, as shown Fig. 11.

In order to use dual-threshold CMOS and gate-length biasing techniques, critical and non-critical regions should be identified for the entire circuit. The high-V_t devices can reduce greatly leakage dissipations. However, the high-V_t devices will lower the performance of the circuits, thus they are used for the non-critical regions. Increasing gate lengths slightly can decrease leakage dissipation effetely, while circuit performance only has little effect. Therefore, gate-length biasing is used for critical regions. For the sequential benchmark s27, the shaded are non-critical regions that use the DTCMOS technique, while the others are critical regions that use gate-length biasing technique, as shown in Fig. 11.

The power consumption comparisons have been carried out for the sequential benchmark s27 based on conventional CMOS logic, basic I-ECRL and I-ECRL with both gate-length biasing and DTCMOS techniques, as shown in Fig. 12. For gate-length biasing, the gate length of the transistors is chosen as 54 nm.

Among three implementations, the power consumption of the I-ECRL s27 using dual-threshold CMOS and gate-length biasing techniques is the lowest. Simulation results show that the I-ECRL s27 based on the DTCMOS and gate-length biasing techniques attains 23.3 to 28.2% energy savings compared with the basic

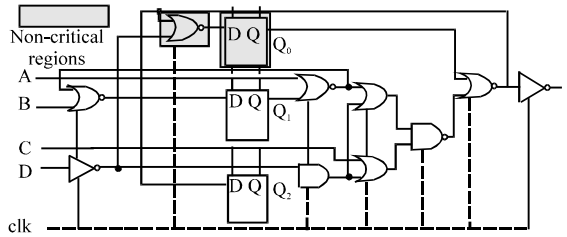

Fig. 11: I-ECRL s27 with gate-length biasing and DTCMOS

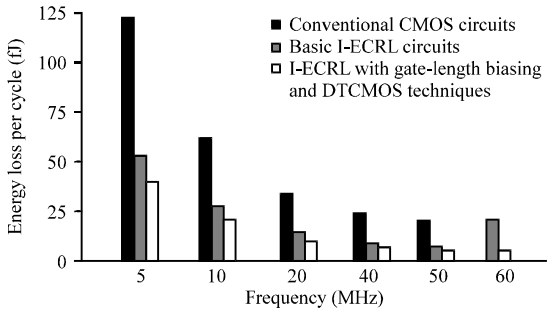

Fig. 12: Energy consumption comparisons of the benchmark s27 based on conventional CMOS, basic I-ECRL and I-ECRL with both gate-length biasing and DTCMOS techniques

I-ECRL. Compared with conventional CMOS, the I-ECRL s27 based on the DTCMOS and gate-length biasing techniques attains 66.2 to 79.7% energy savings.

CONCLUSIONS

Present study focuses on adiabatic computing for dynamic and leakage consumption reductions of the CMOS ICs. An improved Effective Charge Recovery Logic (I-ECRL) based on adiabatic computing with dual-threshold CMOS and gate-length biasing techniques have been proposed. Compared with the basic ECRL circuits, the proposed I-ECRL circuits use simple power clocks. Moreover, complex digital circuits that are widely used in low-power portable computers can easily been implemented by the I-ECRL circuits without pipeline operating demand. Results show that both leakage and dynamic dissipation of the I-ECRL circuits based on adiabatic computing with dual-threshold CMOS and gate-length biasing techniques are greatly reduced compared with the conventional CMOS circuits

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