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Low-voltage MOS Current Mode Logic for Low-Power and High Speed Applications

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Abstract: Low power design has already become the main challenge in the modern VLSI design community. The voltage scaling techniques have proved one of the most effective methods for low power design. In this study, the design method of the low-voltage low-power MOS Current-Mode Logic (MCML) in nanometer CMOS technology is addressed. The analytical formulation of minimum supply voltage of the two-level MCML is derived. The results show that the power consumption in MCML can be decreased by reducing the supply voltage V_{DD} without degrading the performance of MCML. As examples, the low-voltage MCML 1-bit full adder and 4-2 compressor are designed and simulated by HSPICE at the 45 nm CMOS process using the NCSU PTM model. The simulation results show that the proposed 1-bit full adder can obtained about 36 and 31% energy savings compared with the conventional MCML and CMOS ones using normal supply voltage at 4.0 GHz, respectively. The low-voltage MCML 4-2 compressor based on full adders can obtained about 33% energy savings compared with the conventional CMOS one at 5.0 GHz.

Key words: MOS current mode logic, low voltage, low power, full adder, 4-2 compressor

INTRODUCTION

MOS Current-Mode Logic (MCML) is one of the most widely used logic styles in high-speed circuits such as high-speed processors and Gbps multiplexers for optical transceivers (Cao *et al*., 2002; Tanabe *et al*., 2001; Yamashina and Yamada, 1992). However, MCML has high static power consumption due to its constant operation current. Recently, the low power MCML logic design has obtained quit some attentions (Heydari, 2003; Caruso and Macchiarella, 2007; Anis and Elmasry, 2002; Hassan *et al*., 2006). Caruso and Macchiarella (2007) presented the methodologies for the low-power design of MCML-based ring oscillators and buffer chain, respectively. Anis and Elmasry (2002) proposed the multi-threshold MCML (MTMCML) technology that allows the reduction of the minimum supply voltage of the two-level MCML circuits, hence lower the power dissipation of the MCML circuits (Anis and Elmasry, 2002). However, the analysis presented by Anis and Elmasry (2002) for MTMCML was based on inaccurate long-channel modeling equations which is inappropriate to use in today's nanometer CMOS technologies. Hassan *et al*. (2006) presented a comprehensive MTMCML analytical formulation based on the BSIM3v3 model.

Power dissipation in MCML is equal to $V_{DD}\times I_B$, where V_{DD} is the supply voltage and I_B is the current flowing through the constant current source. So the power dissipation of MCML can be saved by reducing either the V_{DD} or the I_B. While I_B can not be reduced under a certain limit, otherwise performance will be degraded. Hence, reducing the supply voltage is an effective method to lower the power consumption of MCML circuits.

The aim of this study to propose a low-voltage low-power design technique of MCML in nanometer CMOS technology.

REVIEW OF CONVENTIONAL MCML CIRCUIT

MCML topology: The basic MCML inverter/buffer and bias circuit are shown in Fig. 1. The MCML inverter is composed of three main parts: the load transistors P1 and P2, the full differential pull down switch network consisting of N1 and N2 and the current source N_S. The load transistors are designed to work as load resistors by operating them in linear region of operation. This is accomplished with the help of the control voltage VRFP produced by the bias circuit which also controls the output logic swing (Musicer and Rabaey, 2000). Figure 2 shows the MCML universal logic gate (Abdulkarim and Shams, 2007), XOR2/XNOR2 and 2-1MUX. The MCML universal logic gate can realize any of the basic two-input logic functions, namely, the AND2, NAND2, OR2 and NOR2 operations. The additional transistor, i.e., N5, improves the symmetry of the universal gate and has been shown to improve the MCML gate's performance in high-speed applications (Abdulkarim and Shams, 2007).

The operation of MCML is performed in the current domain. The pull down network switches the constant

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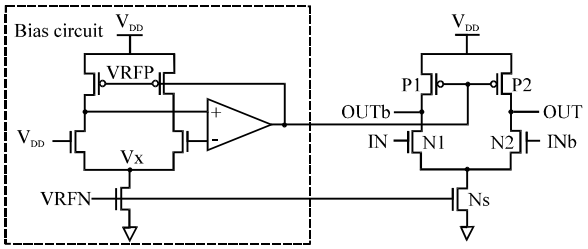


Fig. 1: MCML inverter and bias circuit

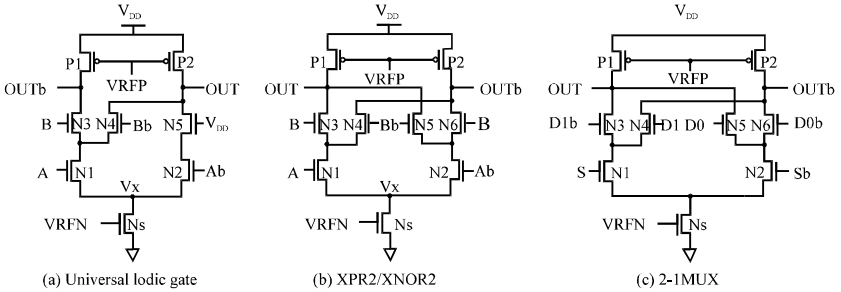


Fig. 2(a-c): MCML gates, (a) Universal logic gate, (b) XOR2/XNOR2 and (c) 2-1 MUX

current between two branches and the load converts the current to output voltage. The high and low digital logic levels are $V_{OH}=V_{DD}$ and $V_{OL}=V_{DD}-I_BR_D$, respectively, where R_D is the PMOS load impedance. The logic swing $\Delta V= V_{OH} - V_{OL} = I_BR_D$.

Performance metrics of basic MCML gate: The metrics of basic MCML gate can be divided into two categories: hard constraints and optimization goals. Hard constraints place a limit on some performance metric which must not be violated. Optimization goals do not have any fixed requirements but should be minimized or maximized whenever possible. The main hard constraints include DC voltage gain A_v, Noise Margin (NM), Voltage Swing Ratio (VSR) and Signal Slope Ratio (SSR).

DC voltage gain A_v is defined as the mid-swing voltage gain. A_v controls the robustness of the circuit, and is always chosen larger than 1 to ensure regeneration and stability for subsequent stages. A_v is given by Alioto and Palumbo (2003):

$$A_v = g_m \cdot R = \Delta V\sqrt{\mu_n C_{ox}\frac{W_n}{L_n I_B}} \quad (1)$$

where, g_m is the transconductance of the differential pair, C_{ox} is the oxide capacitance of the MOS and μ_n is the differential pair electrons mobility.

The Noise Margin (NM) of the MCML inverter can be expressed as:

$$NM = \Delta V(1-\frac{\sqrt{2}}{A_v}\sqrt{1-\frac{1}{\sqrt{2}A_v}}) \quad (2)$$

MCML circuits have high noise immunity because of their differential structure; hence, a small NM is sufficient for proper operation.

Voltage Swing Ratio (VSR) is defined as the ratio of the current in the ON branch I_{on} to the total circuit current I_B:

$$VSR = I_{on}/I_B \quad (3)$$

The optimization performance metrics of the MCML gate mainly include propagation delay, power dissipation and power-delay product. The delay time of a MCML gate can be calculated assuming that, at each transition, the whole I_B, ideally, flows through one branch of the differential pair and charges the total load capacitance C, is given by:

$$t_d = 0.69RC = 0.69C(\Delta V/I_B) \quad (4)$$

The power consumption of a MCML gate is independent of the switching frequency and it is given by:

$$P = V_{DD} \times I_B \quad (5)$$

where, V_{DD} is the supply voltage. I_B is the bias current of the MCML gate.

Finally, the power-delay product is independent of the switching frequency and can be calculated as:

$$PDP = P \times t_d = 0.69 V_{DD} \times \Delta V \times C \quad (6)$$

LOW VOLTAGE MCML CIRCUITS

Power vs frequency analysis of MCML and conventional CMOS circuits: For given V_{DD} and I_B, the power dissipation of MCML gates is a constant value. It is independent of both the operation frequency and fanout. Furthermore, the power of MCML gates is also independent of the logic function. It is well known that MCML managed to meet the needs for high-speed VLSI circuits while consuming less power than conventional CMOS circuits at these high-frequencies.

The power dissipation of conventional CMOS circuits can be expressed as:

$$P = \alpha f V_{DD}^2 C_L \quad (7)$$

The power of CMOS circuits is dependent of the operation frequency linearly. So there exists a cross-frequency, above which it is more power efficiency to use MCML rather than conventional CMOS. It is importance to estimating the cross-frequency for effectively using MCML circuits from the power efficiency point of view. There is a simple method to estimating the cross-frequency according to the energy dissipation per cycle of the conventional CMOS gates. The energy dissipation per cycle of the conventional CMOS gates can be expressed as:

$$E_{CMOS} = V_{DD}^2 C_L \quad (8)$$

where, V_{DD} is the supply voltage, C_L is the load capacitance of the gate. While the energy dissipation per cycle of the MCML gates is:

$$E_{MCML} = P_{MCML} T = P_{MCML} / f \quad (9)$$

where, P_{MCML} is the power of the MCML gates, f is the operation frequency. When $E_{CMOS} = E_{MCML}$, the cross-frequency f_c can be derived,

$$f_c = I_B / (V_{DD} C_L) \quad (10)$$

It is assumed that the MCML and conventional CMOS circuits operate in the same supply voltage. According to the Eq. 10, the cross-frequency f_c can be estimated. Taken the CMOS inverter as an example, at a 45nm process, V_{DD} =1.1V, I_B = 10 μA and C_L = 1fF, then the cross-frequency f_c is about 9.1 GHz.

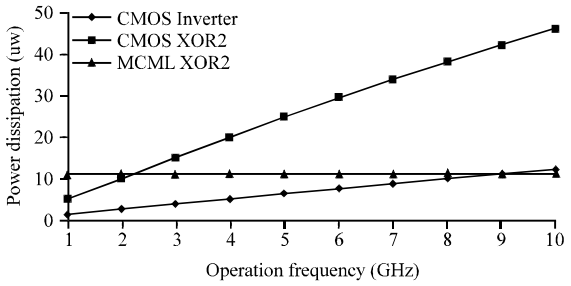


Fig. 3: Power vs. Frequency in CMOS and MCML Gates for a CMOS 45nm Process, V_{DD}=1.1V

Furthermore, some interesting observation can be obtained from Eq. 10. Firstly, the cross-frequency f_c will lower with the increase of load capacitance at a specific process. It means that complex MCML gates are more power efficiency than simple ones to implementing the same logic function. Secondly, the cross-frequency f_c will increase with the technology scaling down. For example, in 0.18 μm CMOS process the cross-frequency of the inverter is about 2.2 GHz (Hassan *et al*., 2006), while in 45 nm process it is about 9.1 GHz.

The cross-frequency of different logic gates is measured using HSPICE at a 45 nm process with the NCSU PTM model. The supply voltage of all gates, include MCML and conventional CMOS circuits is the technology nominal supply voltage (1.1 V). The bias current I_B of the MCML is 10 μA. The simulation results are shown in Fig. 3.

According to the simulation results, the cross-frequency of simple logic gates (inverter, NAND2, NOR2) is higher than complex gates. Hence, the MCML circuits are more suitable to implemented complex gates from the energy efficiency point of view.

Minimum supply voltage analysis: According to Eq. 4 and 5, it can be seen that the power consumption in MCML can be decreased by reducing V_{DD} and without degrading the performance of MCML. Meantime, the power-delay product can also be improved as the V_{DD} decreased. So the low-voltage design method is an effective way to improve the power efficiency of the MCML gates.

It is essential to analysis the minimum supply voltage needed for the proper operation of the MCML circuit. The minimum operating supply voltage for an MCML circuit is defined as the lowest voltage at which the differential pairs as well as the current source (Ns) are made to operate in the saturation region to ensure correct

functionality and adequate performance. The V_{min} of MCML universal logic gate, shown in Fig. 2a), can be expressed as:

$$V_{min} = V_{ds1,sat} + V_{dss,sat} + V_{gs3} \quad (11)$$

where, $V_{ds1,sat}$, $V_{dss,sat}$ and V_{gs3} are the drain-source saturation voltage for N1, drain-source saturation voltage for Ns and the gate-source voltage for N3, respectively. In general, the drain-source saturation voltage $V_{ds,sat}$ is expressed as:

$$V_{ds,sat} = \frac{I}{2WC_{OX}v_{sat}}\left(\sqrt{1+\frac{4E_{sat}WLC_{OX}v_{sat}}{I}}-1\right) \quad (12)$$

where, E_{sat}, C_{ox} and v_{sat} are the saturation electric field, oxide capacitance and saturation velocity, respectively, while W and L are the transistor effective width and length, respectively V_{gs3} is given by:

$$V_{gs3} = V_{th3} + \frac{I}{2W_3C_{OX}v_{sat}}\left(1+\sqrt{1+\frac{4E_{sat}W_3L_3C_{OX}v_{sat}}{I}}\right) \quad (13)$$

Substituting with Eq. 11 and 12 into Eq. 13, the V_{min} of MCML universal logic gate is:

$$\begin{aligned} V_{min} = {} & \frac{I}{2W_1C_{OX}v_{sat}}\left(\sqrt{1+\frac{4E_{sat}W_1L_1C_{OX}v_{sat}}{I}}-1\right) \\ & + \frac{I}{2W_sC_{OX}v_{sat}}\left(\sqrt{1+\frac{4E_{sat}W_sL_sC_{OX}v_{sat}}{I}}-1\right) \\ & + V_{th3} + \frac{I}{2W_3C_{OX}v_{sat}}\left(1+\sqrt{1+\frac{4E_{sat}W_3L_3C_{OX}v_{sat}}{I}}\right) \end{aligned} \quad (14)$$

According to the Eq. 14, the minimum operating voltage of the MCML can be estimated. Using the BISM4 model, the relationship of the bias current I_B,V_{th3} and the V_{min} is depicted in Fig. 4.

It is shown that V_{min} decreases with reducing V_{th3}. Hence, the static power dissipation of the MCML gates can be reduced by using the low-threshold voltage devices in the NMOS differential pair, while maintain the performance of the MCML gates. And furthermore, Fig. 4 dictate that reducing I_B can further allow a decrease in V_{min}. MCML circuits operating at lower speeds require smaller I_B for the same ΔV, the supply voltage can be reduced. Thus more power saving can be obtained. This is an interesting observation as it offers a way to reduce power dissipation in circuits operating at lower frequencies, thus moving the cross-point frequency point in Fig. 3 to the left.

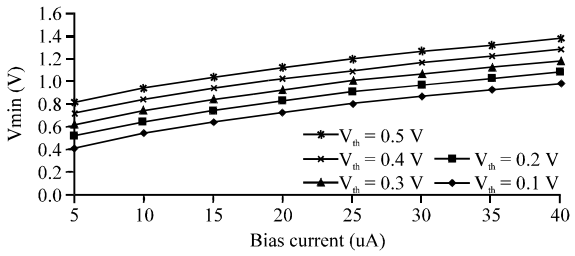


Fig. 4: Minimum supply voltage of mcml circuits

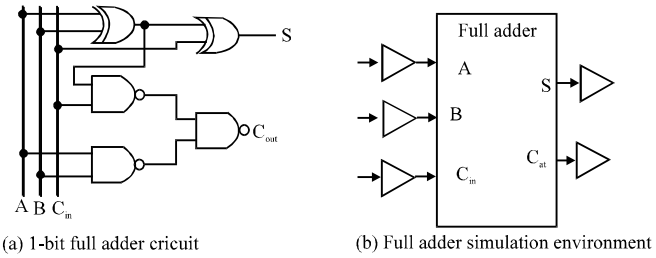
LOW-VOLTAGE LOW-POWER MCML CIRCUITS DESIGN

The optimization design methods of MCML circuits are already presented (Alioto and Palumbo, 2003; Hassan *et al*., 2005; Musa and Shams, 2010). So, the optimization problems of the MCML circuits are not discussed in this section. We will mainly concern the power characteristics of the low-voltage MCML circuits. In the section, the low-voltage MCML full adders and 4-2 compressor are designed to demonstrating the low power feature of the proposed low-voltage MCML technology.

Low-voltage MCML (LV MCML) full adder: The conventional 1-bit full adder circuit is shown in Fig. 5a). The simulation environments for the full adder circuits are shown in Fig. 5b). Each input is driven by buffered signals and each output is loaded with buffers which provide a realistic simulation environment reflecting the full adder operation in actual applications. The LV MCML full adder is simulated using HSPICE at the 45 nm CMOS process using the NCSU PTM model. The device size of PMOS load transistors and current source NMOS transistor is taken with W/L =4γ/2γ and 20γ/6γ, respectively. The device size of NMOS transistors of the differential pair is taken with 8γ/2γ and γ = 25 nm. The V_{th0} of the NMOS transistors is 0.466 V. The bias current of the LV MCML is 10 μA.

According to the analysis results of minimum supply voltage the supply voltage of LV MCML circuits is selected as 0.7 V. The supply voltage of the conventional MCML is 1.1 V. For comparison, the conventional CMOS and MCML full adders are also verified using the 45 nm CMOS process based on the same architecture. The power-frequency relationship of the LV MCML, conventional MCML and CMOS full adders is shown in Fig. 6.

The simulation results show that the cross-frequencies of the LV MCML and Conventional MCML are 2.8 and 4.3 GHz, respectively. The LV MCML 1-bit full adder can obtained about 31 and 36% energy savings



(a) 1-bit full adder cricuit (b) Full adder simulation environment

Fig. 5(a-b): Full adder and simulation environment, (a) 1-bit full adder and (b) Simulation environment

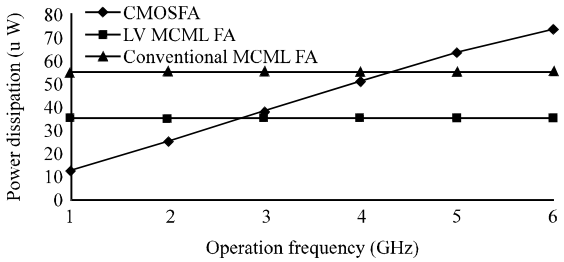
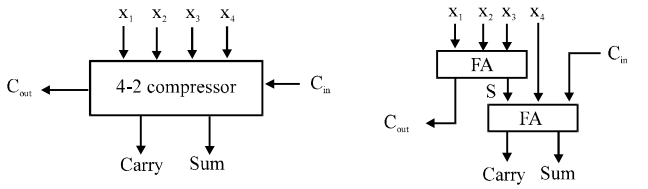


Fig. 6: Power-frequency relationship of lv mcml, conventional mcml and cmos full adders



(a) Diagram of 4-2 compressor (b) Conventional 4-2 compressor

Fig. 7(a-b): 4-2 Compressor, (a) Diagram of 4-2 Compressor and (b) Conventional 4-2 Compressor

compared with the conventional MCML and CMOS one operating at normal supply voltage at 4.0 GHz, respectively.

Low-voltage MCML 4-2 compressor: The 4-2 compressors have been widely employed nowadays for high-speed multipliers. Owing to its regular interconnection, 4-2 compressors are ideal for the construction of regularly structured Wallace tree with low complexity (Chang *et al*., 2004).

A 4-2 compressor has five inputs and three outputs, as shown in Fig. 7a). The four inputs (x_1, x_2, x_3 and x_4) and the output (Sum) have the same weight. The output Carry is weight one binary bit order higher. The 4-2 compressor receives an input C_{in} from the preceding module of one binary bit order lower in significance and produces an output C_{out} to next compressor module of higher significance. To accelerate the carry save summation of the partial products, the output C_{out} must be independent of the input C_{in}.

The conventional implementation of a 4-2 compressor is composed of two serially connected full adders. We can also use low-voltage MCML full adders to configure a 4-2 compressor, as shown in Fig. 7b).

The power of the LV MCML, conventional MCML and CMOS compressor has been compared, as shown in Fig. 8. The simulation results show that the proposed LV MCML compressors have considerable power saving. The cross-frequencies of the two MCML compressors to the CMOS one are 3.3 and 5.2 GHz, respectively. The LV MCML compressor only consumes about 64% of the dissipated energy of the conventional one operating at nominal supply voltage (1.1 V). Compared with the conventional CMOS implementation, the LV MCML compressor attains energy savings of 33% at 5.0 GHz.

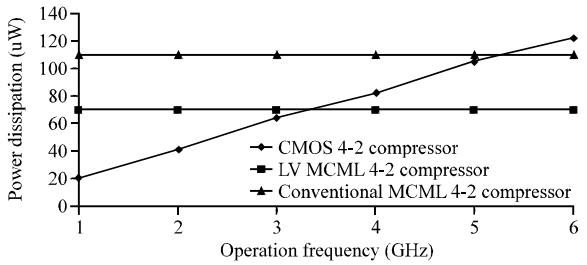


Fig. 8: Power dissipation of the LN MCML, conventional and CMOS 4-2 compressor

CONCLUSIONS

In this study, the minimum supply voltage (V_{min}) of the two-level MCML circuits is analyzed and its analytical formulation is derived. According to the proposed analytical formulation, it is found that there is a minimum supply voltage (V_{min}) of MCML which ensure correct functionality and adequate performance. A low-voltage low-power design strategy about MCML circuits is proposed. The main idea of the proposed strategy is lower operating voltage of the MCML to improve the power efficiency without performance penalty. The low-voltage MCML 1-bit full adder and 4-2 compressor are designed and simulated by HSPICE at the 45 nm CMOS process using the NCSU PTM model. The simulation results show that the proposed 1-bit full adder can obtained about 31 and 36% energy savings compared with the conventional MCML and CMOS ones operating at normal supply voltage at 4.0 GHz, respectively. The LV MCML 4-2 compressor based on full adders can obtained about 33% energy savings compared with the conventional CMOS one at 5.0 GHz. Hence, the proposed low-voltage MCML design strategy is an attractive method for low-power and high speed applications.

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