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Ant Colony Algorithm and Genetic Algorithm Optimization for Test Vector Reordering

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Abstract: Power dissipation during testing has been found to be much more than during normal mode due to increased switching activity. Test vector reordering technique helps mitigate this problem as it enables the reduction of switching activity during testing. This study presents a new test vector reordering approach. This approach maps the reordering problem to Traveling Salesman Problem (TSP). A hybrid ant colony algorithm and genetic algorithm is presented to solve this problem. The proposed approach is effective and verified with ISCAS'85 benchmark circuits which shows that yield on an average of about 30.05% reduction in switching activity.

Key words: Test vector reordering, ant colony algorithm, genetic algorithm, testing, traveling salesman problem

INTRODUCTION

For CMOS circuits, there are two main sources of power dissipation: dynamic dissipation due to switching transient current and discharging of load capacitances and static dissipation due to leakage current through the channel and the tunneling current through the gate oxide drawn. For existing CMOS technology, dynamic dissipation is the dominant source of power dissipation and is proportional to the amount of switching activity in the circuit. Switching activity in a circuit can be much greater during test than during normal operation. This is because successive functional input vectors applied to a given circuit during system mode have a significant correlation and in severe situation, the extra power consumption might destroy circuits (Zorian, 1993).

Many techniques have been proposed to address the problem of reduction test power. Sharifi *et al*. (2005) have used low leakage blocking pattern in conjunction with non-critical inputs only. Major drawbacks of this approach include area and functional timing overheads and scan enable relate timing closure. Another approach is to divide the scan chain into multiple scan segments (Whetsel, 2000). The approach requires additional clock gating and bypasses multiplexers (Huang and Lee, 2001; Elshoukry *et al*., 2005; Yoshida and Watati, 2003; Lin *et al*., 2007). Scan chain modification is a method that targets at reducing the number of transitions in scan chain during shift cycle. Reordering of scan chain may conflict with other objectives during scan chain optimization including wire length minimization and timing closure. The easiest approach to make the transition during test comparable to that of the normal function is to reorder the test vector which reduces the internal switching activity by reducing transition density at circuit inputs (Kavousianos *et al*., 2004; Chakrabarty and Dabholkar, 1994; Girard *et al*., 1999). Changing the order of application test vector from ATE to circuit under test can reduce test power. The techniques map the reordering problem to Traveling Salesman Problem (TSP) and Hamming distance is applicable to the reordering of test vectors (Attofian *et al*., 2003; Latypov, 2001).

This study presents a new test vector ordering techniques that reduce power dissipation during test operation. For this purpose, the proposed technique reduces the total switching activity by lowering the switching activity at circuit inputs. The objective is to find an optimal test vector ordering for a given test sequence such that the switching activity in the circuits is minimum. This problem can be seen as a problem of TSP. In this method for test vector ordering, test vectors are like cities and their Hamming distance are distance between cities. A hybrid ant algorithm is presented to solve this problem (Bala and Perinbam, 2006; Chang *et al*., 2010; Kundu *et al*., 2009). This algorithm combines genetic algorithm with the improved crossover operator and mutation operator which makes the local optimal solution cross and mutate, then improves the algorithm's search

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and enhances the ability to find feasible solutions. The method considers combinational circuits or full scan sequential circuits and has no impact on the initial defect coverage. Compared with existing test vector ordering methods, this technique is the most efficient solution proposed up to now. This feature is illustrated with the experimental results gathered on the benchmarks.

BACKGROUND AND RELATED WORK

The two components of power dissipated in a CMOS circuit are static dissipation (P_{st}) and dynamic dissipation due to switching transient current (P_{sc}) and discharging of load capacitances (P_d). The total power dissipation (P_{total}) is given by:

$$P_{total} = P_{st} + P_{sc} + P_d \quad (1)$$

In above three parts, P_d is the main source of power dissipation. P_d can be calculated using the following equation:

$$P_d = \frac{1}{2}\alpha C V_{DD}^2 f \quad (2)$$

where, V_{DD} and C are the power supply voltage and the total capacitance of circuit, respectively. These values depend on the chosen technology and cannot be adjusted in the design phase. f is the clock frequency and is decided based on the normal operation of circuit rather than the test mode. α is the occurrence probability of a transition.

To decrease power consumption in the design phase, the common way is to decrease the switching activity because this factor completely depends on the design and test policy. Therefore, the aim is to find out the optimal order of test vector application to minimize power dissipation. The test set reordering can be reduced to the well-known traveling salesman problem (Sokolov *et al.*, 2005; Chattopadhyay and Choudhary, 2003; Jelodar and Mizanian, 2006; Wang *et al.*, 2009) where the individual test vectors are the cities and the Hamming distance between any two test vectors is the distance between those two cities and we find the shortest path way to achieving the minimum switching activity. The problem can be describes as follows:

Given an undirected graph G = (V, E) where V = $\{V_1, V_2, ..., V_n\}$ to find path $\langle V_1, V_2, ..., V_n \rangle$, such that for $i_j = \{1, ..., n\} \forall j$, each vertex from the graph can be visited once and only once.

TEST VECTOR REORDERING

Ant colony algorithm and genetic algorithm can solve TSP problem. Considering ant colony algorithm have the positive feedback effect and convergence easily to a local optimum. Simultaneously, crossover operator and mutation operator of genetic algorithm can expand diversity of solution. So genetic algorithm can be embedded into the ant colony algorithm (Liu *et al.*, 2011; Gu *et al.*, 2011). Algorithm for test vector reordering based on ant colony algorithm and genetic algorithm is show as follows:

- **Step 1:** Parameter initialization. Let t = 0, iteration times $N_c = 0$ and the maximal iteration times be $N_{c\,max}$, $\eta_{ij}(t) = 1/d_{ij}$ where d_{ij} is the Hemming distance between test vectors i and j. Set the n ants on the n elements. Let the initialization information for each edge on the directed graph be $\tau_{ij}(t)$, where const denotes constant and the initial time be $\Delta\tau_{ij}(0) = 0$
- **Step 2:** To encode
- **Step 3:** Let iteration times be $N_c \leftarrow N_c+1$
- **Step 4:** Let the index number for ant taboo list be k = 1
- **Step 5:** Let the number of ants be $k \leftarrow k+1$
- **Step 6:** The individual ant chooses the city $j(j \in \{C-tabu_k\})$ to move to according $p^k_{ij}(t)$
- **Step 7:** Modify the pointer of taboo list which denotes the new city that the ant attempts to move to after choice and then add this city to the taboo list for the ant
- **Step 8:** If set C is not visited thoroughly, that is, $k<n$, then go to step 5, else execute step 10
- **Step 9:** On the ant colony individual crossover and variation
- **Step 10:** Update the information according $\tau_{ij}(t+n)$, $\Delta\tau_{ij}(t)$, $\Delta\tau^k_{ij}(t)$
- **Step 11:** If the conditions for loop terminates are satisfied, that is, if iteration times subjects to $N \geq N_{c\,max}$, jump from the loop and output the results, else clear the taboo list and jump step 3

τ^k_{ij}, $\tau_{ij}(t+n)$, $\Delta\tau_{ij}(t)$, $\Delta\tau^k_{ij}(t)$ and $p^k_{ij}(k)$ is computed according to Dorigo *et al.* (2006).

EXPERIMENTAL RESULTS

Experimental results based on ISCAS'85 benchmark circuits are performed. In these experiments, only the dynamic power dissipation is considered since it is the dominant term in the total power consumption of CMOS

Table 1: Results on test vector reordering

Circuit	Initial transition	Final transition	Improve (%)
C432	2961	1832	38.13
C880	7638	5498	28.02
C1355	16535	12457	24.66
C1908	41102	28425	30.84
C2670	46589	30622	36.42
C5315	111521	88734	21.33
C7552	284658	206531	30.96

circuits. Achieved experimental results are given in Table 1. The first column denotes the type of circuit, the second and the third column denotes the total number of transitions before using proposed algorithm and that after using proposed algorithm. The fourth column is the percentage of power dissipation reduction.

It can be seen that in the best case the proposed method reduces the power dissipation for circuit C432 by 38.13%, in the worst case, power dissipation for circuit C5315 by 21.33%. The average power dissipation is reduced by 30.05%. For all circuit, the proposed method reduces circuit transition activities significantly.

CONCLUSIONS

As the technology has scaled down from submicron to nanometer region, power minimization problem has become very important both during design and test of VLSI circuits. In this study, a new approach based on ant colony algorithm and genetic algorithm Optimization for test vector reordering is proposed for minimizes the total power dissipation through test vector reordering. This approach is an effective technique for saving scan power during testing since it requires no extra DFT logic and does not the fault coverage. The switching activity for the proposed algorithm has been reduced compared with that obtained by reorder before. Experiments have been performed on ISCAS'85 benchmark circuits and the results show that for all circuits, this reordering approach can obtain a great reduction in test application power consumption. This approach does not involve at any point reordering of the of scan cells which might be used for future work.

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