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The Design for Airborne Electronic Equipment Fault Diagnostic System Base on IPC

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Abstract: With the rapid development of science and technology, modern aviation equipment increases its functionality, while, its structure becomes more and more complex, the speed and reliability requirements are increasing also. The study introduces the design for airborne electronic equipment fault diagnostic system based on IPC, containing the design about the hardware and software, as well as function and task.

Key words: Airborne electronic equipment, diagnostic system, IPC, BIT

INTRODUCTION

In the process of development of electronic circuits, analog circuits were earlier than digital circuits but the pace of development of digital circuits was much faster than analog circuits. The researches of analog circuit automatic testing and fault diagnosis have been relatively slow progress and the application was also not wide enough. Because first, the integration of analog circuits is low and the scale is small. By using the traditional manual testing and diagnosis of maintenance, it can meet the actual needs but the analog circuit automatic test and fault diagnosis lack strong external force. Second, the analog circuit automatic test and fault diagnosis are much more difficult than the digital circuits, none of the theories which are fully mature, could be put into practical application so far (Lord and Gleason, 1981).

Test design is the ability how to determine the working status of systems and equipment timely and accurately and isolate faults in the design of its internal characteristics. With the rapid development of computer technology, test technology is to improve the effective of the system maintenance and technical support capabilities.

FAULT DETECTION RATE, FAULT ISOLATION RATE

It is the percentage that the fault can be tested by using in the method under the condition in all faults which occurred in the specified time, as the Expression 1:

$$R_{FD} = (ND/NT)\times 100\% \tag{1}$$

Where:

NT: All faults which occurred in the specified time

ND: The fault can be tested by using in the method under the condition

The test projects contain system, combination, modules, boards and other components and important parts. Specified time refers to the time which is used for aggregating the total failures number and detecting them. Prescribed conditions contain the state of the tested items, the maintenance level and the officer level. Ordain methods mean BIT, the external test equipment dedicated or general-used, ATE, manual inspection or several methods integrated to complete the fault detection. The rate of integrated automatic testing fault detection is generally 98% (Shao and Lamberson, 1988).

Fault isolation rate:

$$R_{FI} = (NL/ND)\times 100\% \tag{2}$$

Where:

NL: The number of faults could be detected correctly by using the provisions method under specified conditions

ND: With the provisions under specified conditions, the number of fault can be isolated correctly to the prescribed replaceable unit number = L (normal = 3)

Fault isolation degree D_{FI} False alarm rate, Fault detection time T_{FD}, Fault isolation time T_{FI}: The data means fault isolation and positioning accuracy. The fault isolation degree for different levels is different; Isolation is usually divided into LRU (Line Replaceable Unit) and SRU (Shop Replaceable Unit). Testing fault isolation is generally component level.

Detection error probability is also called the false alarm rate detection. False alarm is the test device or equipment shows the test project fault but actual there isn't fault for the project. False alarm rate is the number of false alarms occurred take up the ratio of the total number of fault. Requirements of airborne electronic equipment false alarm rate is less than 2%. Fault detection time means how long the time is needed from the fault happened to be detected. Comprehensive automatic test failure detection time normally should not exceed 10 min. Fault isolation time is the time from the fault being detected to the fault being isolation to the replaceable unit provided is how long. Integrated automatic testing fault isolation time normally should not exceed 15 min.

INFORMATION EXTRACTION, THE DESIGN OF THRESHOLD LEVEL, READ INFORMATION OCCASION

To improve the fault detection coverage and improve fault location capability, it is needed for fully extracting all kinds of digital avionics information, discrete amount of information, testing information. The rational design of the circuit threshold level is one important factor which is relate to the automatic test equipment and it can judge the electronic device functionality and performance are correct or not, as well as, whether is there a failure and how to achieve accurate position and reduce false alarm rate. The threshold level should be reference to the discrete signal input/output level value of the device.

The occasion for reading information isn't appropriate may result in the information wrong, then come to the judgment that the product function/performance does not meet the design requirements and the product has fault, so the correct time setting information is an important design aspects for automatic test equipment.

The design of software criterion, information integrate processing: Whether the design of the software criterion is rational, it is the second important factor for the automatic test equipment to judge the airborne electronic equipment's function and performance are correct or not, whether there are failures and how to achieve the failures' accurate position and reduce false alarm rate. There are several modules which share the same information in the airborne electronic equipment, the failure of one module which will also reflect the failure of other related modules, so how to achieve the accurate position information and this will be the key factor for the automatic test equipment will not reduce its airborne electronic equipment fault detection for itself and the accurate location capability.

Currently, avionics system uses more and more technology with microprocessor control and system integrated but the devices under test often do not have complete test checking for themselves. So, the ATE requires the extension of the function, machine inspection, performance testing, fault detection, fault location and so on, including the wholes' and the part's. The functional requirements of automatic test equipment compose diagram shown in Fig. 1.

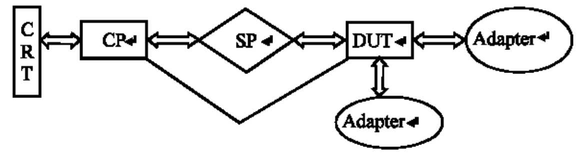

Fig. 1: The functional diagram, CP: Center processor, SP: Signal processor, DUT: Device under test

CP, THE COMMUNICATION BUS MODULE

CP is composed by IPC, the communication bus module, data acquisition interface board module and the analog-digital conversion interface board modules. Center processor is the control center and the data processing center of the automatic test equipment, the center processor can complete the airborne electronic products function tests, performance tests, fault detection and fault location by gathering and outputting in the form of stimulus of various digital information and discrete information. The communication bus module is fit for the IPC with PCI which contains the integrate design with BC, RT, MT. As the software selects the work way, the bus transfer rate of 1 MB/s while the bus transfer error rate is less than 10^{-7} and the response time for RT status word less than 12 μsec, as well as other functions.

A/D conversion card, data acquisition card: With 16 single-ended or 8 differential input channels and a 12 bit analog output channels, programmable timer/counter, automatic channel/gain scanning, programmable gain input channels and other functions, A/D conversion card is fit for pulse amplitude, width, spacing and other indicators test. With 48 digital I/O, 8255 PPI mode simulation, interrupt handling, timer/counter interrupting, maintaining I/O ports setting and digital output after system restart, it is used in gathering digital signal, analog signal and outputting of all control signals.

IPC, SP: Industrial control computer is the main part of the automatic test equipment. With a P III 1 GHz, the hard disk 60G, 512 M memory and other performance indicators, it takes charge the equipment test data analysis and processing. The main function of the signal processor is to process various digital information and discrete information which is the output by the center processor (including amplification, shaping, coding and decoding), then the processor formats the signal which is

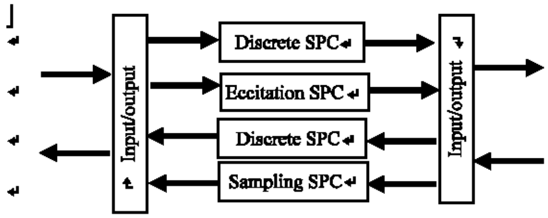

Fig. 2: The central processor

complied with the requirements of airborne electronic equipment and sends to the device and processor the signals which is output by airborne electronic equipment and the adapter (including amplification, shaping, coding and decoding), the final step is to format the signal which meets the requirements of central processors and send to the central processor as shown in Fig. 2.

Software design: The design is modular design, also containing the design of fault-tolerant methods. According to the functional requirements of automatic test equipment, software mainly is composed by several modules, such as the system functional testing, system parameters, fault detection, automatic self-test equipment, data processing, information display and other modules. The function of airborne electronic equipment test is completed by system function test sending an order under way and analyzing the receiving state. By collecting amplitude information and variety time information of electronic equipment the parameters test is completed, fault detection finishes the system-level fault detection and location, also including the extension level fault detection and location which is through the way of ordering issued and gathering feedback from electronic equipment.

CONCLUSION

The airborne self-test circuit-board enhances the airborne electronic equipment fault detection capabilities, such as the reliability of fast response and accurate location, automated isolation and early warning, also reduces the maintenance time, as the integration and complexity of electronic devices increasing, it will be more difficult for the BIT design which will lead to it need more efforts in the hardware and software to improve equipment self-test capability (Chen and Xu, 2002).

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