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A Multi-stage Design of Intermediate Frequency Digital down Converter

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Abstract: Digital Down Converter (DDC) is one of the key technologies in Software Defined Radio (SDR), especially in the Intermediate Frequency (IF) digitization systems. Accordingly, this study introduces a multi-stage design of IF DDC which begins with the performance indication determination, followed by two decompositions of multiple filter combinations, then the comparison between these two decompositions are presented to choose a better decomposition, finally the fix-point bit error rate simulation is carried out and the result shows that the proposed DDC design yields excellent performance close to the theoretical Bit Error Rate (BER) bound.

Key words: Digital down converter, bit error rate, FIR filter, multi-stage design

INTRODUCTION

Digital Down Converter (DDC) and multi-rate signal processing are the key technologies in Software Defined Radio (SDR) and DDC has become an indispensable component in modern radar, sonar, wireless communication systems (Harris, 2004; Ma *et al*., 2005; Nakagawa *et al*., 2008; Cui *et al*., 2006; Perez-Pascual *et al*., 2009). In IF DDC, it shifts the desired spectrum from its carrier frequency (intermediate frequency, in fact) to the base band. Once Nyquist theorem is satisfied, the reduction of data rate degrades the amount of effort required for subsequent signal processing while ensures no information loss.

Typical structure of DDC consists of the Numerically Controlled Oscillator (NCO), mixer and decimating filter consist of decimation and lowpass filter (Harris, 2004). This study focuses on the decimating filter and a multi-stage structure is investigated and compared, resulting in preferable structure decomposition which reduces the filter length and computation complexity while maintains the filtering performance.

Generally, a decimating filter can be decomposed into the Cascaded Integrator-comb (CIC) filter, the Half Band (HB) filter and the Low-pass Filter (LPF). In order to optimize the structure of decimating filter, we should take into consideration the CIC filter length, the HB filter length and the design of LPF. The last filter is very helpful to DDC and there are two alternatives: the FIR filter and the IIR filter (Lyons, 2004; Lai, 2009; Lai and Lin, 2010; Tseng, 2004; Yang and Yu, 2007). Due to the linear phase requirement in communication systems (Proakis, 2000), FIR filter is more suitable in our study. The design methods include the linear Programming method (Johnson, 1990; Samueli, 1988), the Parks-McClellan algorithm (McClellan and Parks, 2005; McClellan *et al*., 1973), the window method, the frequency sampling method and the least squares method (Lyons, 2004). Without loss of generality, the Parks-McClellan algorithm is employed in our study.

A number of researchers had limited their study to design of DDC with few considerations on quantification which may cause performance loss after quantization in real-world applications. Meanwhile, few papers mention the complete process of designing a DDC from performance specification determination to realization. Accordingly, this paper tries to fill up the gap which is helpful to practical applications.

THE DDC STRUCTURE

Typical structure of DDC: Figure 1 shows a typical structure of DDC which consists of the NCO, mixer and decimating filter. The Analog-to-digital Converter (ADC) outputs sampling signals and the NCO realize the quadrature demodulation, while the LPF filters the background noise, finally the D-times decimation

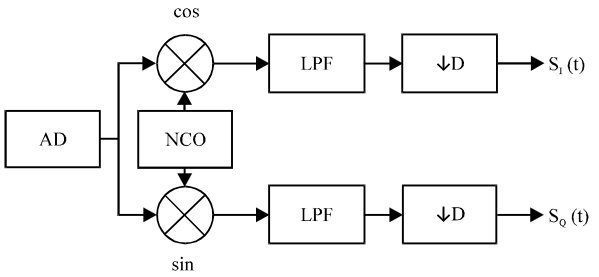

Fig. 1: Typical structure of DDC

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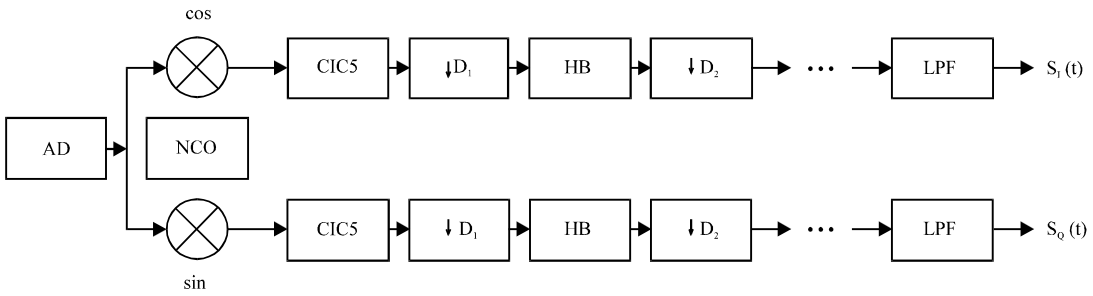

Fig. 2: Structure of DDC based multi-stage design

decreases the sampling rate. Since, the computing ability of DDC limits the highest rate of input signal data stream, it is very important to optimize the structure of DDC.

DDC structure based on multi-stage design: The different between Fig. 1 and 2 is that Fig. 2 employs a multi-stage decimation instead of the single stage decimation. It consists of the CIC filter and the HB filter (Harris, 2004; Hogenauer, 1981; Lim *et al*., 2005) both of which are of high efficiencies. For example, the CIC filter uses the shift operation instead of the multiply operation and the HB filter has a property that its impulse response coefficient is zero at even indices except the zero index which means that only half calculating works are required for two times decimation realized by the HB filter.

Signal model of DDC: Let the modulated signal be:

$$s(n) = a(n)\cos(\omega_0 n+\varphi(n)) \quad (1)$$

where, a (n) and φ (n) are amplitude and phase information carried by this signal. Formula 1 can also be described as:

$$s(n) = 1(n)\cos(\omega_0 n)-Q(n)\sin(\omega_0 n) \quad (2)$$

where, I (n) = a (n) cos (φ (n)) and Q (n) = a (n) sin (φ (n)) represent the in-phase component and the quadrature component (Proakis, 2000). The quadrature demodulation extracts both of them by NCO and LPF. Make the in-phase component as example:

$$\begin{aligned} Z_I(n) &= s(n)\cos(n) \\ &= I(n)\cos^2(\omega_0 n) - Q(n)\sin(\omega_0 n)\cos(\omega_0 n) \\ &= \frac{I(n)(1+\cos(2\omega_0 n))}{2} - \frac{Q(n)\sin(2\omega_0 n)}{2} \end{aligned} \quad (3)$$

when, z_I (n) passes through the LPF, only the low-pass element (I (n)) remains and the high-frequency element is cancelled.

Table 1: The parameter of DDC

Parameters	Values
Carrier frequency	50 MHz sec^{-1}
Signal rate	1.28 MHz sec^{-1}
Roll-off factor	0.22
Oversampling factor	4
Total bandwidth	1.5616 M

MULTI-STAGE DESIGN AND DECOMPOSITION OF DDC

Some system parameters of this study come from the TD-SCDMA standard (Meng *et al*., 2008). One can use other parameters from different standards to design DDCs analogously.

According to Table 1 and the band-pass sampling theorem (Harris, 2004), we choose 61.44 MHz (1.28 MHz×48) as the sampling frequency of ADC. Moreover, because the oversampling factor is four, the decimating filter requires twelve times decimation in all.

The DDC performance specification determination by single stage method: There are no literature about the detailed performance specification of a certain DDC, thus many simulations have to be done to search the appropriate performance specification for DDCs of TD-SCDMA, where, the tested signal is generated by MATLAB and the BER is exploited to distinguish different single stage filters.

Three kinds of single stage filters are designed by Parks-McClellan algorithm and listed in Table 2. The specification of the better one will be chosen to use in the multi-stage DDC. Certainly, it may not be the best one but an acceptable one. The filters act as the LPF in Fig. 1 and a twelve times decimation followed.

There is a relationship like triangle between transition bandwidth, passband ripple and stopband attenuation (Lyons, 2004), i.e., these three parameters cannot approach the optimum point at the same time which is explicitly shown in Table 2. Moreover, Fig. 3 presents the BER simulation to find the best single stage filter and give suggestion which parameter is more important to DDC.

Obviously, Fig. 3 demonstrates that FIR1 is the best and FIR3 is the worst, it also presents stopband attenuation is most important to DDC. For this reason, the performance specification of FIR1 will be used in the following multi-stage design. Figure 4 shows the frequency response of FIR1.

Now return to the multi-stage DDC design. Since, the decimation factor is twelve and the HB filters can only realize 2 M times decimation, there are two kinds of DDC realization. One is the two stage design with a single CIC filter realizing six times decimation and a single HB filter realizing two times decimation as shown in Table 3, the other is the three stage design in which a CIC filter realizes three times decimation and two HB filters realize four times decimation as shown in Table 4.

The two stage design of DDC: Note that the filters in Table 3 are working at different sampling rates, however, by padding zeros into the filter coefficient, they can be converted to the highest sampling rate, i.e., 61.44 Mbps. In other words, all three filters will construct a cascade equivalent filter working at 61.44 Mbps sampling rate as shown in Fig. 5.

Table 2: The parameter of single stage filter

Parameters	FIR1	FIR2	FIR3
Filter length	1526	934	924
Passband cut-off frequency (MHz)	1.28	1.28	1.28
Stopband start frequency (MHz)	1.5616	1.5616	1.5616
Normalized passband cut-off frequency	0.0208	0.0208	0.0208
Normalized Stopband start frequency	0.0254	0.0254	0.0254
Passband ripple	0.057 dB	3 dB	0.01 dB
Stopband attenuation	78.7 dB	80 dB	20.5 dB

Table 3: The parameter of two stage decimating filter

Parameters	CIC5	HB	SR-Nyquist
Filter length	26	26	106
Passband cut-off frequency	4.2 MHz	4.78 MHz	1.28 MHz
Stopband cut-off frequency	18.33 MHz	6.83 MHz	1.56 MHz
Normalized passband cut-off frequency	0.14	0.47	0.25
Normalized stopband cut-off frequency	0.500000	0.67	0.305
Passband ripple	3 dB	0.0017 dB	0.0005 dB
Stopband attenuation	47.7 dB	80 dB	79.79 dB
Attenuation at 1.28 MHz	0.27 dB	0.0014 dB	0.0005 dB
Attenuation at 1.5616 MHz	0.4048 dB	0.0014 dB	79.79 dB
Decimation factor	6	2	

Because the bandwidth of the input signal is 1.5616 MHz, the passband cut-off frequency of CIC filter or HB filter is much larger. Thus, they play a role as all-pass filters which suggests that the SR-Nyquist filter (Farhang-Boroujeny, 2008; Tuncer, 2002) after decimation affects the DDC performance significantly. In multi-stage DDC, the SR-Nyquist filter is used as the matched filter and lowpass filter.

Figure 5 presents the frequency response of the equivalent filter by cascading all filters in the 61.44 Mbps sampling rate, where the passband ripple, the stopband attenuation, the passband cut-off frequency and the stopband start frequency are 0.28, 80 dB, 1.27 and 1.78 MHz, respectively. We can conclude that the CIC filter influences the passband ripple of the equivalent filter and the LPF influences the stopband attenuation, while the passband cut-off frequency and the stopband start frequency is affected by all filters. The frequency response of SR-Nyquist filter is given in Fig. 6.

The three stage design of DDC: Analogous to the above discussion, we design the three stage filter in Table 4.

Figure 7 presents the frequency response of the equivalent filter by cascading all filters in the 61.44 Mbps

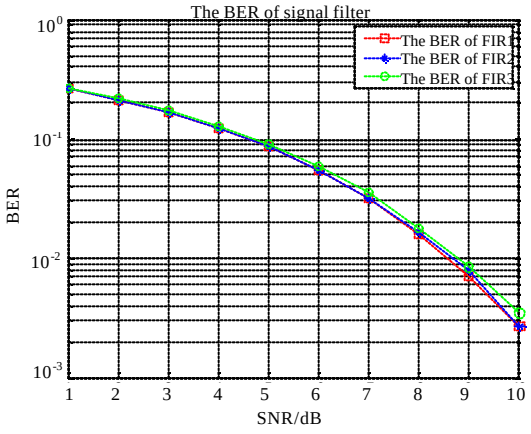

Fig. 3: The BER of FIR1, FIR2 and FIR3

Table 4: The parameter of three stage decimating filter

Parameters	CIC5	HB1	HB2	SR-Nyquist
Filter length	10	10	26	106
Passband cut-off frequency	8.84 MHz	8.84 MHz	4.78 MHz	1.28 MHz
Stopband cut-off frequency	30.72 MHz	17.15 MHz	6.83 MHz	1.56 MHz
Normalized passband cut-off frequency	0.14	0.43	0.47	0.25
Normalized Stopband cut-off frequency	0.50	0.84	0.67	0.305
Passband ripple	3 dB	0.0017 dB	0.0017 dB	0.0005 dB
Stopband attenuation	47.71 dB	80 dB	80 dB	79.79 dB
Attenuation of 1.28 M	0.062 dB	0.0015 dB	0.0014 dB	0.0005 dB
Attenuation of 1.5616 M	0.093 dB	0.0017 dB	0.0014 dB	79.79 dB
Decimation factor	3	2	2	

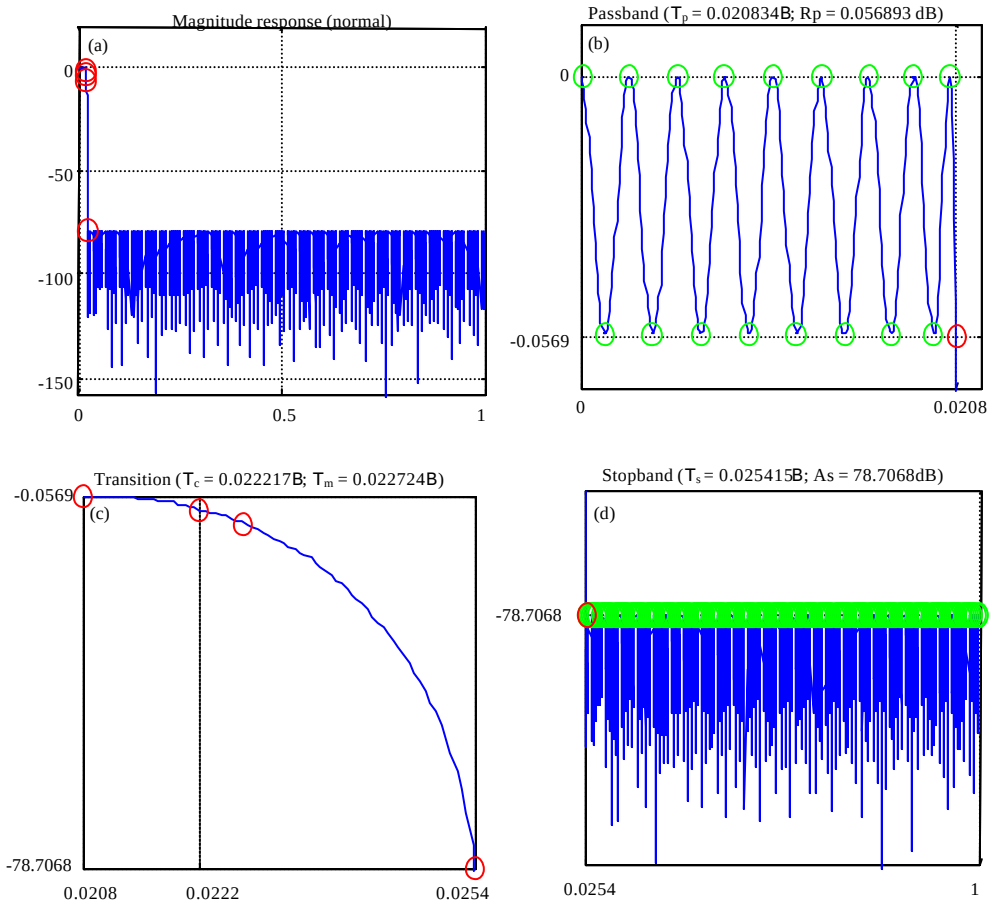

Fig. 4(a-d): The frequency response of FIR1

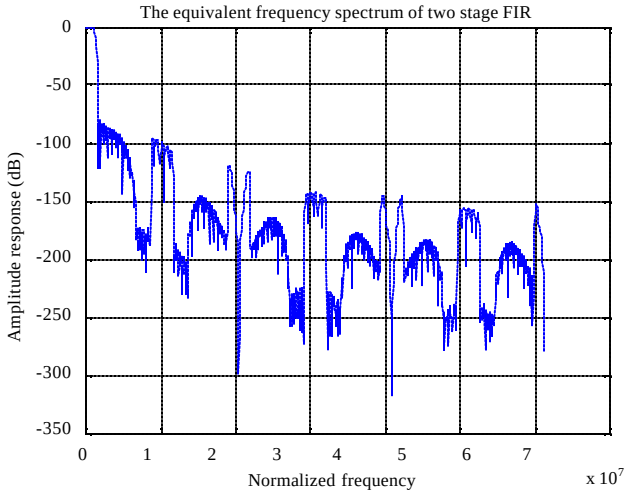

Fig. 5: The frequency response of the equivalent filter with the 61.44 MHz sampling frequency

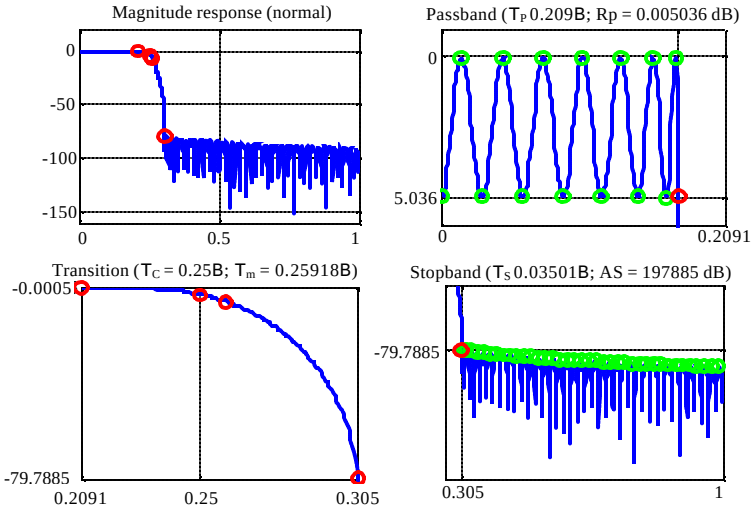

Fig. 6: The frequency response of SR-Nyquist filte

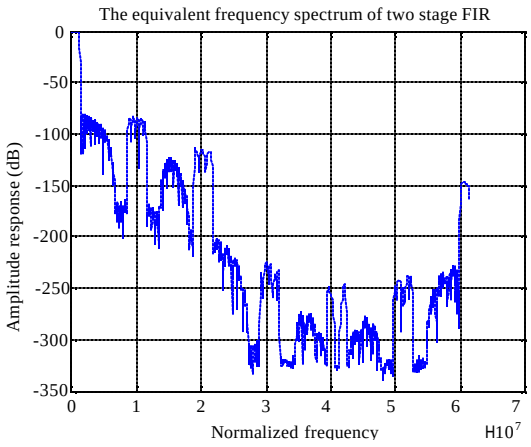

Fig. 7: The frequency response of the equivalent filter with the 61.44 MHz sampling frequency

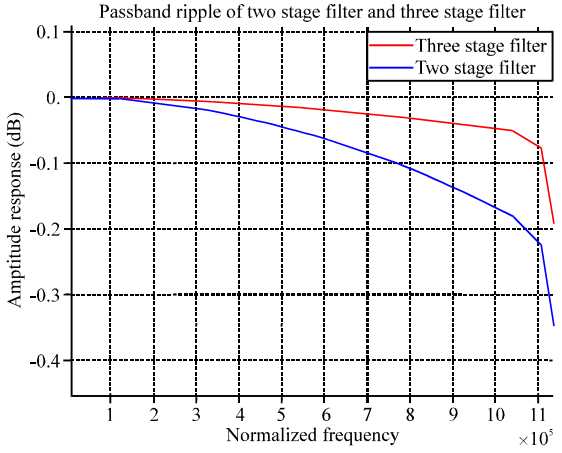

Fig. 8: The passband ripple of two stage filter and three stage filter

sampling rate, where the passband ripple, the stopband attenuation, the passband cut-off frequency and the stopband start frequency are 0.067, 80 dB, 1.275 and 1.58 MHz, respectively. The passband ripple of two stage equivalent filter is compared with that of three stage equivalent filter in Fig. 8. From Fig. 7 and 8, in terms of performance specification of the equivalent filter, the three stage design is better than the two-stage design. Moreover, Table 3 and 4 demonstrate that the passband ripple of six times decimation CIC filter is much larger than three times decimation CIC filter and the former's length is also larger than that of the latter. Therefore, the following discussion will exploit the three stage structure.

Figure 9 shows that the single stage filter has similar performance specifications as the three-stage filter. However, the total length of single stage filter is 1526, resulting in 763 multiplying unit, while in three stage structure, since the CIC filter doesn't need multiplying unit and the length of HB1 filter, HB2 filter and the SR-Nyquist filter are 10, 26 and 106, respectively, only 63 multiplying units are required (HB1 filter needs 3 multiplying units and HB2 filter needs 7 multiplying units). Obviously, the multi-stage structure can meet the requirement of performance specification and significantly decrease the number of multiplier.

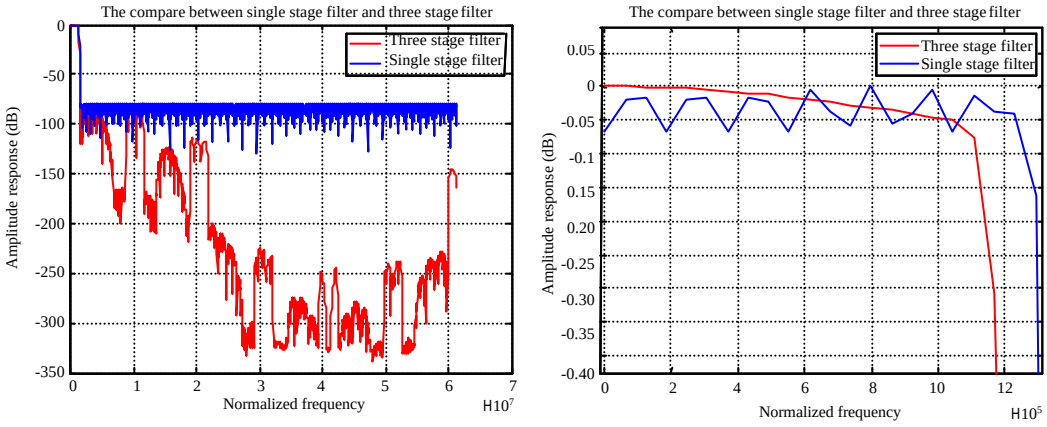

Fig. 9: The frequency response of the single stage filter and three stage filter

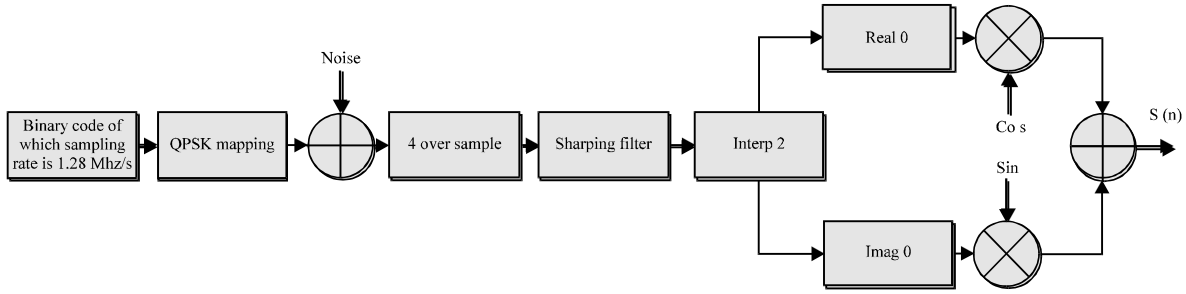

Fig. 10: The test signal generation

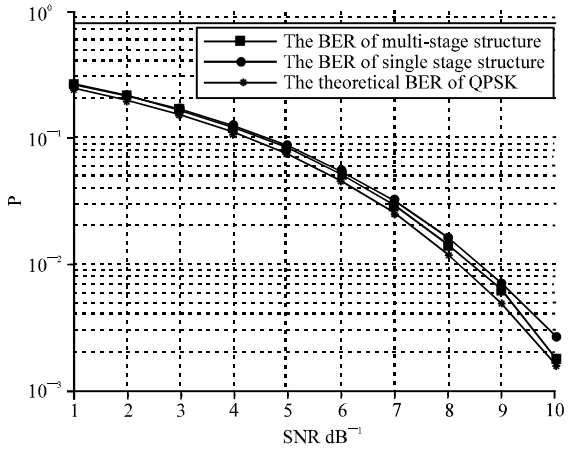

Fig. 11: The BER of multi stage structure and single structure in continuous domain

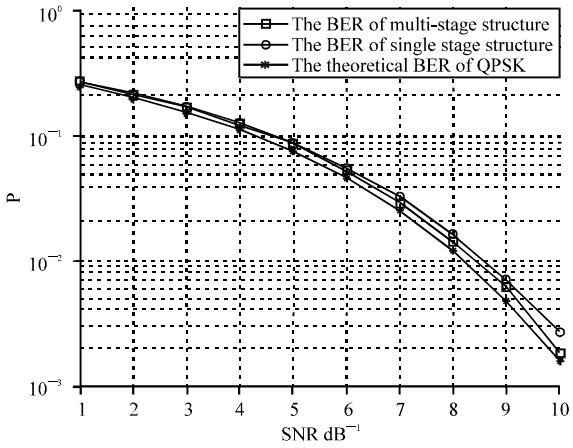

Fig. 12: The BER of multi stage structure and single structure after 8 bits quantification

SIMULATION AND ANALYSIS

This section gives the BER simulation of single stage DDC and multi-stage DDC. The test signal is generated according to Fig. 10 which is an universal structure in wireless communications (Proakis, 2000). In Fig. 10, the shaping filter exploits the root-raise-cosine filter and the twelve times interpolation uses the built-in MATLAB function interp.

Figure 11 shows BERs of single stage DDC and multi-stage DDC in continuous domain, while Fig. 12 presents the result with 8 bits quantification (fix-point

scenarios). It's easy to find that the BER of multi-stage DDC is lower than that of single stage DDC in Fig. 11 and 12. Moreover, even with 8 bits quantification, the proposed DDC design exhibits good performance close to the theoretical curve which is due to that the SR-Nyquist filter plays a role as matched filter and lowpass filter to restrain the noise as well as remove inter-symbol interferences.

CONCLUSIONS

In this study, single stage DDC and multi stage DDC are compared carefully and detailedly, where the multi-stage structure shows a great complexity reduction while maintains the BER performance. However, the single stage structure may be useful when the performance specification is unknown, since at this time it's convenient to simulate and check the performance of the single stage DDC. Moreover, this study just provides a feasible way to design acceptable DDCs instead of the optimum one, since the best performance usually corresponds to large filter length and complexities. In practical environments, there must be a trade-off between the performance and complexity, it can be approached by the proposed design procedure.

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