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Low Power Compact GaAs PHEMT Level Converter for Digital Control Logics of GaAs Switches

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Abstract: In this study a level converter based on GaAs pHEMT technology for a MFC (Multifunctional Chip) is designed, simulated and tested for the application of T/R (Transmit/Receive) module for an X band phase array radar system. It has the advantages of smaller chip size, lower power consumption, higher efficiency, lower cost and high stability. The circuit design is based on a feedback and feed-forward network which compensates the chip process variations during the wafer fabrication and operation temperature changing. It results the designed chip has a high stability. Its supply voltage is -5 v with a shared bias generator, this allows reducing the power consumption compared with the other design at -7.5 v in the literature. The testing results have shown that the proposed novel design has met all the specifications given in this project.

Key words: GaAs pHEMT, control logic, switch, multifunction chip, phase array radar

INTRODUCTION

Level converter is an important part of a MFC (Multifunctional Chip) and the link between the central control units and the MFC's digitally controlled phase shifter and attenuator (Devlin, 1992; Clifton and Arnold, 1992). It can be integrated outside of the MFC as an independent chip and assembled together with MFC as a module, such as introduced by Mazumder and Isham (1995). This arrangement has the disadvantage of bigger overall module size and difficulty, specially in the application of phased array radar T/R module by using LTCC (Low Temperature Co-fired Ceramic) technology introduced by Xia *et al*. (2007). On the other hand, it can be integrated within the MFC which echoes the present trend of microwave device design of high density integration, such as illustrated by De Boer and Mouthaan (2000), Ghione *et al*. (2010) and Van Vliet and de Boer (2004). The advantages of such arrangement are less power consumption, smaller in size due to high integration, lower requirement for system integration. However, it faces the problem of reducing the control lines have been used. De Boer and Mouthaan (2000), introduced a 16-bit series-to-parallel converter integrated within a MFC for the application of a X-band phase array radar system. Total three control lines are used to control a 7 bit phase shifter and 7 bit attenuator. Nevertheless, the reducing of the control lines increases cost for the processing with regarding of the compression in the chip size. A robust LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor) compatible logic for an X-band 5 bit digital attenuator and 6-bit phase shifter has been developed by Van Wanum *et al*. (2006). It has the advantages of insensitive to process variations, but it faces high power consumption due to its -7.5 v power supply. Therefore, a novel design of an X-band level shifter for a 6-bit phase shifter and 6-bit attenuator is introduced in this study. It has the advantages of smaller in size, lower power consumption, immune to the process variation and lower requirement for system assembly.

CONTROL LOGIC DESIGN

In this study the MFC requires control voltages of -2 and 0 v, however, the central control units from the CMOS chip can provides LVCMOS voltages which is 3.3 and 0 v. Therefore, the designed level converter has to have the ability of converting the LVCMOS voltages to the required voltages of -2 and 0 v. The block diagram of the level converter within a MFC chip is illustrated as in Fig. 1.

There are 12 control lines for each of the 6-bit phase shifter and 6-bit attenuator which result a total number of 24 control lines for the output of the designed level converter. Amount of these 24 control lines, 12 of them are used as the complementary part for the phase shifter and attenuator. The definitions of the digitized signals from the analogue signals are shown in Table 1.

As defined in Table 1, when the voltages provided by the CMOS is in the range of 0-1.0 v, two sets of output voltages can be achieved. When the output voltage is less than -1.7 v, it represents the digital logic 0 which

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switches the GaAs switch off. On the other hand, when the output voltage is greater than -0.7 v, it represents the digital logic 1 which switches the GaAs switch on. Same to the voltage of the CMOS output voltage between 1.6 and 3 v.

Table 1: Function of the level shifter

Input voltage value (v)	Output voltage value (V_{out} 1 and 2)	Digital Logic	Description
0 v<v_in<1.0 v	V_{out} 1<-1.7 v	0	GaAs switch off
	V_{out} 2>-0.7 v	1	GaAs switch on
1.6 v<v_in<3 v	V_{out} 1>-0.7 v	1	GaAs switch on
	V_{out} 2<-1.7 v	0	GaAs switch off

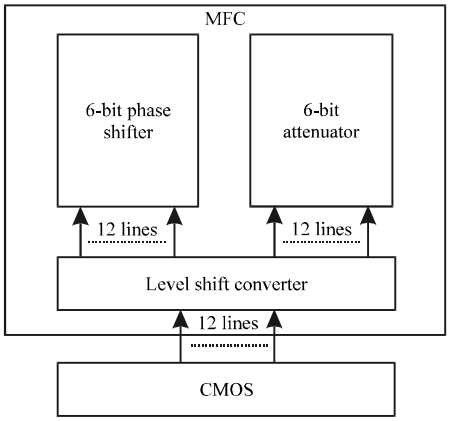

Fig. 1: Designed level converter within a MFC (multifunctional chip)

DESIGN STRATEGY

The circuit design is based on the feedback and feed-forward circuit design introduced by Van Wanum *et al.* (2006). The reason by choosing this circuit design is to avoid the effect of the process variations. However, the main difference compared with the circuit by Van Wanum *et al.* (2006) is that the new development has reduced the power supply voltage from -7 to -5 v which is more suitable for the low power consumption applications.

Proposed scheme: The overall schematic circuit is depicted in Fig. 2. From left to right, the power supply for the proposed circuit is -5 v. FET3, FET4 are used to generate the bias voltages for FET1, FET2. FET6 and FET7 are constructed in the differential mode which converts the LVCMOS voltage to the voltage required by the phase shifter and attenuator illustrated in Table 1. FET2 acts as a current stabilizer which keeps shifted voltage at the gate of FET7 has a near constant voltage drop compared with V_{in}. In order to ensure that the chip design immune to the temperature and chip process variation, a feed-forward and feedback circuit in the FET1, R6 and FET3 loop are applied (Van Wanum *et al.*, 2006). For the purpose of reducing the power consumption of the level converter, the amplitude of the supply power has to be reduced as well.

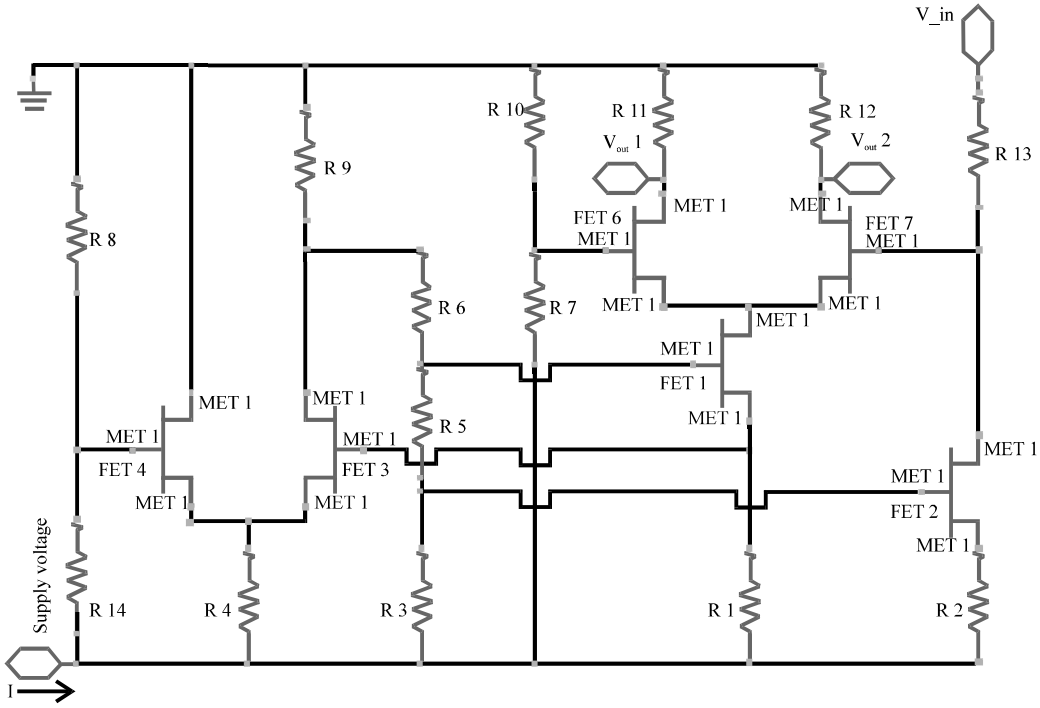

Fig. 2: Schematic circuit of the level converter

Analysis for circuit performances: After designing the schematic circuit, a Montecarlo simulation analysis is performed by using the ADS (Advanced Design Software) tool with regarding the variation of the resistors, temperature and the process variation. The values of the resistors have been changed around ±18% of its real value. The temperature is changed from -40-80°. The process variation is achieved by changing the threshold voltage of all the FET in the same way which is in the range of ±0.3 v. The simulation results are demonstrated in Fig. 3.

As shown in Fig. 3, the horizontal axis shows the input voltage V_{in} provided by the CMOS chip and the vertical axis represents the output voltages of the level converter, V_{out} 1 and 2, in which are plotted in Fig. 3. When V_{in} is less than 1 v, V_{out} 1 are less than -2.5 v with small linear variation of less than 0.2 v between the maximum value and minimum value; under the same condition, the V_{out} 2 are at 0 v with unnoticeable changing. When V_{in} is greater than 1.5 v, the V_{out} 1 with output voltage around 0 v are observed regarding the different variation conditions introduced in the previous paragraph; and the V_{out} 2 are all under -2.5 v with variation of less than 0.2 v peak to peak. These results have illustrated the characteristics of immune to the temperature and process variations in this novel design. However, in order to evaluate the effects of the supply voltage regarding the outputs of the level converter, a simulation with supply voltage varies from -5.5 to -4.5 v is carried out in which is shown in Fig. 4.

In Fig. 4, it can be seen that when V_{in} is less than 1.0 v, the outputs of V_{out} 2 are shifted linearly with the changing of the supply voltage, but there are no effects on the outputs of V_{out} 2. On the other hand, when the V_{in} is greater than 1.5 v, the changing of power supply has no effect on the outputs of V_{out} 1 and the outputs of V_{out} 2 are shifted linearly in the vertical axis.

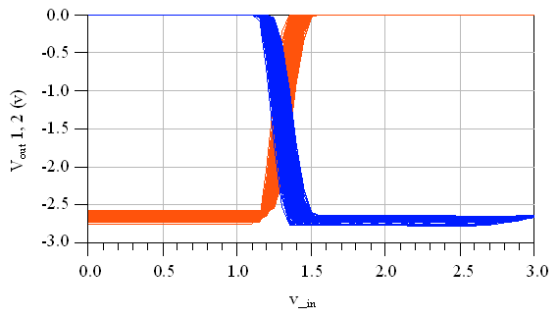

Fig. 3: DC simulation results of level converter versus input voltage with variations of the resistors (±18%), threshold voltage (±0.3 v) and temperature (-40-80 v)

Figure 5 shows the current with respect to different supply voltage. It can be observed that when the supply voltage increases from -5.5 to -4.5 v, the supply current has reduced from a maximum value of 880 uA to a maximum value of less than 600 uA for the range of V_{in} is changing between 0.0 and 3.0 v. At -5.0 V power supply, the maximum supply current is around 740 uA. This diagram has shown that the decreasing of the amplitude of the supply power is able to reduce the power consumption of the level converter. It leads to the reducing of the power consumption of the overall MFC chip, in which is an important factor in the phase array radar system application. However, the gate voltages for the FET's used in this design have to be considered as well during the choosing the power supply voltage. In the other word, the amplitude of the gate voltages for the FETs cannot be infinitely small with respect to the present process technology.

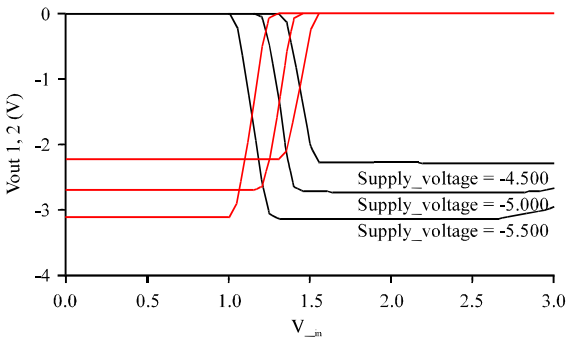

Fig. 4: DC simulation results of level converter versus supply voltage from -5.5 to -4.5 v

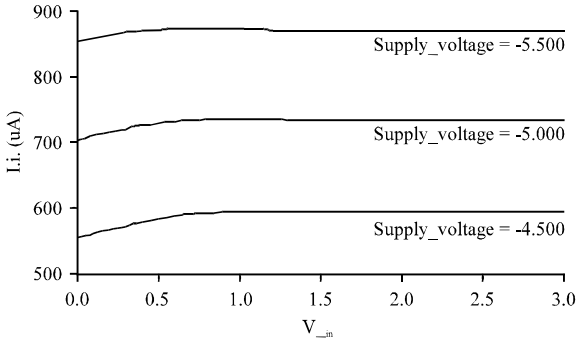

Fig. 5: DC simulation results of consumption current versus supply voltage from -5.5 to -4.5 v

REALIZATION AND CHARACTERIZATION

In order to compare with the results have shown in previous section and reference (Van Wanum *et al*., 2006), a set of 5-bit level shifter by using 6 inch 0.5 um GaAs pHEMT technology has been developed and tested. The stand-alone chip is integrated with the size of 1.3×0.4 mm including the banding pad to CMOS chip and the testing pads (which are deleted in a MFC). It is smaller compared with same 5-bit level converter introduced in (Van Wanum *et al*., 2006). A photograph of the realized chip is illustrated in Fig. 6.

In Fig. 6, the upper pads are used to connect the phased shifter or attenuator in which each pair of them represents a V_{out} 1 and 2 in Fig. 2 apart from the one at the right hand side upper corner. The lower pads are used as the V_{in} in Fig. 2 from the left hand side. This level converter is able to be scaled by adding or deleting the basic cell with regarding the application. For each cell the current of 0.225 mA is observed, the bias current is shared by the whole converter which is 0.5 mA. Thus the total current for the whole 5-bit level converter is 0.5+0.225×5 = 1.625 mA. Then, the power consumption of a level converter with 7 bit phase shifter and 7-bit attenuator is derived as: (0.5+0.225×14)×5 = 18.25 mw which is much smaller for the serial to parallel converter with 7 bit phase shifter and 7 bit attenuator of 70 mw introduced in (De Boer and Mouthaan, 2000).

The temperature variation effects of the level converter are demonstrated in Fig. 7. The temperature is model by using a thermal chamber in the range of -40-80°. The input signal of the testing chip is a squire wave illustrated in Fig. 8. When the input is high level, V_{out} 1 is appeared as high level and V_{out} 2 is shown as low level.

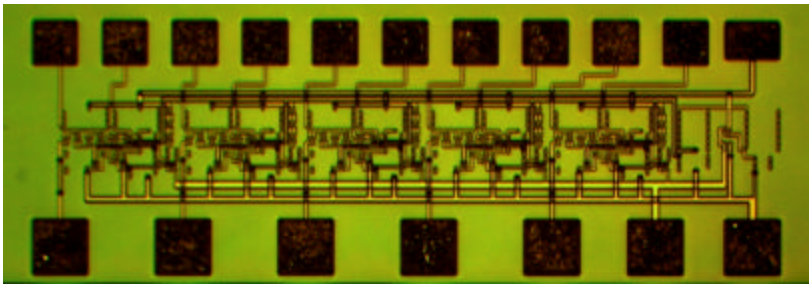

Fig. 6: The 5 bit level converter (size: 1.3×0.4 mm)

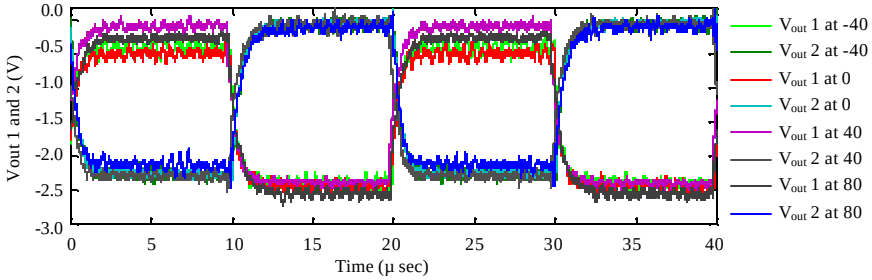

Fig. 7: Level converter versus the temperature (-40-80 v)

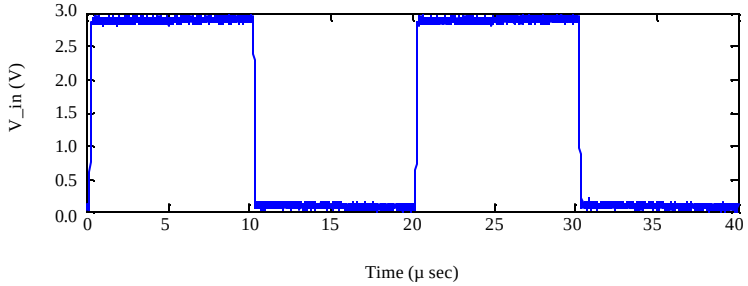

Fig. 8: Input signal for the testing level converter

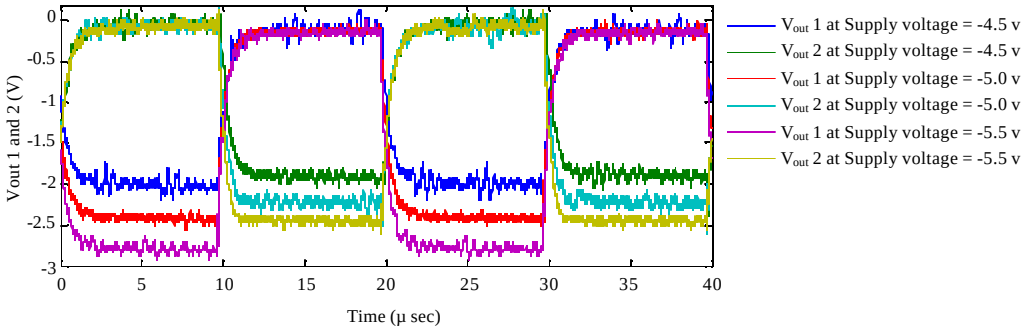

Fig. 9: Measurements of level converter versus supply voltage from -5.5 to -4.5 v

For V_{out} 1, the variation with respect to the temperature changing is approximately 0.65 v at its peak value in every 10 us time period. In the case of V_{out} 2, the maximum peak to peak value in every 10 us time period is less than 0.5 v with regarding all the temperature range. The output of V_{out} 1 and 2 are fit with the logical defined in Table 1.

Figure 9 shows measurement performances of the level converter with respect to the supply voltage variation from -5.5 to -4.5 v. With respect to the changing of the supply voltage, V_{out} 1 is greater than -0.4 v for high level and less than -1.7 v for low level. It is same to V_{out} 2, the high level is greater than-0.4 v and the low level is less than -1.8 v.

CONCLUSION

In this study a novel design of a scalable level converter within a MFC chip for the application of phased array radar system is introduced. The circuit is based on the feed-forward and feedback circuit design. It has the advantages of immune to the process variation and temperature changing. The reducing of the power supply leads to a much lower power consumption, specially comparing with a typical serial to parallel converter used in many applications. It has a smaller chip size compared with the level shifter which is not integrated within the MFC. The testing results have demonstrated that the proposed novel level converter is able to achieve the entire design requirement with respect to temperature and power supply variations. The future work this work is to integrate this design together with a 6 bit phase shifter and 6 bit attenuator within a MFC to evaluate the overall performance of the MFC for X-band phased array radar.

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