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A Modified Integrated Circuit Interface Based on M-ary Digital Pulse Cycle Modulation

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Abstract: A modified integrated circuit interface based on M-ary digital pulse cycle modulation is proposed in this study by describing its principle and structure to reduce the complexity of a high-speed circuit design and to improve the data transfer rate of a bandwidth-limited system. A demonstration system is built by using Field Programmable Gate Array (FPGA) to simulate the transceiver functions in a bandwidth-limited RS232 bus with a maximum data transfer rate is 320 Kbps and the interface proposed is used to achieve the maximum data transfer rate of more than 1.1 Mbps, without any other change in hardware circuit. Experimental results indicate that the interface proposed can be used to achieve a better data transfer performance.

Key words: M-ary digital pulse cycle modulation, modified interface, complexity of circuit design, data transfer rate

INTRODUCTION

With the fast development of manufacturing technologies, the interfacing speed requirement for Integrated Circuits (IC) is becoming increasingly stringent. For example, the interfacing speed for PCI-E (Peripheral Component Interconnect Express), Serial Advanced Technology Attachment (SATA) or several graphics DRAM (Dynamic Random-Access Memory), has gone up to Gbps level (Budruk *et al*., 2003; Grimsrud and Smith, 2003, Pareschi *et al*., 2010). A high interfacing speed results in more stringent requirements for circuit design, including impedance matching or electromagnetic compatibility (Eric, 2010). And the bandwidth limitation of a key device may limit the maximum data transfer rate of the whole system. For example, a long rise and fall time of white LED may cause the modulation bandwidth of tens of MHZ for a visible light communication system (Delgado *et al*., 2010). It is therefore of great significance to find ways and means to improve the data transfer rate of a system.

M-ary Digital Pulse Cycle Modulation (MDPCM) (Guanghui *et al*., 2013) is a base band modulation technology designed for bandwidth-limited systems. This is why a modified IC interface based on MDPCM is proposed in this study.

PRINCIPLE OF MDPCM

All M messages in a MDPCM system can be denoted as m_i and can be mapped to MDPCM symbol cycle T_i using binary or gray mapping. If a gray mapping is used, the messages associated with signal cycles are then adjacent to each other with a difference of one bit. The ith signal cycle can be expressed as:

$$T_i = \begin{cases} t_{BS} + [m_i + 1] \cdot t_{slot} & \text{for Binary mapping} \\ t_{BS} + [G_i + 1] \cdot t_{slot} & \text{for Gray mapping} \end{cases} \quad (1)$$

where, G_i is the gray mapping code for message m_i, t_{BS} is the duration of MDPCM of base symbol and t_{slot} is the time-resolved interval between adjacent MDPCM symbols.

The ith transmitted signal can be expressed as:

$$s_i(t) = \begin{cases} 1 & 0 \le t < t_{H0} \\ 0 & t_{H0} \le t < T_i \end{cases} \quad (2)$$

where, t_{H0} is the high level duration of a MDPCM base symbol when i = 0, t_L is the low level duration of a MDPCM base symbol, the minimum value of t_{H0} and t_L are defined using the bandwidth of a system and the minimum value of t_{slot} is defined using the time resolution of a system and it is determined by the jitter of a system and the time resolved interval a transceiver.

As shown in Fig. 1, MDPCM transmit waveform support binary mapping and gray mapping. Difference with binary mapping, the messages associated with symbol duration are made gray mapping adjacent to each other with a difference of one bit.

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Upon reception of MDPCM modulation symbol $s_x(t)$, the receiver uses an electronic counter to get period T_x of $s_x(t)$ and maximum likelihood (ML) symbol decision rule is used to get source gray data. The ML symbol decision rule can be expressed as:

$$dec_{ML}[T_x] = \arg\min_{t\in T} \|T_x - t\|^2 \quad (3)$$

After T_x is gotten, according to the mapping rules of binary or gray code and source code, demodulation message m_x can be expressed as:

$$m_x = enc^{-1}[dec_{ML}(T_x)] \quad (4)$$

Decision regions t_i (i = 1,..., M) can then be mathematically defined as:

$$t_i = \begin{cases} \left(-\infty, t_{BS} + \frac{3}{2}t_{slot}\right) & , \quad i = 1 \\ \left[t_{BS} + \left(M + \frac{1}{2}\right)\cdot t_{slot}, +\infty\right) & , \quad i = M \\ \left[t_{BS} + \left(i + \frac{1}{2}\right)t_{slot}, t_{BS} + \left(i + \frac{3}{2}\right)t_{slot}\right) & , \quad 2 \le i \le M-1 \end{cases} \quad (5)$$

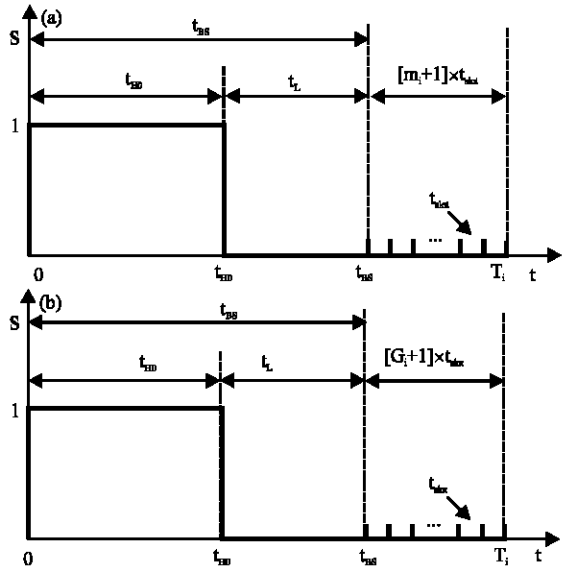


Fig. 1(a-b): M-ary digital pulse cycle modulation transmit waveform with (a) Binary mapping and (b) Gray mapping, where t_{H0} is the high level duration of base symbol when i = 0, t_L is the low level duration of base symbol, t_{BS} is the duration of base symbol, t_{slot} is the time-resolved interval between adjacent symbols, $(m_i+1)\times t_{slot}$ and $(G_i+1)\times t_{slot}$ are the duration of information symbol with binary mapping and gray mapping

PERFORMANCE OF MDPCM

Parameter r is the ratio of bit rate of signaling scheme to its bandwidth and it can be used to measure the bandwidth efficiency of a system. If $a=t_{slot}/t_{BS}$, the bandwidth efficiency of MDPCM can be expressed as:

$$r_{MDPCM} = \frac{\log_2 M}{a(M+1)+2} = \frac{b}{a(2^b+1)+2} \quad (6)$$

As shown in Fig. 2, MDPCM has a higher data transfer rate when parameter a is below 0.1 and b takes an appropriate value, because MDPCM uses a small t_{slot} to distinguish different transfer data, that means MDPCM can be used to achieve a higher transfer rate for a bandwidth-limited system. MDPCM can also be used to reduce the bandwidth requirement at the same data transfer rate when parameter a is below 0.1 and b takes an appropriate value. That means MDPCM can also be used

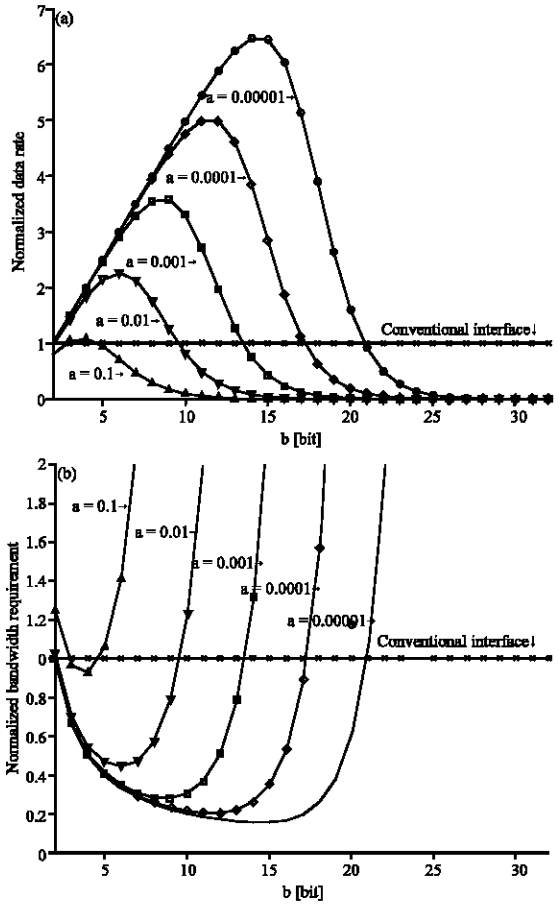


Fig. 2(a-b): (a) Normalized data transfer rate and (b) Normalized bandwidth requirement and for m-ary digital pulse cycle modulation

to reduce the switching frequency requirement for the interface of a system, thereby reducing the design complexity of integrated circuits.

MODIFIED HIGH-SPEED DIGITAL INTERFACE

Figure 3 shows, the modified interface mainly consists of Central Controller Unit (CPU), Phase Locked Loop (PLL), MDPCM modulator and demodulator. After the interface CPU is set by external control signals, including its modulation parameters and PLL parameters properly, CPU provides a response signal. After new parameters are set with CPU, PLL generates four reference clocks for the modified interface based on clk_in, as shown in Table 1.

After being set with new parameters, MDPCM modulator loads data through a bit width programmable bus and generates a modulated waveform with clk_outT2 and then responses to CPU. MDPCM demodulator monitors the input waveform and demodulates those waveform based on clk_outR2 if an effective modulated waveform is detected.

Figure 4 shows MDPCM modulator and demodulator have a controller to communicate with the CPU of an interface and to set parameters into a modulator or demodulator. MDPCM is a cycle modulation technology and its data transfer rate is changing with the data within the symbol and so, an input or output data latch is necessary for modulation or demodulation. From Eq. 1 and 2, the mapping schemes used for MDPCM supports binary or gray mapping, so a mapper or anti-mapper is also necessary. MDPCM Generator and Identifier are the key parts of modulator or demodulator and can be used to generate a MDPCM waveform or demodulate a MDPCM waveform received.

Figure 5 shows the modified interface proposed in this study can be integrated into any integrated circuits, to support either transmission or reception, or integrated transceiver function. If multiple channels are used with a modified bus, the efficiency of the modified bus can be increased in the form of index.

PERFORMANCE ANALYSIS OF MODIFIED INTERFACE

Figure 6 shows theoretical simulations have been done to evaluate the data transfer performance of a modified interface. As shown in Fig. 6a, the modified interface can be used at a fixed data transfer rate to reduce the bandwidth and the switching frequency requirements, thereby reducing the design complexity of a high-speed system. As shown in Fig. 6b, the modified interface can also be used at fixed bandwidth to achieve a higher data

Table 1: Four reference clock for modified interface

	Clocks	Properties	Functions
Modulator	clk_outT1	Low-speed	Data load reference clock before modulator
	clk_outT2	High-speed	Reference clocks for MDPCM modulator
Demodulator	clk_outR1	Low-speed	Data output reference clock after demodulator
	clk_outR2	High-speed	Reference clocks for MDPCM demodulator

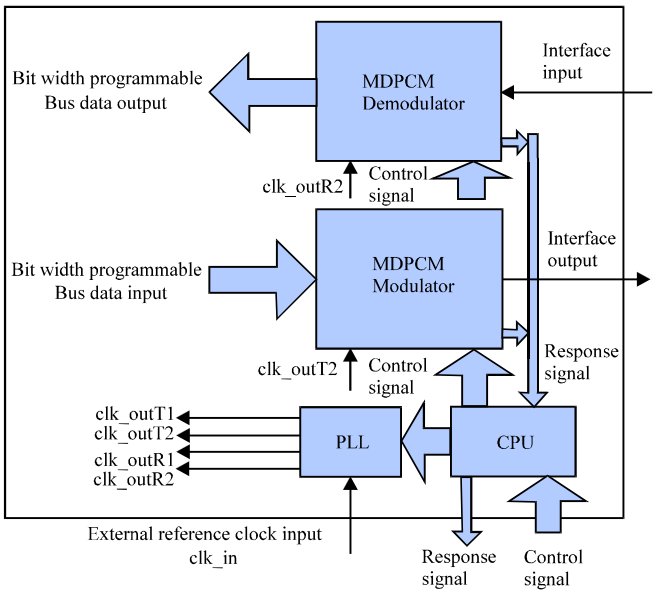


Fig. 3: Block diagram of modified high-speed digital interface

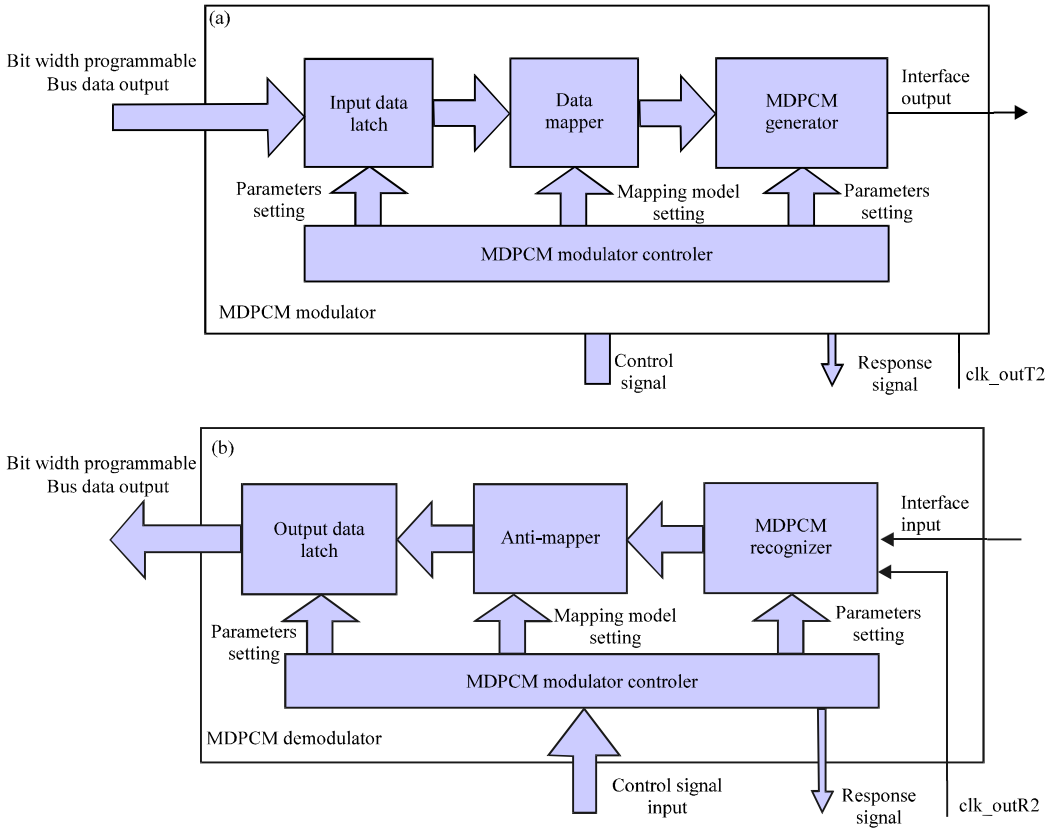


Fig. 4(a-b): Block diagram of m-ary digital pulse cycle modulation (a) Modulator and (b) Demodulator

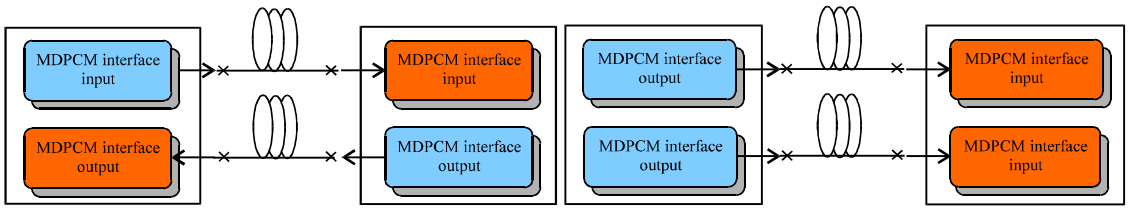


Fig. 5: Connection diagram between two integrated circuits with modified interface

transfer rate when the bandwidth is limited by a key device in a system. This result provides more positive significance to a bandwidth-limited system.

A demonstration system is developed to study the applicability of a modified interface in industrial surroundings. As shown in Fig.7, the demonstration system uses a communication distance of about 50 m between two PXI5310. PXI5310 is an industrial communication board which provides ten isolated channels of RS422 and RS232 serial buses. The demonstration system uses Altera FPGA EP3C55F484I7 on PXI5310 to simulate the modified interface and output the MDPCM waveform to a RS232 serial bus. An oscilloscope is used to monitor the transfer waveform, channel one for the signal on RS232 bus and channel two for the signal input FPGA of the receiver. Those processes are controlled using a computer through a National Instruments general-purpose PXI chassis, PXI-1000 B.

It can be seen from the experimental results of maximum data transfer rate of a demonstration system that, the data transfer rate achievable with a conventional interface is 320 kbps maximum. In addition, although the waveforms shown in Fig. 8 can still be received and demodulated properly, it is apparent that the transfer square wave in RS232 bus has been seriously deteriorated into a triangular wave.

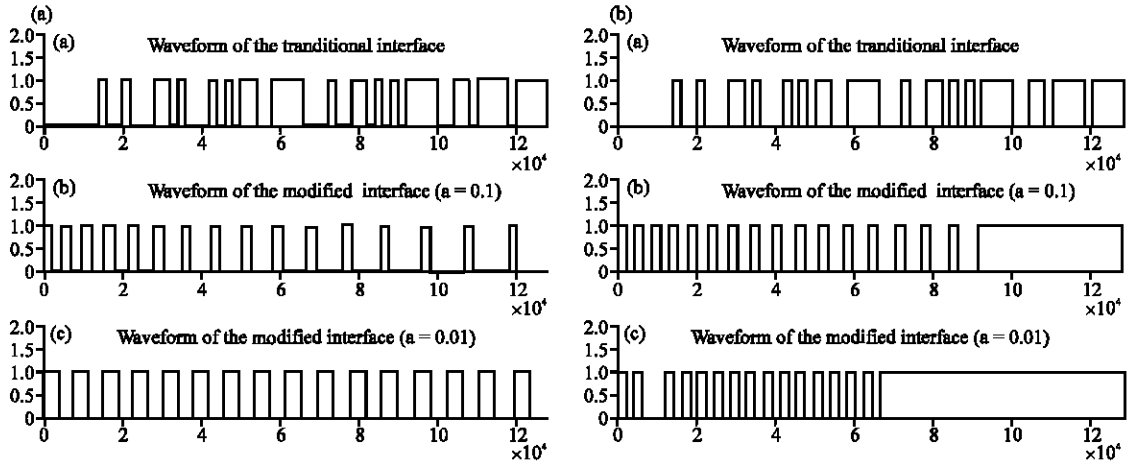
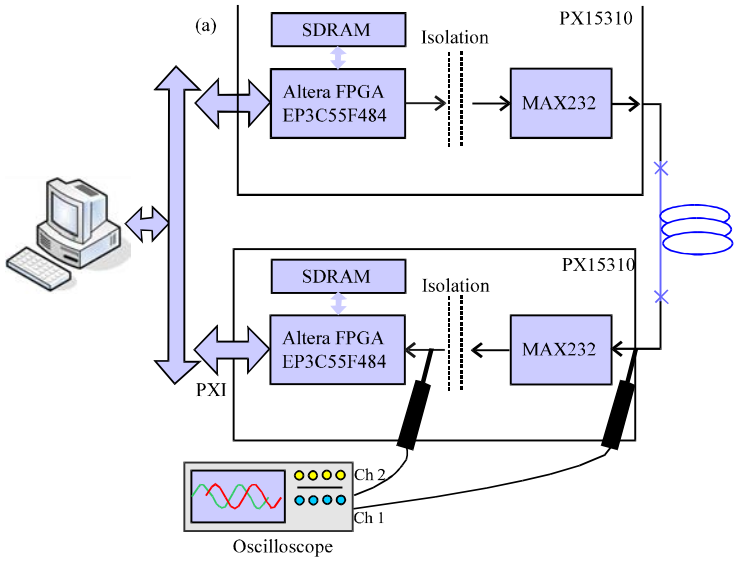


Fig. 6(a-b): Comparison between modified interface and conventional interface (a) With data transfer rate fixed and (b) With bandwidth fixed



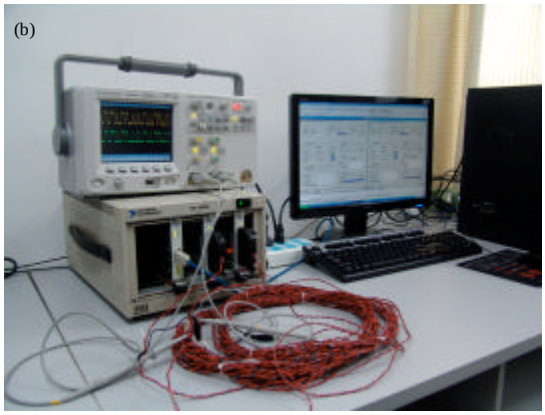


Fig. 7(a-b): Performance demonstration system for modified interface (a) System diagram and (b) Test surrounding

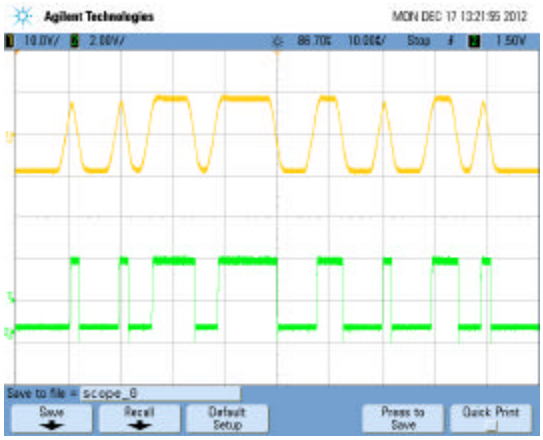


Fig. 8: Conventional interface waveforms of a demonstration system with R_b = 320 Kbps

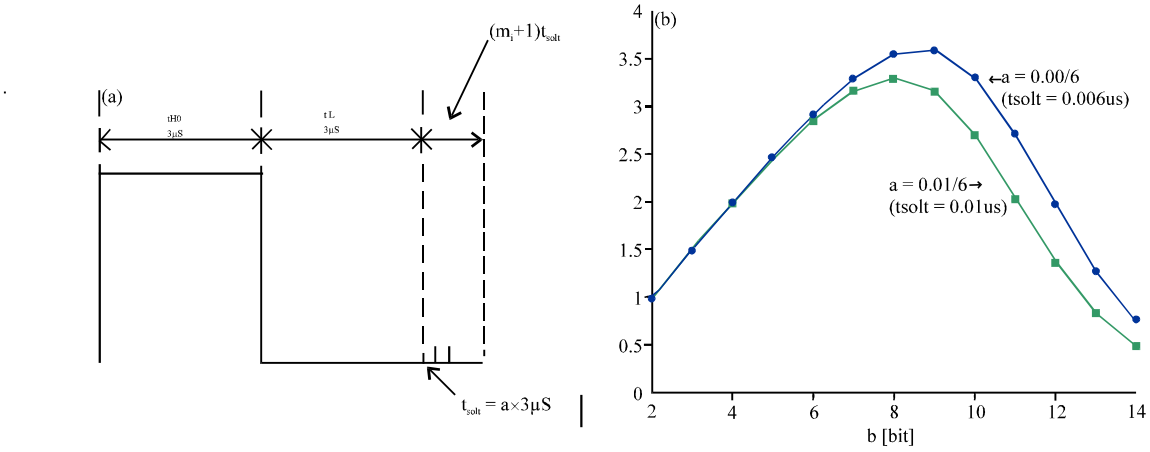


Fig. 9(a-b): (a) Waveforms designed for modified interface and (b) Bandwidth efficiency curves, for demonstration system with modified interface

The parameters set with the modified interface can also be referred to the conclusion of Fig. 8. Both t_{H0} and t_{L0} are fixed 3 us to ensure this waveform can be received and demodulated properly. As shown in Fig. 9a, the modified interface can be used to improve the data transfer rate of a RS232 bus by changing the duration of t_{slot}. In order to make sure a proper signal transmission, the ±1 counting error of a transceiver counter and a certain interference resistance must be taken into consideration. It can be seen from the obtained with a demonstration system that, the transfer waveform of a modified interface with t_{slot} setting of 0.006 and 0.01 us can be received and demodulated properly. The relationship between bandwidth efficiency r of a modified interface and bit width b with t_{solt} is 0.006 or 0.01us as shown in Fig. 9b. It is obvious that maximum equivalent data transfer rate of 1145.9 Kbps can be obtained when t_{solt} is 0.006 us and b equals 9 and maximum equivalent transfer rate of about 1054.08 Kbps can be obtained when t_{slot} is 0.01 us and b equals 8.

Figure 10 shows, for a data transfer strategy ranging from 0 to 511, the experimental waveform for t_{slot} is 0.006us or 0.01us and b is 9. Of course, the modified interface transfer waveform in RS232 bus has also been seriously deteriorated. However, the modified interface is sensitive to the rising edge of a transfer waveform only and so, a deteriorated waveform can also be received and demodulated properly. Other experiments made with different b have also been completed and a summary of experimental results are shown in Table 2. According to the experimental results, the equivalent maximum data transfer rate is changed when t_{slot}, b, or M is changed.

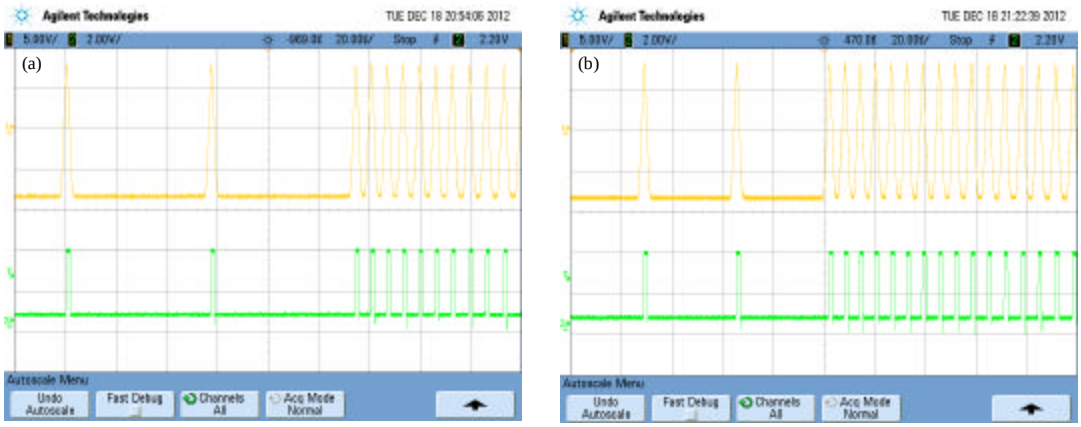


Fig. 10(a-b): Waveforms of modified interface with t_{slot} changed (a) t_{slot} = 0.01 us (R_b=1008 Kbps) and (b) t_{slot} = 0.006 us (R_b = 1145 Kbps)

Table 2: Performance of modified interface verified by demonstration system

t_{slot}(us)	0.01	0.01	0.01	0.006	0.006	0.006
a	0.01/6	0.01/6	0.01/6	0.006/6	0.006/6	0.006/6
b	7	8	9	8	9	10
M	128	256	512	256	512	1024
r	3.16	3.294	3.152	3.545	3.581	3.306
R_b(Kbps)	1011.2	1054.08	1008.64	1134.4	1145.9	1057.9

t_{slot}: Time-resolved interval between adjacent modified interface symbols, a: Rate of t_{slot} to t_{BS}, b: Values of tuples of modified interface and $M = 2^b$, r: Bandwidth efficiency of the modified interface and R_b: Data transfer rate of modified interface using RS232 bus

When t_{solt} is 0.006 or 0.01 us, the equivalent maximum data transfer rate is more than 1Mbps if the value of b is 7, 8, 9 or 10. On the other hand, according to the specification of RS232 bus, the maximum data transfer rate of RS232 bus is no more than 300 Kbps for reliable transmission (Sun and Dazhong, 2006), if a higher data transfer rate is needed, for example 1Mbps, it is must to change the hardware structure and using a another universal asynchronous receiver/transmitter interface. But according to the experimental results shown in Table 2, the interface proposed is used to achieve the maximum data transfer rate of more than 1Mbps, without any other change in hardware circuit.

It can be seen from Fig. 10 and Table 2, the duration of t_{solt} has a direct effect on the data transfer rate and a smaller t_{solt} can reduce the duration of a transfer waveform and achieve a higher data transfer rate. However, it is can also reduce its resistance to an external interference. On the other hand, a bigger t_{solt} will prolong the duration of a transfer waveform and reduces the data transfer rate. It is very important to strike a compromise between data transfer rate and resistance to interface before parameters are set with the modified interface proposed in this study.

CONCLUSION

A modified interface is proposed in this study to improve the bandwidth efficiency of a communication system. The modified interface can be used not only to reduce the complexity of circuit design but also to improve the data transfer rate of a bandwidth-limited system. A demonstration system is built using two FPGA to simulate the modified interface proposed. The feasibility and validity of the modified interface are verified through comparison of data transfer performance.

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