http://ansinet.com/itj

ITJ

ISSN 1812-5638

INFORMATION TECHNOLOGY JOURNAL

ANSInet
Asian Network for Scientific Information
308 Lasani Town, Sargodha Road, Faisalabad - Pakistan

Information Technology Journal 12 (8): 1620-1625, 2013
ISSN 1812-5638 / DOI: 10.3923/itj.2013.1620.1625

Research and Application of Surface Image Acquisition System for Sheet Material Defect Inspection

[1]Qiwu Luo, [1,2]Yigang He, [1]Wenxin Yu and [1]Jian Zheng
[1]College of Electrical and Information Engineering, Hunan University, Changsha, Hunan 410082, China
[2]School of Electrical and Automation Engineering, Hefei University of Technology, Hefei, Anhui 230009, China

Abstract: Real time quality control based on machine visual in sheet material industries is becoming a crucial technology. During the defect inspection process, surface image acquisition which is the first significant step, is challenging since fast manufacture speed and various tough condition. Choosing DS90CR288A, DS90LV047 and DS90LV019 for series-parallel data conversion and command interaction, this study presents a hardware architectural structure and turns it into reality, then develops driver program embedded into Field Programmable Gate Array (FPGA), we reduces the signal crosstalk through using reasonable termination, differential pairs controlling and the division of ground etc. The data transfer rate of this image acquisition system can reach up to 5.12 Gbps when pixel clock is up to 80 MHZ with an excellent performance. And it has already been applied to a hot rolling strip surface inspection system steadily for more than one year.

Key words: Defect inspection, field programmable gate array, differential pairs, camera link, high speed line-scan digital camera

INTRODUCTION

The strip surface quality inspection is one of the crucial techniques in the industry of automatic steel rolling and its online characteristic is the important focus and difficult point (Wang *et al*., 2009; Pernkopf, 2004; Jia *et al*., 2004) On one hand, as a result of the serious wicked operation condition, the steel surface images are noisy and blurred (Ghorai *et al*., 2013), on another hand, with the rapid development of machine vision technology, an increasing number of high speed line-scan digital cameras are widely used in lots of areas, most of which are equipped with Camera link interface because of the high image data acquisition rate, generally higher than the 1 Gbps. Nearly all this camera producers also provide camera image acquisition board with related hardware driver program, completing the data transmission to the host for the follow-up image processing. Because large amounts of instruction need to be executed serially, the traditional approach can not meet the real time requirements of image processing and algorithm analysis (Hu *et al*., 2006). Thus, hardware implementation method to embed image algorithm into processor units such as FPGAs becomes necessary and significant.

This system adopts high-speed cameras with camera link interface installed inside and also adopts various image processing algorithms and chooses different main processors according to different image features. In addition, the main processing for the same project can be changed at different stages, when high-speed cameras with camera link interface come to application, the repeated design of high-speed LVDS signal would be involved inescapably. Because LVDS signal keeps high requirements on PCB layer settings, impedance matching and topology of power supply system, any misconduct in above stages may lead to lower image transmission speed and quality, especially poor communication caused by plenty of signal crosstalk. Sometimes, we also need to redesign the whole hardware system even though the remaining parts of the image acquisition and processing board are still in good performance which means a tremendous waste of R and D time and investment.

In this study, we developed a hardware architectural structure which supports full model for camera link interface, according to this schematic, one 4-layer Print Circuit Board (PCB) was realized, then we finished the

Corresponding Author: Qiwu Luo, College of Electrical and Information Engineering, Hunan University, Changsha, Hunan 410082, China

corresponding image acquisition driver program based on FPGA. Finally, we applied the brand-new image acquisition board in a hot rolling strip surface inspection system and it worked steadily for more than one year.

ARCHITECTURAL STRUCTURE DESIGN

In order to avoid inconvenience caused by various standards of communication interface from different camera and image acquisition board manufacturers, Camera link protocol which can simplify the image acquisition interface was proposed by NIC (2000) and the related cameras providers (such as Basler, Dalsa etc.). Until now, it has been widely used in the field of machine vision. The design of hardware architectural structure of Camera link interface is shown in Fig. 1. This board is connected to industrial camera through MDR 26 interface with Camera link cable. The length of Camera link cable between them should be customized according to the site situation. Normally, the 3 m is recommended while, the maximum supportable length is 12 m. If the transmitting distance is longer than 12 m, optical transmitter and receiver would be used to convert the electric signal into optical signal for transmission. The signal standard between MDR26 interface and electric level conversion chip (DS90CR288A, DS90LV047 and DS90LV019) is Low Voltage Differential Signal (LVDS) while that between electric level conversion chip and RAMON General

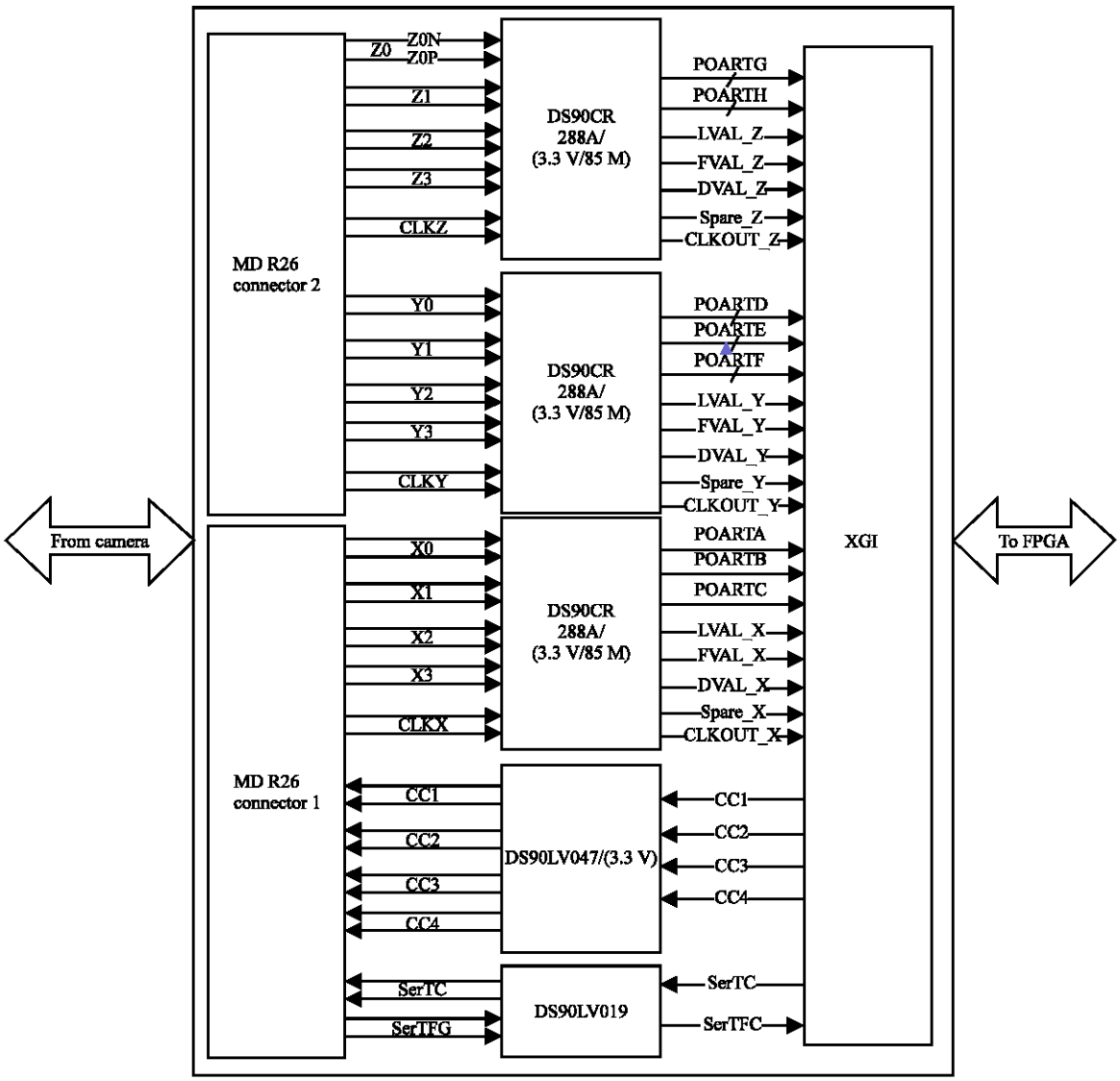

Fig. 1: Hardware architectural structure

Interface (RGI) is CMOS / TTL (TIC, 2004). In addition, the Xilinx General Interface (XGI) which complies with the Xilinx enterprise standard can be flexibly used together with certain image processing board.

The hardware supports three types of model which are Full, Medium and Base model with the POARTA~POARTH for Full model, POARTA~POARTF for Medium model and POARTA~POARTC for Base model. Among them, Full/Medium model takes the interface No.1 and 2 of MDR26 while Base mode takes the interface No. 1.

HARDWARE IMPLEMENTATION AND TESTING

Hardware implementation: According to the standard of camera link protocol (NIC, 2000), frequency of the LVDS signal is 7 times as high as that of CMOS/TTL signal. If the pixel clock of high-speed camera is 80 MHZ, the bus frequency of LVDS inserted from MDR 26 interface to the electric level conversion chip would be high up to 560 MHZ. According to the theory of transmission line, in order to reduce the signal interference, the impedance of LVDS line must be controlled at 100 ohms (±5%). The PCB layer structure is shown in Fig. 2 with its parameters shown in Table 1.

Table 1: Board layer parameters

Layer No.	Electronic net	Technical parameters
1st layer	Top	0.5 oz
Interlayer	Dielectric layer	FR4 (0.13 mm)
2nd layer	GND	1 oz
Interlayer	Dielectric layer	FR4 (1.34 mm)
3rd layer	VCC	1 oz
Interlayer	Dielectric layer	FR4 (0.13 mm)
4th layer	Bottom	0.5 oz

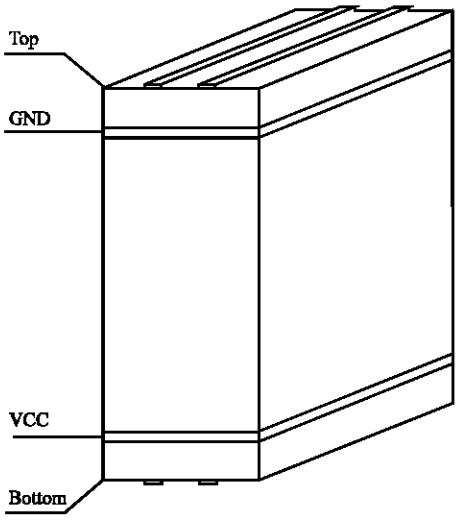

Fig. 2: 4-layer structure

The total thickness of PCB is around 1.6 mm and constant of dielectric is about 4.3. Due to one sixth rising electrical length of PCB high speed LVDS signal is around 0.09 inch which is slightly narrower than the PCB line length, so terminator is necessary (Luo and Li, 2010). The red zone shown in Fig. 3 is the LVDS signal line which needs to meet differential and isometric requirement. In order to minimize the signal 1st-reflection, 100-ohm impedance termination is necessary and important near the electric level conversion chips.

Hardware testing: Hardware testing was divided into two parts which were circuit debugging and driver development. According to the parameters requirement described in Table 1, we generated the PCB gerber files, provided them to the PCB producers and finished PCB impedance test strictly. When the results met the standards, all the chips and components were welded on the board. After that, high-speed camera could be connected to the MDR 26 connector, so image signal was imported to this acquisition system. Then we adjusted the line clock, working pattern, pixel clock and gain of the camera for the high-quality image. Through Agilent oscilloscope DSO-X 3052A, we could observe and check the waveform before and after the electric level conversion chip to ensure the correctness of waveform. The test results of 80MHz differential pixel clocks were given in Fig. 4. As shown in Fig. 4, the board we designed presented an excellent performance and successfully met the requirement of Gbps-grade image acquisition.

Using VHDL language, we developed the image acquisition driver programs and packaged them into the Intellectual Property Core (IP Core). This kind of IP core

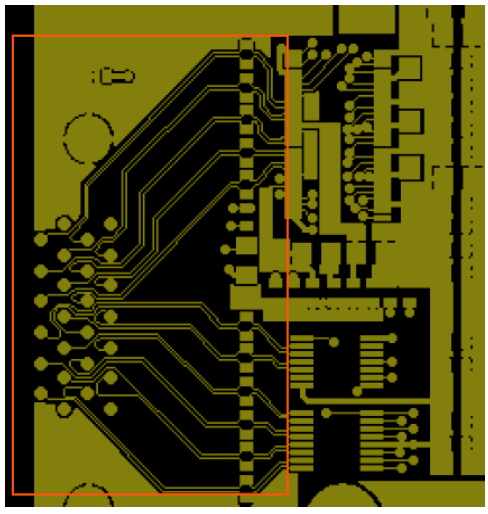

Fig. 3: PCB layout on allegro

could be constituted in surface defect on-line inspection system conveniently and flexibly through supplied Processor Local Bus (PLB) interface (supporting MicroBlaze, PowerPC). Besides to open handover signal transmitted to image processing unit, the virtual logic analyzer IP Core (Chipscope Integrated Controller, Chipscope Integrated Logic Analyzer) was embedded in the driver program. After setting the capture depth and width of signal, we could monitor all the internal signals in the FPGA. As shown in Fig. 5, it was the data of a line

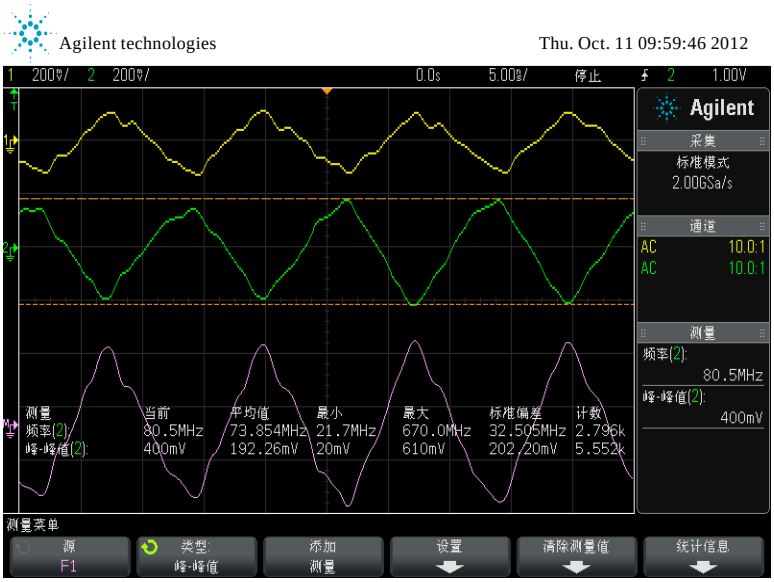

Fig. 4: Waveform on oscilloscope of differential pixel clock

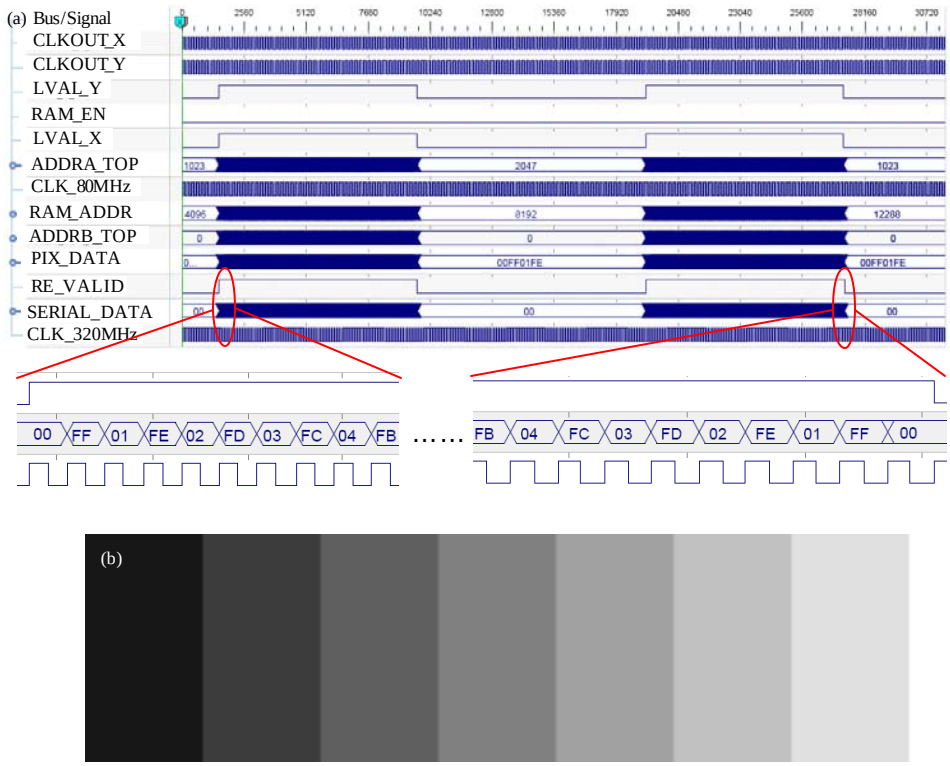

Fig. 5(a-b): (a) Debugging result on embedded chipscope and (b) Test image under “fixed gray gradient” mode

image transmitted from DALSA line-scan camera in Medium mode under "fixed gray gradient" mode (DTC, 2005), where CLKOUT_X and CLKOUT_Y were pixel clock signals, LVAL_X and LVAL_Y were line valid signals. In order to insure the steady image data, we adopted ping-pong approach, when the former line data was under acquisition process, the latter line data was under storage process which means the acquisition and storage process executed one after another. It can be seen clearly from Fig. 5a and b that the brand-new board finished the imagine acquisition correctly with good signal integrity.

APPLICATION CASE

In the continuous steel rolling and casting industry, there are a large number of defects such as: roller traces, foreign matters, scarring errors, scratches and spots on the slab surface caused by the fast production speed, occasional faults of rolling or casting machine, current environmental changes, operators lacking of professional skills and inescapable maturing of rollers. These quality defects are serious threats to quality of strips and finished product ratio which means huge loss to producers and sometimes may lead claim event. This system has been applied in a Chinese steel plant successfully and steadily and got a high evaluation by leaders of that steel plat. The related parameters on site are as follows: the rolling speed is up to 18 m sec^{-1}, the width is less than 1.65 m and the resolution radio of target defects is 0.5×0.5 mm. Figure 6a is the photo of the image acquisition system which has been installed on the image processing board. An image sample of strip surface is shown in Fig. 6b as well.

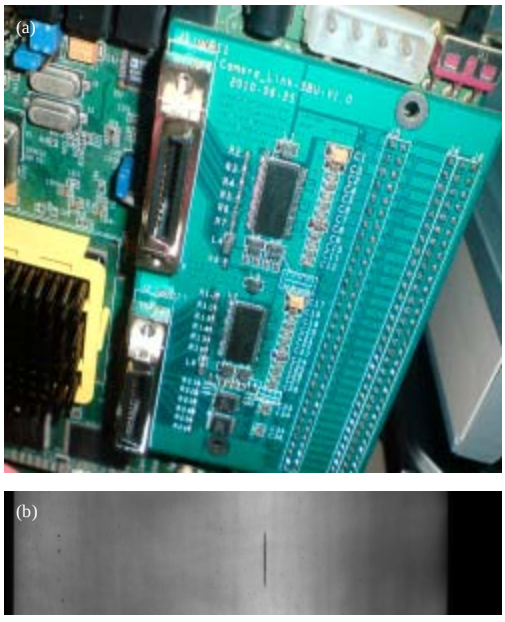

Fig. 6(a-b): (a) Photo of the image acquisition system and (b) Photo sample of steel strips

CONCLUSION

The hardware scheme and diver program of the new designed Camera link have been successfully realized and applied to surface defect online inspection equipment for hot rolling strips as standard parts in the field of image acquisition and processing. The standard configuration is Full model, but Medium and Base models are compatible. When camera pixel clock is up to 80 MHZ, the data transfer rate can reach up to 5.12 Gbps with an excellent and steady performance of image acquisition.

ACKNOWLEDGMENT

This study was supported by the National Natural Science Funds of China for Distinguished Young Scholar under Grant No. 50925727, The National Defense Advanced Research Project Grant No. C1120110004 and 9140A27020211DZ5102, Hunan Provincial Science and Technology Foundation of China under Grant No.2010J4 and 2011JK2023, the Key Grant Project of Chinese Ministry of Education under Grant No.313018.

The authors would like to express their gratitude to Lu TIAN and his image processing team members of steel surface defect inspection system in RAMON Tech. Co., Ltd., for their assistance to this research project.

REFERENCES

DTC, 2005. Piranha enhanced sensitivity camera user's manual. Teledyne DALSA Inc., pp: 72-74. http://www.teledynedalsa.com/imaging/products/cameras/line-scan/piranha-es/ES-80-04K40/

Ghorai, S., A. Mukherjee, M. Gangadaran and P.K. Dytta, 2013. Automatic defect detection on hot-rolled flat steel products. IEEE Trans. On Instru. Measure., 62: 612-621.

Hu, L., F.J. Duan and D.Q. Ding, 2006. The application of FPGA-based image processing technology in surface defect inspection system for steel strip. Chinese J. Sens. Actuat., 19: 694-701.

Jia, H., Y.L. Murphey, J. Shi and T.S. Chang, 2004. An intelligent real-time vision system for surface defect detection. Proc. 17th Int. Conf. Pattern Recogn., 3: 239-242.

Luo, Q.W. and F.H. Li, 2010. Design and implementation of data acquisition system based FPGA. Comput. Measur. Control, 18: 2656-2658.

NIC, 2000. Specifications of the camera link interface standard for digital cameras and frame grabbers. QImaging Inc., Surrey, BC, Canada, pp: 7-13.

Pernkopf, F., 2004. Detection of surface defects on raw steel blocks using Bayesian network classifiers. Pattern Anal. Appl., 7: 333-342.

TIC, 2004. DS90CR287/DS90CR288A+3.3V rising edge data strobe LVDS 28-bit channel link-85 MHZ. Texas Instruments Incorporated, pp: 1-2. http://www.ti.com.cn/cn/lit/ds/symlink/ds90cr287.pdf

Wang, Z.C., Z.Z. Wu and L. Feng, 2009. Design and implementation of a surface defect inspection system for steel sheets. Comput. Eng. Sci., 31: 61-65.