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General Optimization Algorithm for Capacitor Voltage Balance of Multilevel Inverters

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Abstract: A simple equivalent circuit of multilevel inverters to predict the deviation of node voltages was analyzed and the capacitor voltage imbalance mechanism of diode clamped multilevel inverter was analyzed. An optimization algorithm of Space Vector Pulse Width Modulation (SVPWM) for capacitor voltage balance of diode clamped multilevel inverters is presented. This algorithm predicts the deviation of node voltages for different operation modes to develop an optimization algorithm to minimize the voltage deviation among different capacitors. This algorithm selects the best switch combinations during each switching cycle to reach node voltage balance. This algorithm is naturally applicable to inverters with an arbitrary number of levels. The simulation and experimental results verify the correctness of this algorithm.

Key words: Multilevel inverters, voltage balance of capacitors, space vector pulse width modulation

INTRODUCTION

At present, multilevel converters has been achieved wide range of applications in the field of high-voltage AC drive, wind power, the new DC transmission and reactive power compensation (Colak *et al*., 2011; Xia *et al*., 2011; Hochgraf and Lasseter, 1997; Mishra *et al*., 2003). Diode clamped without the need the separate DC power supply has been extensively studied. But voltage balance of DC link capacitors is a special problem in that topology, when the inverter more than three-level the capacitors balance control algorithm will become complicated. Different solutions were proposed to overcome this problem. Additional circuitry to inject or extract current to the capacitor was presented (Akagi *et al*., 2008; Hasegawa and Akagi, 2011; Sano and Fujita, 2008; Seo *et al*., 2001), but this way increases the hardware and the size of system with reducing efficiency. The algorithm using redundant state to change the action time of positive and negative small vector was proposed to control the balance of the capacitor voltage (Lee *et al*., 1996; Celanovic and Boroyevich, 2000; Dou *et al*., 2008; Lewicki *et al*., 2011; Hatti *et al*., 2008). But this method is suitable for three-level and is difficult to be extended to multi-level. The capacitor voltage balance control method for back to back multilevel converter can achieve the power flow in both directions (Pan and Peng, 2009; Ishida *et al*., 2002; Saeedifard *et al*., 2009; Busquets-Monge *et al*., 2011). However, this approach only applies to the back to back multilevel converter generating the extra device, complexity and the higher cost.

In this study, a simple equivalent model of the multilevel inverter was established and the SVPWM algorithm based on the 60° coordinate system was studied. A universal optimized SVPWM algorithm for multilevel inverter capacitor voltage balance was presented. This algorithm selects the optimal switching combinations during each switching cycle by predicting DC-side node voltage deviation under different switching state to achieve the balance of node voltage, as well as capacitor voltage balance. Simulation and experimental results are presented for three and five level inverter to verify the effectiveness of this optimal algorithm.

EQUIVALENT CIRCUIT OF DIODE CLAMPED MULTILEVEL INVERTER

Diode clamped N-level inverter equivalent model is presented in Fig. 1. The current i_m is flowing from the generic node m. The voltage of node m opposed to node 0 is:

$$V_{m\text{-}ref} = mV_{dc}/(N-2) \quad (1)$$

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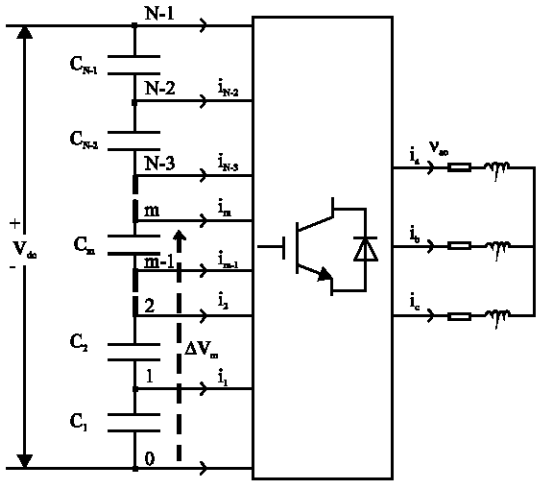

Fig. 1: Equivalent circuit of diode clamped N-level inverters

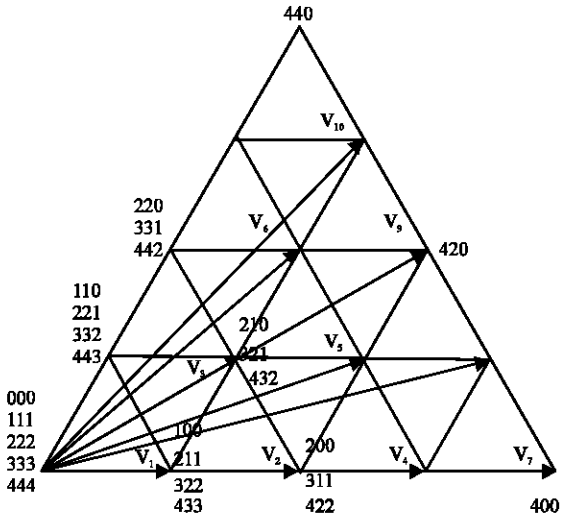

Fig. 2: First sector of five-level voltage space vector

Respectively define the switch variables S_a, S_b and S_c as A, B, C three-phase switching state and the range is [0, 1, 2...N-1]. Set V_{dc} = (N-1) E, the A-phase output voltage is:

$$v_{ao} = (S_a-2)V_{dc}/(n-1) = (S_a-2)E \quad (2)$$

Voltage space vector is defined in the complex plane:

$$V = 2(V_a+V_b e^{12\pi/3}+V_c e^{-j2\pi/3})/3 \quad (3)$$

When the switch variables S_a, S_b and S_c simultaneously increase or reduce the integer N and satisfy 0 = S_a-N, S_b-N, S_c-N = N-1, the synthesis of space voltage vector is unchanged. Therefore, a basic voltage vector may correspond to the multiple switch status.

CAPACITORVOLTAGEIMBALANCEMECHANISM OF MULTILEVEL INVERTER

From the equivalent model of the diode clamped N-level inverter shown in Fig. 1, the size of current i_m which inflows or outflows the node m and the time dT during which the node m is charged or discharged was different. And those differences produce the node voltage deviation. The current i_m that outflow from node m is:

$$i_m = \delta(S_a-m)i_a+\delta(S_b-m)i_b+\delta(S_c-m)i_c \quad (4)$$

where i_a, i_b and i_c are three-phase load currents:

$$i_a+i_b+i_c = 0 \quad (5)$$

$$\delta(i)=\begin{cases}0, & i\neq 0\\ 1, & i=0\end{cases} \quad (6)$$

Selecting a different switch state (S_a, S_b and S_c), i_m is different. When i_m is not zero, the node m is charged or discharged causing the voltage deviation. When i_m>0, the node m is discharged; when i_m<0, the node m was charged; when i_m = 0, the node voltage is unchanged. Different switching states of the same voltage vector have different impact on each node. So, this algorithm dynamically selects the optimal switching state in order to minimize the node voltage deviation.

In order to fully illustrate the imbalance mechanism of diode clamped multilevel inverter, the first sector of the first sector of the space voltage vector diagram shown in Fig. 2 is analyzed, similarly to the other sectors. Table 1 and 2, respectively give each voltage vector, the corresponding switching states and the charging or discharging current of each node in the first sector for a three and five level inverter. As long as the load power factor is not zero, there is the phenomenon of the capacitor voltage imbalance.

As shown in Table 1, the switch states corresponding to the voltage vector V_1 either charge or discharge the node 1. Switch state corresponding to V_2 have no impact on the voltage of node 1, as charging or discharging current is zero. Switch state corresponding to V_3 charge or discharge node 1 all along. Therefore, by dynamically selecting the redundant switching state of the V_1, the node voltage can maintain balance.

Table 1: Node currents of three level inverter

Voltage vector	Switch state	i_1
V_1	100	i_a
	211	$-i_a$
V_2	200	0
V_3	210	i_b

Table 2: Node currents of five-level inverter

Voltage vector	Switch state	i_1	i_2	i_3
V_1	100	i_a	0	0
	211	$-i_a$	i_a	0
	322	0	$-i_a$	i_a
	433	0	0	$-i_a$
V_2	200	0	i_a	0
	311	$-i_a$	0	i_a
	422	0	$-i_a$	0
V_3	210	i_b	i_a	0
	321	i_c	i_b	i_a
	432	0	i_c	i_b
V_4	300	0	0	i_a
	411	$-i_a$	0	0
V_5	310	i_b	0	i_a
	421	i_c	i_b	0
V_6	320	0	i_b	i_a
	431	i_c	0	i_b
V_7	400	0	0	0
V_8	410	i_b	0	0
V_9	420	0	i_b	0
V_{10}	430	0	0	i_b

As shown in Table 2, the five-level voltage vector V_1, V_2 and V_7 is balance voltage vector while the switch states corresponding to the rest of the voltage vector charge or discharge one or more nodes all along. Thus, the greater the voltage vector modulation is, the greater the imbalance of node voltage is. When the modulation is greater than 0.5, the node voltage cannot keep balance only by dynamically selecting the redundant switching state, unless by rounding a lot of unbalanced voltage vector.

Equivalent Capacitance of node m can be formed by the connection of m capacitors in series, between node m and 0, in parallel with the series of (N-1-m) capacitors, between node m and N-1. Set the value of DC side capacitor is C and then the equivalent capacitance of node m is:

$$C_{m\_eq} = \frac{C}{m} + \frac{C}{N-1-m} \tag{7}$$

The voltage deviation of node m is:

$$\Delta V_m = \frac{1}{C_{m\_eq}} \int_{t_0}^{t_0+dT} i_m(t)\,dt \tag{8}$$

If the current $i_m(t)$ may be considered constant within the interval dT, then the voltage deviation is simplified to:

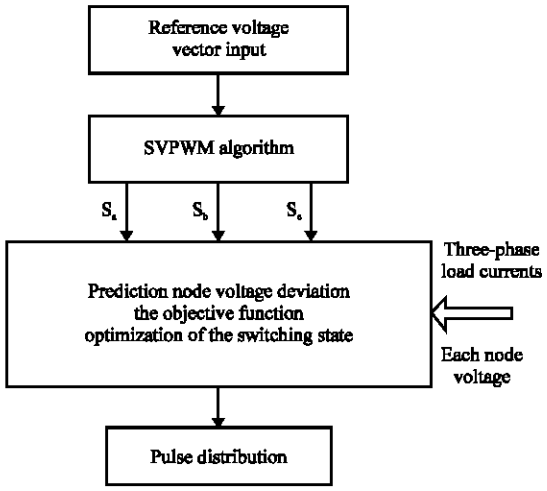

Fig. 3: Optimization SVPWM flow chart

$$\Delta V_m \approx \frac{i_m(t_0)\,dT}{C_{m\_eq}} \tag{9}$$

Define the action time of three basic voltage vectors which synthesize reference voltage vector V_{ref} is t_x, the corresponding switching state is (S_{xa}, S_{xb}, S_{xc}), voltage deviation of the node m is Δv_{mx}, where x = 1, 2 and 3. Putting 4 into 9, node voltage deviation during action time of each the basic voltage vector is:

$$\Delta V_{mx} = \frac{(\delta(S_{xa}-m)i_a + \delta(S_{xb}-m)i_b + \delta(S_{xc}-m)i_c)t_x}{C_{m\_eq}} \tag{10}$$

Optimization algorithm: According to the value and direction of the node voltage deviation, optimal redundancy switch state can be selected to control the balance of the node voltage for diode clamped multilevel inverter. This paper presents an optimization SVPWM algorithm of which flow chart is shown in Fig. 3. This algorithm predicts the deviation of node voltages for different operation modes to develop an optimization algorithm to minimize the voltage deviation among different capacitors.

This algorithm can accurately predict the node voltage deviation at next time and establish the objective function. During each switching cycle, optimization of the all switch status was completed in order to minimize the objective function, in other words, minimizing the node voltage deviation of the next time ultimately to achieve node voltage balance. The disadvantage of this algorithm do not consider the principle of minimum switching, it may increase the switching losses.

Define the actual voltage at kT moment between node m and node 0 as $V_m(kT)$ and then the node voltage deviation is:

$$E_m(kT) = V_m(kT)-V_{m\text{-}ref} \quad (11)$$

The node voltage deviation at (k+1)T moment is predicted as:

$$E_m[k+1)T] = |E_m(kT)+\Delta V_m| \quad (12)$$

The objective function is established to optimize the switching states corresponding to a voltage space vector and then there is the minimum node voltage deviation at next time. Ultimately the inverter capacitor voltage can keep balance.

Firstly, each node voltage deviation is calculated for switch state (S_a, S_b and S_c) to predict the node voltage deviation at next time. Then select the value of the largest node voltage deviation:

$$M(S_a, S_b, S_c) = \max(\sum_{1}^{N-2} E_m[(k+1)T]) \quad (13)$$

Secondly, the optimal switching state is selected from the switching states corresponding to space voltage vector to minimize M (S_a, S_b, S_c). Then optimize the switch states corresponding to three basic voltage vectors one by one in order to control the balance of the node voltage.

SIMULATION RESEARCH

This algorithm was studied and analyzed for three and five level inverter. System parameters are as follows: the DC power V_{dc} = 1 kV, output frequency f = 50 Hz, capacitance of each DC capacitor C = 2200 μF, switching frequency f_s = 5 kHz.

Situation of the three-level inverter under different load power factor and different modulation was presented. The simulation results are shown in Fig. 4 and 5. Figure 4 shows waveforms of line output voltage and capacitor voltages with different modulation when cosϕ = 1. Figure 5 repeats waveforms of line output voltage and capacitor voltages with different modulation when cosϕ = 0.95.

The value of DC capacitor was used in the algorithm to predict node voltage deviation. However, the capacitance value of each capacitor may go awry in the practical application. This algorithm was studied and analyzed when there are the deviations of the capacitance values. Figure 6 shows waveforms of line output voltage and capacitor voltages when the power factor cosϕ = 0.95 and the modulation m = 0.9.

Simulation results show that the algorithm can effectively control the balance of the node voltage. When there is a small deviation in the capacitance, the algorithm can also be effective in controlling the balance of the node voltage.

In this study, the algorithm was extended to the multi-level. For example, five-level inverter was studied

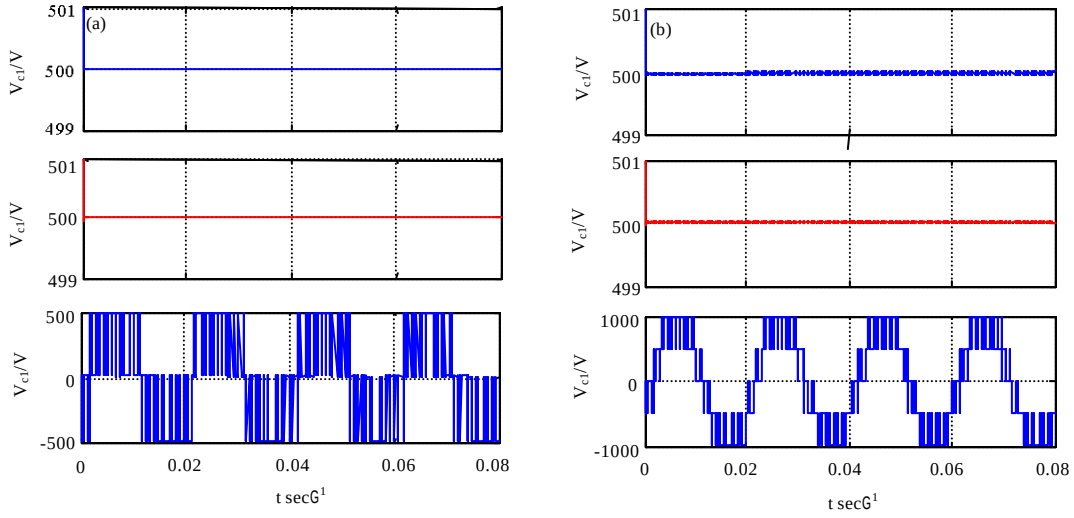

Fig. 4(a-b): Waveforms of line output voltage and capacitor voltages when cosϕ = 1 (a) M = 0.5 and (b) M = 0.9

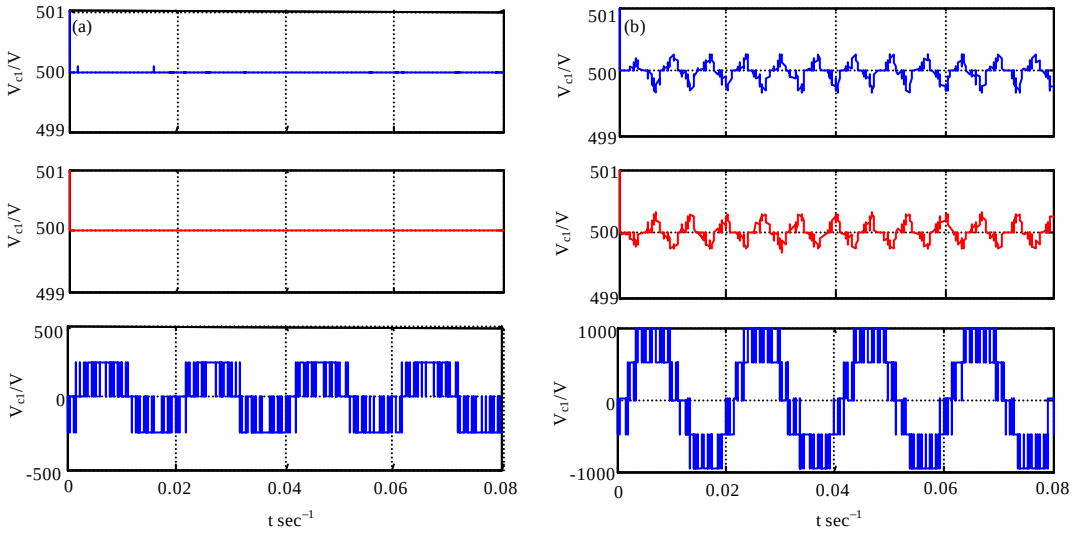

Fig. 5(a-b): Waveforms of line output voltage and capacitor voltages when cosϕ = 0.95 (a) M = 0.5 and (b) M = 0.9

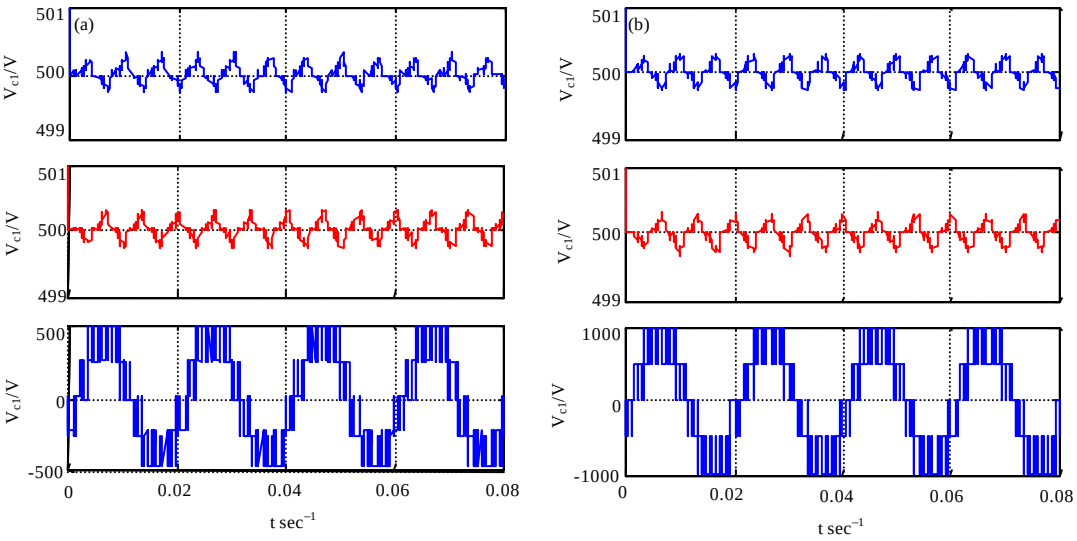

Fig. 6(a-b): Waveforms of line output voltage and capacitor voltages under different capacitance deviation, (a) C_1 = 2200 MF, C_1 = 2100 MF and (b) C_1 = 2250 MF, C_1 = 2150 MF

and analyzed with different modulation when the power factor cosϕ = 0.95. Waveforms of line output voltage and capacitor voltages with different modulation is shown in Fig. 7, in which (a), (b) and (c), respectively shows the waveforms of capacitor voltage and line voltage when m = 0.2, m = 0.5 and m = 0.8.

From Fig.7 it shows that the capacitor voltage balance method prospered by this paper can also work well when it extends to more than three-level inverter.

EQUATIONS

In this study, experimental research of the algorithm on three-level and five-level experimental platforms was presented. For the basic parameters of three-level platforms: Vdc = 550 V, DC capacitor C1 = C2 = 2200 μF, R-L load, modulation M = 0.8. The basic parameters of five-level platforms: Vdc = 350 V, DC capacitor C1 = C2 = C3 = C4 = 2200 μF, R-L load, modulation M = 0.8.

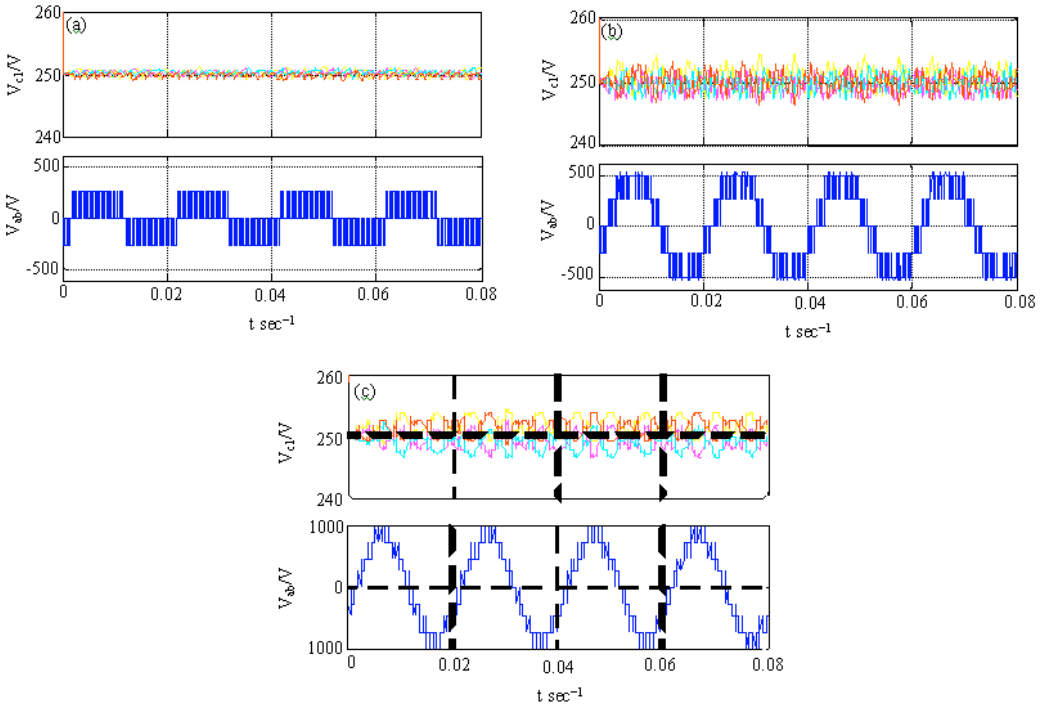

Fig. 7(a-c): Waveforms of five-level capacitor voltages and line voltage under different the modulation (a) M = 0.2, (b) M = 0.5 and (c) M = 0.8

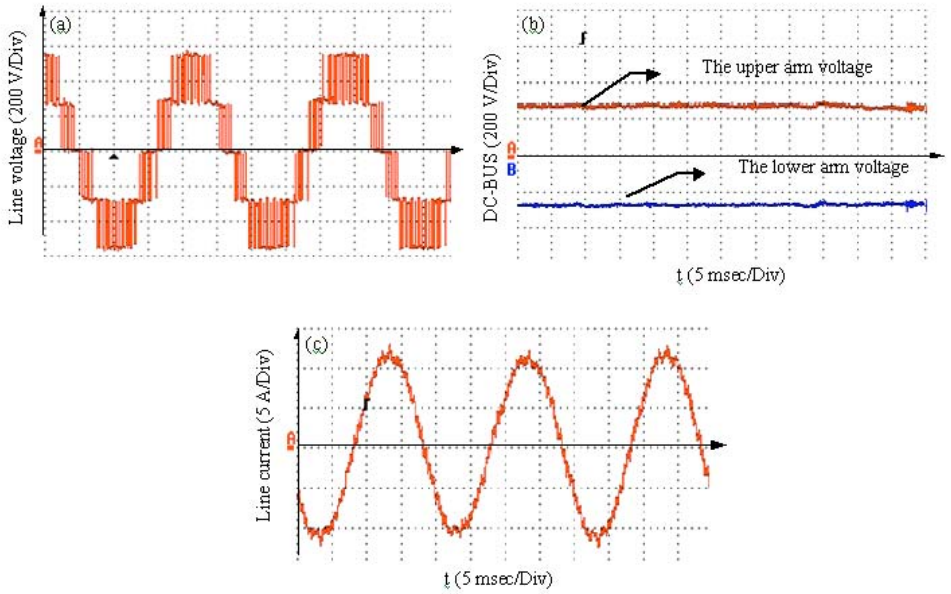

Fig. 8(a-c): Waveforms of line output voltage, capacitor voltages and load current of three-lever inverter

The experimental results of three-level inverter was shown in Fig. 8, in which (a) Presents the waveform of line voltage (b) Shows the waveform of DC-Bus voltage (c) Shows the load current. From the experimental results, the algorithm can effectively control the balance of the node voltage of DC capacitor.

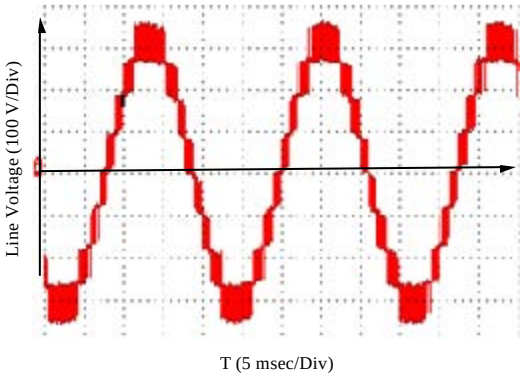

Fig. 9: Waveforms of line output voltage of five-level inverter

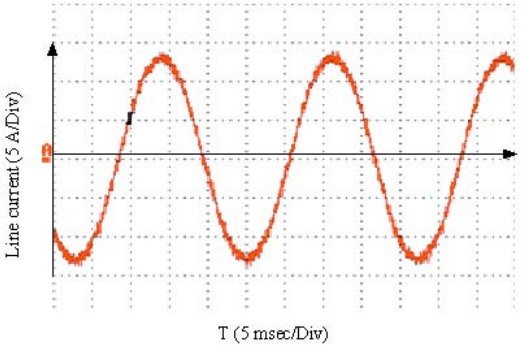

Fig. 10: Waveforms of load current of five-lever inverter

The experimental results of five-level inverter was shown in Fig. 9 and 10, in which Fig. 9 presents the waveform of line voltage, Fig. 10 shows the waveform of load current. It can be seen that the voltage steps are equal, proved the effectiveness of the capacitor balance control algorithm.

CONCLUSION

This study analyzed the capacitor voltage unbalance mechanism of the diode clamped multilevel inverter. A general optimized SVPWM algorithm for multilevel inverter capacitor voltage balance was presented. This algorithm predicts the deviation of node voltages for different operation modes to establish objective function in order to optimize the switching states corresponding to a voltage space vector and finally minimize the voltage deviation among different capacitors. The balance algorithm is confirmed by the three-level and five-level experiment platform, in theory, the algorithm is suitable for any level inverter to control the capacitor voltage balance.

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