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A State Metrics Cache Reduced Decoding Architecture for Double Binary Convolutional Turbo Code

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Abstract: The size of State Metrics Cache (SMC) has a predominant impact on overall power dissipation of double binary convolutional turbo code (DB-CTC) decoder. This study proposes a scheme to reduce the word width of SMC and hence to decrease its total size. Instead of accessing the forward state metrics from the SMC, the index sequence and the increase metric are used to estimate these forward metrics. At the cost of dummy calculation performed by the com-pressing and the regeneration modules, the SMC size is 62.5% reduced compared to that of the conventional decoding scheme. Moreover, by simplifying the multivariable max* operation, Bit Error Rate (BER) of this scheme is 0.1 dB superior to that of the enhanced Max-Log-MAP algorithm.

Key words: DB-CTC; index sequence, MAP algorithm, state metrics cache

INTRODUCTION

Turbo codes introduced by Berrou *et al*. (1993) have been demonstrated with superior error correction capabilities. In 1999, double binary convolutional turbo code (DB-CTC) was proposed (Berrou and Jezequel, 1999) and attracted hot attention due to its advantages over single binary turbo codes (Berrou *et al*., 2001). As a result, DB-CTC has been adopted as the Forward Error Correction (FEC) coding scheme by several wideband wireless communication standards (WiMAX; DVB). Recently, DB-CTC was accepted in IEEE 802.16 m (MTT-S, 2010) to guarantee reliable transmission in highly mobile scenarios.

The maximum *a posteriori* probability (MAP) algorithm is the optimal decoding algorithm for turbo-like decoder (Bahl *et al*., 1974). However, being the decoding algorithm iteratively applied, the MAP algorithm is transformed into logarithm domain, which is known as the Log-MAP algorithm, to reduce the decoding complexity. A basic turbo-like decoder consists of two soft in and soft out (SISO) constituent decoders, each one provides soft extrinsic information to the other one. The constituent decoder includes three memories, which are assigned to the soft received bits, the soft extrinsic information and the State Metrics Cache (SMC), respectively. Because of this memory-intensive decoding architecture, energy dissipation of SMC has been reported a predominant impact on turbo decoder (Liu *et al*., 2007). For DB-CTC, whose trellis diagram is much complicated, researchers have developed radix-4 traceback (Lin *et al*., 2009; Lin *et al*., 2011) and state metric compression approaches (Martina and Masera, 2011), but the tradeoff between the saved SMC area and the decoding performance is limited. This motivates the need of new techniques to further reduce the size of SMC. In this study, we propose a method to calculate the state metrics by the index sequence and the increase metric, while degradation of the decoding performance is tolerable.

This study proceeds as follows. Section II gives an introduction of the DB-CTC decoding algorithm. Section III describes how to approximate the forward state metrics in detail, while architecture of the DB-CTC decoder is also presented. Section IV evaluates SMC size and bit error rate (BER) of the proposed decoding scheme. Finally, Section V gives conclusion this study.

DB-CTC ENCODER AND DECODING ALGORITHM

Figure 1a is the DB-CTC encoder adopted by the IEEE 802.16 m standard [6], where $u_k = (u_k^a u_k^b)$ is the bit pairs of information frame and k is the time slot. Firstly, when the switch is connected to "1", u_k is input into the constituent encoder to perform the C1 encoding. Secondly, when the switch is connected to "2", the interleaved sequence of u_k is input into the constituent encoder, which is called the C2 encoding. The above steps give the encoded sequence with code rate equals to 1/3, for detailed encoding procedures about DB-CTC, please refer to (MTT-S, 2010).

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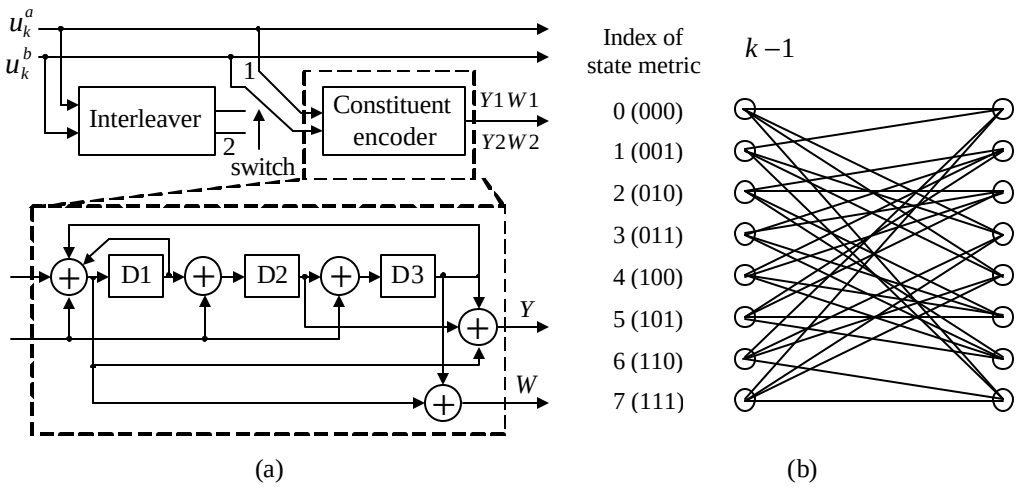

Fig. 1: DB-CTC: (a) Structure of the encoder and (b) Trellis diagram

To simplify the decoding complex, Log-MAP algorithm and its derivatives are mainly used in the implementation of turbo-like decoders. As for DB-CTC, by assuming the:

$$\gamma_k^{(z)}\left(s_{j1,k-1}, s_{j2,k}\right) = \frac{L_c}{2}\left(x_k^{s1} y_k^{s1} + x_k^{s2} y_k^{s2} + x_k^{p1} y_k^{p1} + x_k^{p2} y_k^{p2}\right) + \Lambda_{apr,k}^{(z)}(u_k) \quad (1a)$$

$$\alpha_k\left(s_{j2,k}\right) = \max_{s_{j1,k-1}}^{*}\left[\alpha_{k-1}\left(s_{j1,k-1}\right) + \gamma_k^{(z)}\left(s_{j1,k-1}, s_{j2,k}\right)\right] \quad (1b)$$

$$\beta_k\left(s_{j1,k}\right) = \max_{s_{j2,k+1}}^{*}\left[\beta_{k+1}\left(s_{j2,k+1}\right) + \gamma_{k+1}^{(z)}\left(s_{j1,k}, s_{j2,k+1}\right)\right] \quad (1c)$$

$$\begin{aligned}\Lambda_{apo,k}^{(z)}(u_k) = &\max_{(s_{j1,k-1}, s_{j2,k}, u_k = z)}^{*}\left[\alpha_{k-1}\left(s_{j1,k-1}\right) + \gamma_k^{(z)}\left(s_{j1,k-1}, s_{j2,k}\right) + \beta_k\left(s_{j2,k}\right)\right] \\ &- \max_{(s_{j1,k-1}, s_{j2,k}, u_k = 00)}^{*}\left[\alpha_{k-1}\left(s_{j1,k-1}\right) + \gamma_k^{(z)}\left(s_{j1,k-1}, s_{j2,k}\right) + \beta_k\left(s_{j2,k}\right)\right]\end{aligned} \quad (1d)$$

$$\begin{cases}\Lambda_{ex,k}^{(z)}(u_k) = \Lambda_{apo,k}^{(z)}(u_k) - \Lambda_{apr,k}^{(z)}(u_k) - \Lambda_{in,k}^{(z)}(u_k) \\ \Lambda_{in,k}^{(00)}(u_k) = 0 \\ \Lambda_{in,k}^{(01)}(u_k) = L_c y_k^{s1} \\ \Lambda_{in,k}^{(10)}(u_k) = L_c y_k^{s2} \\ \Lambda_{in,k}^{(11)}(u_k) = L_c\left(y_k^{s1} + y_k^{s2}\right)\end{cases} \quad (1e)$$

encoded sequence is binary phase shift keying (BPSK) modulated and is transmitted through an additive white Gaussian noise (AWGN) channel with noise variance σ^2, Log-MAP algorithm is described by Eq. 1. Where $x_k^{s1}, x_k^{s2}, x_k^{p1}, x_k^{p2}$ are the transmitted codewords (s and p denote the systematic and the parity bits), $y_k^{s1}, y_k^{s2}, y_k^{p1}, y_k^{p2}$ are the soft received bits, $z \in \{00, 10, 11\}$, $j \in \{0, 1 \ldots 7\}$ is the index of state metrics, $s_{j,k}$ is the jth state at time slot k, $L_c = 2/\sigma^2$. $\gamma_k^{(z)}$ is the branch metrics, α_k is the forward state metrics and β_k is the backward state metrics. $\Lambda_{apr,k}^{(z)}(u_k)$, $\Lambda_{apo,k}^{(z)}(u_k)$ and $\Lambda_{ex,k}^{(z)}(u_k)$ are the a priori Log-Likelihood Ratio (LLR), the α posteriori LLR and the extrinsic information for $u_k = z$, respectively.

Moreover, the two-variable max* operator is defined and approximated as:

$$\begin{aligned}\max^{*}(x_1, x_2) &\triangleq \ln\left[\exp(x_1) + \exp(x_1)\right] \\ &\approx \max\{x_1, 0.25x_1 + 0.75x_2 + 0.5, \\ &\quad 0.75x_1 + 0.25x_2 + 0.5, x_2\}\end{aligned}$$

and has been demonstrated with near optimal decoding performance (Papaharalabos *et al*., 2009). For the max* operation with more than two variables (there are four variables in (1b) and (1c) and eight variables in (1d)), (2) is recursively used, but this recursion requires more circles in hardware realization. To address this, we propose to decompose the n-variables max* operation as follows ($x_1, x_2, \ldots, x_n$ are the variables):

- Selects the predominant two variables from set $\{x_1, x_2, \ldots, x_n\}$:

$$\begin{cases}y_1 = \max\{x_1, x_2, \cdots, x_n\} \\ y_2 = \max\{\cdots, x_i, \cdots\},\ x_i \neq y_1\end{cases}.$$

- Calculates the n-variables max* as below:

$$\begin{aligned}&\max^{*}\{x_1, x_2, \cdots, x_n\} \\ &\approx \max^{*}\{y_1, y_2\} \\ &\approx \max\{y_1, 0.25y_1 + 0.75y_2 + 0.5, \\ &\quad 0.75y_1 + 0.25y_2 + 0.5, y_2\}\end{aligned}$$

PROPOSED DECODING SCHEME

SMC compressed technique: In conventional decoding scheme (He *et al*., 2010), the eight forward state metrics at each time slot k are stored in the Last In First Out (LIFO) SMC. To reduce the SMC size, compressing and estimating of the forward state metrics are investigated in this section, which have five steps given below:

- $\alpha_k\ (s_{j2,\ k})$ are calculated by the forward recursion module
- $\alpha_k\ (s_{j2,\ k})$ are input into a tree of comparators, which outputs an index sequence ($IS_k = [is_{0,\ k},\ is_{1,\ k},\ \ldots,\ is_{7,\ k}]$) of these metrics from the minimum to the maximum. Then, the minimal and the maximal state metrics ($\alpha_{min,k}$ and $\alpha_{max,\ k}$) are obtained
- By subtracting $\alpha_{min,\ k}$ from $\alpha_{max,\ k}$ and divides this difference metric by 7, an increase metric ($\alpha_{inc,\ k}$) is calculated. Then, IS_k and $\alpha_{inc,\ k}$ are stored in the SMC
- In the backward direction, IS_{W-k} and $\alpha_{inc,\ W-k}$ are read out from the LIFO SMC and then are used to estimate $\hat{\alpha}_{W-k}(s_{j2,W-k})$: i) $\alpha_{inc,\ W-k}$ is recursively added to calculate $j2\times\alpha_{inc,\ W-k}$, j2 = [0, 1, …, 7]; ii) with the index included in IS_{W-k}, $j2\times\alpha_{inc,\ W-k}$ is assigned to the $(is_{j2,\ W-k})^{th}$ position of $\hat{\alpha}_{W-k}$ in a rearrange module
- $\hat{\alpha}_{W-k}(s_{j2,W-k})$ are employed to calculate $\Lambda^{(z)}_{apo,W-k+l}(u_{W-k+l})$ by the a posteriori LLR calculator and $\Lambda^{(z)}_{ex,W-k+l}(u_{W-k+l})$ are calculated by the extrinsic information calculator

For instance, by assuming $\alpha_{W-k}\ (s_{j2,\ W-k})$ take the values as shown in the second line of Table 1, we can derive $\alpha_{min,\ W-k}$ = 10.293, $\alpha_{max,\ W-k}$ = 14.205 and $\alpha_{inc,\ W-k}$ = 0.56. Consequently, $is_{j2,\ W-k}$ and $\hat{\alpha}_{W-k}(s_{j2,W-k})$ are listed in Table 1.

Based on the above discussed steps, $\hat{\alpha}_{W-k}(s_{is_{j2},W-k})$ are the linear approximation of $\bar{\alpha}_{W-k}(s_{is_{j2},W-k})$, where:

$$\bar{\alpha}_{W-k}(s_{is_{j2},W-k}) = \alpha_{W-k}(s_{is_{j2},W-k}) - \alpha_{min,W-k}$$

It should be noted that if:

$$\alpha_{W-k}(s_{is_{j2},W-k})$$

are replaced by:

$$\bar{\alpha}_{W-k}(s_{is_{j2},W-k})$$

the decoding performance would not be degraded. However, when $\bar{\alpha}_{W-k}(s_{is_{j2},W-k})$ are further replaced by $\hat{\alpha}_{W-k}(s_{is_{j2},W-k})$ errors are introduced because of the adopted linear approximation. By using the simplified max* operation that introduced in Section 2, simulation shows degradation of the bit error rate is limited (Fig. 3).

Table 1: An example of the proposed approach

J2	0	1	2	3	4	5	6	7
$\alpha_k\ (s_{j2,\ W-k})$	13.26	12.59	10.56	10.29	14.21	10.79	11.24	11.1
is_{j2}	3	2	5	7	6	1	0	4
$\hat{\alpha}_k\ (s_{is_{j2},\ W-k})$	3.35	2.79	0.56	0	3.912	1.12	2.24	1.68

Table 2: Comparison of SMC size (bit)

Decoding scheme	State metric (or index)	Sign bit	Increase metric	Size of SMC
Conventional decoding scheme [13]	8×10×W	0	0	80×W (100%)
Radix-4traceback decoding scheme [9]	6×10×W	4×W	0	64×W (80%)
State metric compressing decoding scheme [11]	8×5×W	0	0	40×W (50%)
The proposed decoding scheme	8×3×W	0	6×W	(24+m) ×W (37.5%)

Proposed decoding scheme: Throughput is a major task in the realization of turbo code decoder. An efficient scheme is to divide the received sequence into a number of independent windows and each window performs the adopted decoding algorithm in parallel (Abbasfar and Yao, 2003). Let W be the width of the window, by the decoding algorithm in (1), with $\gamma_k^{(z)}$ and $\gamma_{W-k+1}^{(z)}$ that are respectively calculated by the branch metrics unit BMU_α and BMU_β, $\alpha_k\ (s_{j2,\ k})$ and $\beta_{W-k+1}\ (s_{j1,\ W-k+1})$ are calculated in the opposite directions and resulting a decoding structure as shown in Fig. 2: (i) in the forward direction, IS_k and $\alpha_{inc,k}$ are recursively calculated and then stored in the LIFO SMC; ii) in the backward direction, $\beta_{W-k+1}\ (s_{j1,\ W-k+1})$ are calculated in the backward recursion module, with $\hat{\alpha}_{W-k}(s_{j2,W-k})$ calculated by the regeneration module and $\gamma^{(z)}_{W-k+l}$ calculated by the BMU_β module, $\Lambda^{(z)}_{apo,W-k+l}$ are calculated by using (1d), so do $\Lambda^{(z)}_{ex,W-k+l}$ by using (1e).

Compared with the conventional decoding scheme, a compressing module is inserted before the LIFO SMC, while a regeneration module is added behind the LIFO SMC. In the proposed decoding approach, since there are eight forward state metrics at each time slot k, index of the state metric can be 3-bit quantized. Furthermore, the bit length of $\alpha_{inc,\ k}$ is set to 6 in our simulation and resulting in the word width of the SMC equals to 8×3+6 bits. Therefore, the SMC size is considerably reduced.

MEMORY EVALUATION AND BER SIMULATION

To evaluate the memory-reduced approach proposed in this study, the radix-4 traceback (Lin *et al*., 2009) and the state metric compression (Martina and Masera, 2011) techniques are used for comparison. The radix-4 traceback technique stores six difference metrics and four sign bits in the SMC, since the difference metrics and the state metrics have the same quantized bit length, word length

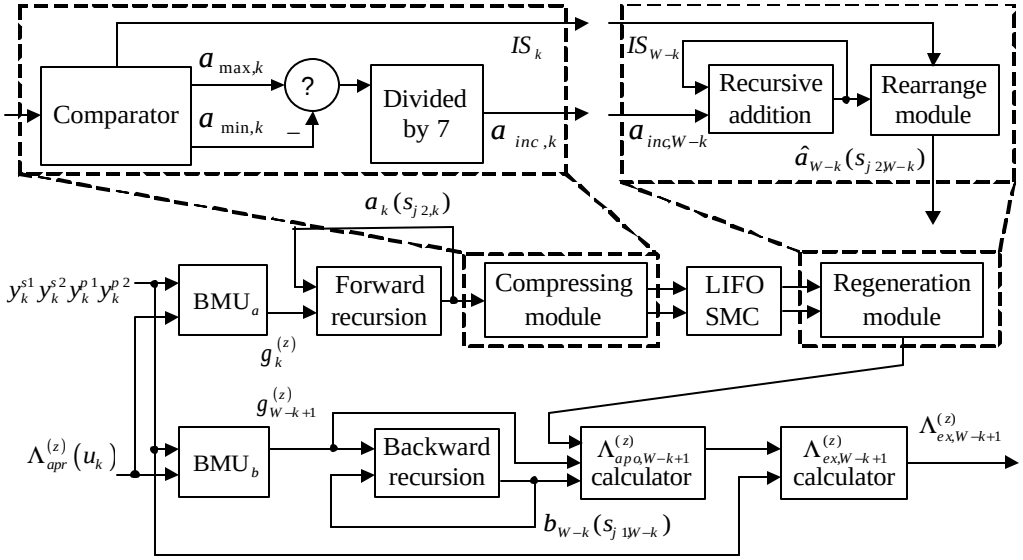

Fig. 2: Structure of the SISO decoding window (k = 1, …, W)

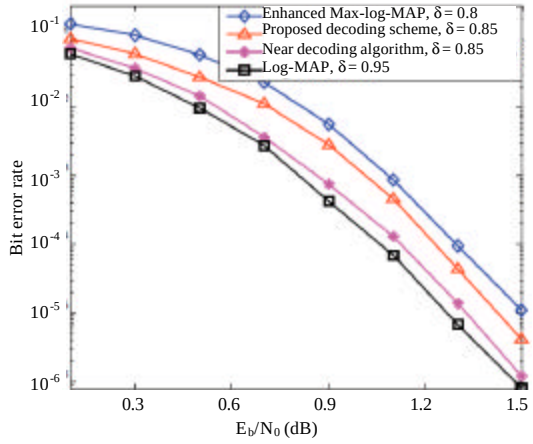

Fig. 3: Comparison of the BER performance

of SMC in this traceback decoding scheme is 6×10+4 bits. Compressing the state metric is another effective technique, in which the Wash-Hadamard Transform (WHT) is applied to compress the bit width of state metrics and word length is thus reduced from 8×10 down to 8×5 bits. For a decoding window with width W, SMC size comparison of the conventional, the radix-4 traceback, the state metric compression and the proposed decoding schemes is summarized in Table 2.

In our investigation, $\alpha_{inc,\ k}$ is 6 bits quantized and Table 2 shows that compared with the conventional decoding scheme, the proposed decoding scheme reduces the SMC size by 62.5%, while the radix-4 traceback and the state metric compressing decoding schemes save the total SMC size by 20% and 50%, respectively.

In Figure 3, the BER performance of the proposed decoding scheme is presented and three well-known decoding algorithms, i.e. the EML-MAP algorithm, the near optimal decoding algorithm in (Papaharalabos *et al.*, 2009) and the Log-MAP algorithm, are also implemented for comparison. Since, better performance can be achieved by scaling the extrinsic information with factor δ (Vogt and Finger, 2000), the scaling technique is adopted to each algorithm. The frame length of information sequence equals to 800 bits and is code rate 1/3 encoded with interleaver parameters in (MTT-S, 2010). By assuming that the received sequence is divided into 20 independent windows with length W = 20 bits and eight iterations are considered, simulation results are presented in Fig. 3.

Seen from Fig. 3, the Log-MAP algorithm gets the best BER performance, about 0.05 dB superior to the near optimal decoding algorithm. Compared to the near optimal decoding approach, the proposed decoding scheme has performance degradation of approximately 0.15 dB, but outperforms the EML-MAP algorithm by about 0.1 dB.

CONCLUSION

This study has proposed an approach to reduce the size of SMC for the realization of DB-CTC decoder. Different from other memory-reduced decoding schemes, the key idea of this approach is to rearrange the forward

state metrics from the minimum to the maximum and then to recalculate these state metrics with linear approximation. By storing the index sequence and the increase metric in the SMC, the total size of the SMC is thus reduced by 62.5%. In addition, combined with the simplified multivariable max* operation, the proposed decoding scheme outperforms the EML-MAP algorithm by 0.1 dB. Considering that the EML-MAP algorithm is widely applied to the hardware implementation, our proposed decoding scheme can be used in the realization of power efficient DB-CTC decoder.

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