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Single-Rail MCML Standard Cells for High-Speed Digital Systems

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Abstract: In this study, standard cells based on single-rail MOS Current Mode Logic (SRMCML) for high-speed applications are developed and introduced into SMIC (Semiconductor Manufacturing International Corporation) 130 nm CMOS libraries which include basic logic gates such as inverter, NAND, NOR. The main design parameters including bias current, output voltage swing and device sizes of transistors in SRMCML cells are optimized to minimize Power Delay Product (PDP). The optimizations and designs for basic standard cells based on SRMCML are carried out. A full adder is verified with the proposed standard cells by using commercial EDA tools. Compared with the conventional static CMOS, the power delay product of the SRMCML AND and OR cells provide a reduction of 50.27 and 63.06% at 3 GHz, respectively. The results indicate the proposed SRMCML standard cells are a good choose in high-speed digital applications.

Key words: MOS current mode logic, standard cell, high-speed application, digital systems

INTRODUCTION

High-speed circuits are frequently required in a wide range of applications such as high-speed processors (Tanabe *et al*., 2001). In MOS Current Mode Logic (MCML) techniques, the output swing is much little than conventional CMOS ones and thus the circuits realized with the MCML techniques can operate at a high speed (Somasekhar and Roy, 1998).

In digital chip designs, widely used methods are cell-based design flow with commercial EDA tools. In order to realize a MCML high-speed chip, MCML standard cells should be constructed. Several construct methods and implementations of standard cells have been reported (Badel *et al*., 2005; Cevrero *et al*., 2011) which include MCML circuit design (Badel *et al*., 2005), physical implementation (Cevrero *et al*., 2011) and characterizing of standard cells (Badel *et al*., 2005). However, all the proposed standard cells are realized with dual-rail MCML (DRMCML) (Hi and Li, 2013; Kim, 2009; Musicer and Rabaey, 2000; Alioto and Palumbo, 2003). The DRMCML circuits increase extra area and the complexity of the layout place and route compared with single-rail MCML (SRMCML) (Hu and Cao, 2012).

In this work, MCML standard cell design methods for high-speed applications are methods for high-speed applications are developed and introduced into SMIC (Semiconductor Manufacturing International Corporation) 130nm CMOS libraries. The proposed MCML standard cells are realized with SRMCML. The SRMCML cells reduce the layout area and simplify the layout place and route and thus it is more suitable for standard cells than DRMCML. These proposed SRMCML standard cells are optimized in term of power delay product (PDP) with the performance analysis and HSPICE simulations.

MCML CIRCUITS

The buffer/inverter based on conventional dual-rail MOS Current Mode Logic (DRMCML) and the biasing circuits are shown in Fig. 1.

The buffer/inverter based on DRMCML is composed of three main parts: the load transistors P1 and P2, the full differential pull-down switch network consisting of the NMOS Pull-down Network (PDN) and its complementary NMOS PDN and the current source transistor (NS). The load transistors are designed to operate at linear region with the help of the control voltage V_{rfp} produced by the bias circuit which also control the output logic swings. The signal V_{rfn} is used to control the demanded bias current I_S which is mirrored from the current source in the bias circuit.

DRMCML circuit is a differential logic one with dual-terminal input and dual-terminal output ports like DCVSL (Alioto and Palumbo, 2003). This structure results in extra area overhead, because the two complementary PDNs must be used. Moreover, the dual-rail structure increases complexity of the layout place and route. A single-rail edition of MCML circuits is shown in Fig. 2 (Li *et al*., 2012). The SRMCML circuits are realized only

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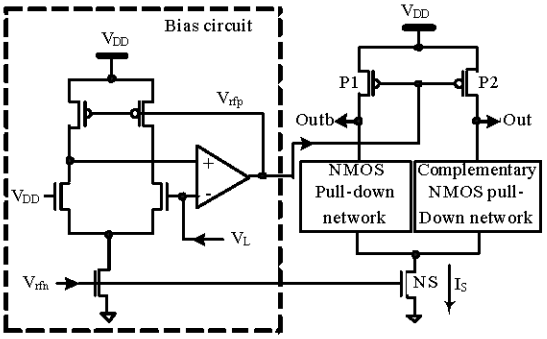


Fig. 1: MCML with dual-rail scheme

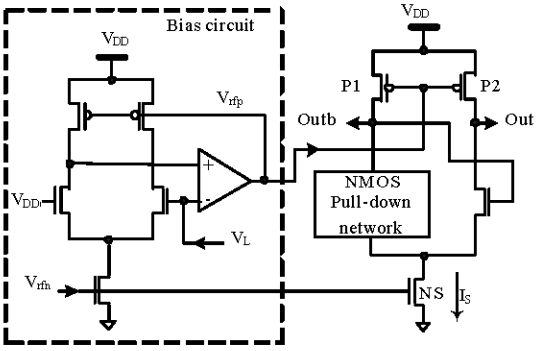


Fig. 2: Single-rail MCML

using a NMOS pull-down network to perform the demanded logic operation. The complementary NMOS PDN used in the DRMCML circuit is replaced with a NMOS transistor and its output is fed back the gate of this NMOS transistor.

The operation of both DRMCML and SRMCML circuits is performed in the current domain. The pull-down network switches the constant current between the two branches. The two PMOS load transistors convert the constant biasing current to output voltage swings. The high and low voltages of the outputs (Out and Outb) are:

$$V_{OH} = V_{DD} \quad (1)$$

$$V_{OL} = V_{DD} - I_S R_D \quad (2)$$

where, V_{DD} is source voltage and I_S is bias current of the MCML circuit and R_D is the linear resistance of the PMOS transistors, respectively. The logic swing of the output voltage can be written as:

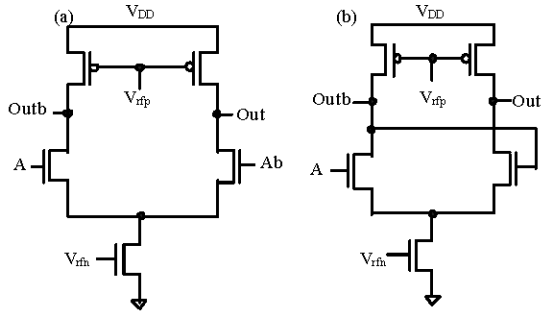


Fig. 3(a-b): Buffer/Inverter based on dual-rail and single MCML schemes (a) Dual-rail scheme and (b) Single-rail scheme

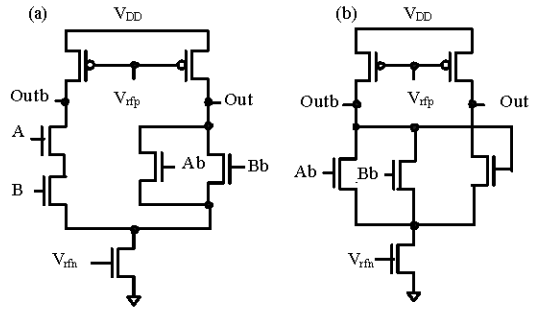


Fig. 4(a-b): AND/NAND based on dual-rail and single MCML schemes (a) Dual-rail scheme and (b) Single-rail scheme

$$\Delta V = V_{OH} - V_{OL} = I_S R_D \quad (3)$$

The proper logic swing ΔV is obtained by setting the negative-terminal voltage of the operational amplifier in the bias circuits as $V_L = V_{DD}-\Delta V$, as shown in Fig. 1 and 2. From (3), for given ΔV and I_S, the linear resistance of the PMOS transistors is determined. The feedback in the bias circuits generates the proper signal V_{rfp} to ensure that the linear resistance R_D meets the Eq. 3.

The transistor-level schematics of basic SRMCML gates, such as buffer/inverter, two-input AND/NAND (AND2/NAND2), two-input OR/NOR (OR2/NOR2), are shown in Fig. 3-5. The structure of the single-rail MCML circuits is simpler than the dual-rail ones, because only a PDN is demanded. Therefore, the single-rail logic circuits reduce area overhead.

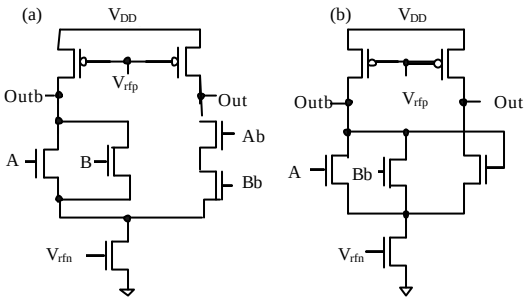


Fig. 5(a-b): AND/NAND based on dual-rail and single MCML schemes (a) Dual-rail scheme and (b) Single-rail scheme

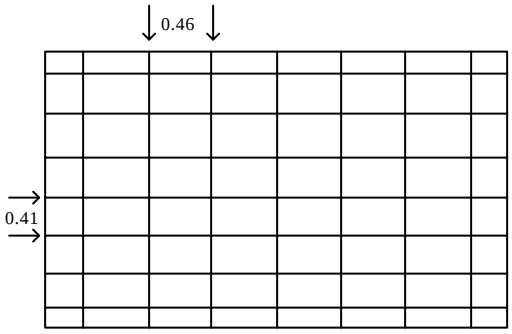


Fig. 6: The layout design template

LAYOUTS AND POST-LAYOUT SIMULATIONS

In the design of standard cell, the layout must be completed for automatic place and route tools (such as Cadence SoC Encounter). For SMIC 130nm standard cells, all cells have been characterized with a fully populated metal2 (0.46 um horizontal pitch) and metal1 (0.41 um vertical pitch) routing grid across the entire cell layout SMIC 130 nm, Thus all the width of the standard cell layout is a multiple of the pitch of metal2 and all the height of the layout is a multiple of the pitch of metal1. The layout design template is shown in Fig. 6.

According to the template of the standard cell, the SRMCML standard cells have been drawn, as shown in Fig. 7. The metal lines are placed horizontally at the top and bottom for the power supply (V_{DD}) and ground (V_{SS}), respectively. The layout heights of all the cells are 3.69um which is the same as 130nm SMIC standard cells.

Table 1 shows the power dissipation comparisons among AND gates based on the SRMCML, the conventional CMOS and the DRMCML at 1 GHz. It is obvious that the power dissipation of conventional CMOS is lower than SRMCML's at low frequency of operation.

The power dissipation comparisons among SRMCML, DRMCML and conventional CMOS circuits are shown in Fig. 8 at different frequency. The power dissipation of the conventional CMOS is positive correlation about f, while the power dissipation of the SRMCML and DRMCML circuits is independent operation frequency. No matter what is shown in the Table 1 or Fig. 8, it can been easily seen that the power consumption of the conventional CMOS logic circuit is much lower than MCML's at the low frequency. When the frequency is greater than a certain value, the power consumption of the conventional CMOS logic circuits are

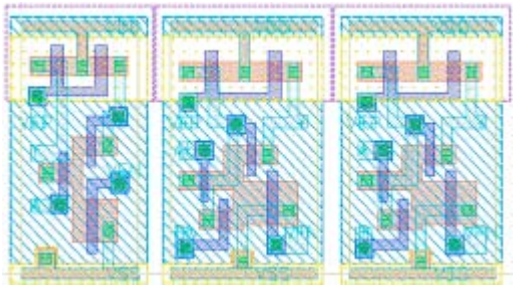


Fig. 7: SRMCML basic standard cells for SMIC 130 nm

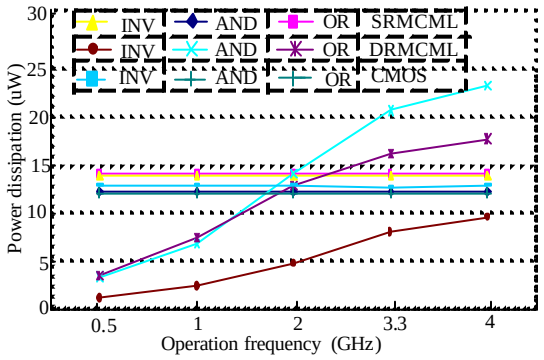
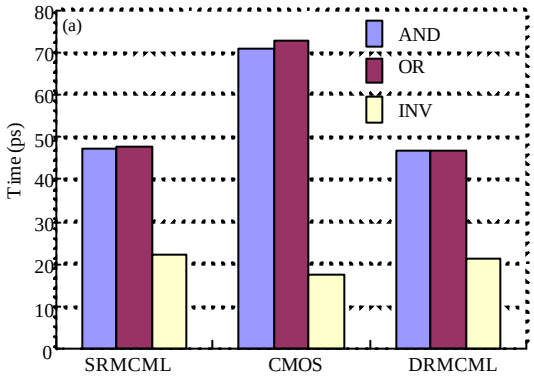


Fig. 8: The power dissipation among the SRMCML, DRMCML and conventional CMOS circuits at different frequency

increasing rapidly and far greater than MCML's. It also shows that the structure of SRMCML and DRMCML circuits is different, but their power consumption is the same. This is because that their power consumption is only related to the power supply V_{DD} and the bias current I_S.

Figure 9 shows the gate delay and power-delay product of conventional CMOS, DRMCML and SRMCML. It can be seen that the conventional CMOS gate delay is the largest in the all circuits. The delay of



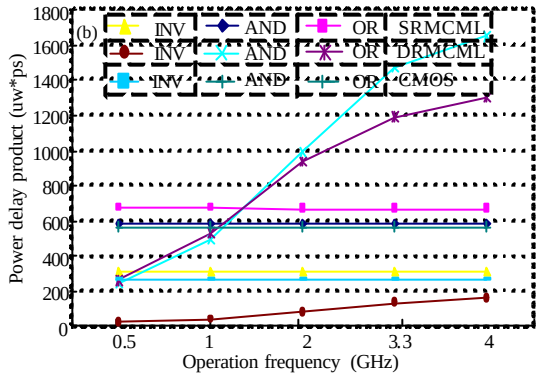


Fig. 9(a-b): The comparison among conventional CMOS, DRMCML and SRMCML, (a) Delay and (b) Power-delay product

DRMCML gate circuits are slightly larger than SRMCML's. In others word, MCML circuit can operate at higher frequency than the CMOS circuit. In terms of delay and power consumption, MCML is undoubtedly the best choice in the high-speed digital circuit.

STANDARD CELL DESIGNS

The layout data-GDS (Graphic Data System) file is extracted by the stream out function of IC5141. The GDS file is used for abstract LEF (library exchange format) file. The Mentor Calibre is used to verify the correctness of the layout electrical rule. The post-layout simulations are carried out by extracting Spice enlists which are used for and also is the key file of generated timing library. The liberty library file is generated by the Liberty NCX and HSPICE which is the physical mapping needed libraries (.lib) and the logic mapping needed library (.db) to be converted by the Library Compiler.

In order to estimate the cells, the 1-bit full adder of the SRMCML is designed and its schematic is shown in Fig. 10. In the process, it is mainly to use synthetically software Design Compiler with Synopsys database library (.db) to carry out the logical mapping. The sum of the 1-bit full adder and the carry are expressed as, respectively

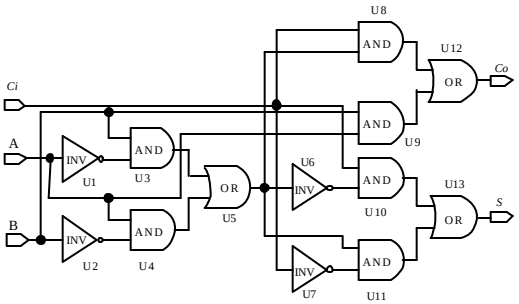


Fig. 10: The schematic of 1-bit full adder

```
****************************************
Report : cell
Design : adder
Version: C-2009.06
Date   : Fri Mar 29 08:40:32 2013
****************************************

Attributes:
    b - black box (unknown)
    h - hierarchical
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library         Area  Attributes
--------------------------------------------------------------------------------
U14                     SRMCML_OR       SRMCML        8.768408
U15                     SRMCML_AND      SRMCML        8.026040
U16                     SRMCML_INV      SRMCML        6.974352
U17                     SRMCML_AND      SRMCML        8.026040
U18                     SRMCML_INV      SRMCML        6.974352
U19                     SRMCML_OR       SRMCML        8.768408
U20                     SRMCML_AND      SRMCML        8.026040
U21                     SRMCML_AND      SRMCML        8.026040
U22                     SRMCML_OR       SRMCML        8.768408
U23                     SRMCML_AND      SRMCML        8.026040
U24                     SRMCML_INV      SRMCML        6.974352
U25                     SRMCML_AND      SRMCML        8.026040
U26                     SRMCML_INV      SRMCML        6.974352
--------------------------------------------------------------------------------
Total 13 cells                                        102.358871
```

Fig. 11: The total area report of the full adder

$$S = \overline{(\bar{a}b + a\bar{b})}c_i + (\bar{a}b + a\bar{b})\bar{c}_i \quad (4)$$

$$Co = ab + (\bar{a}b + a\bar{b})c_i \quad (5)$$

The total area of the adder is shown in Fig. 11 according to the Design Compiler report. As can be seen from the Fig. 11, all cells have been mapped.

Synthesize which needed gate of a 1-bit full adder of the SRMCML is more than the conventional CMOS's, because the standard cell library didn't have all done and it just only have AND, OR, INVERTOR gate. In other words, synthesize results is not the optimal result now.

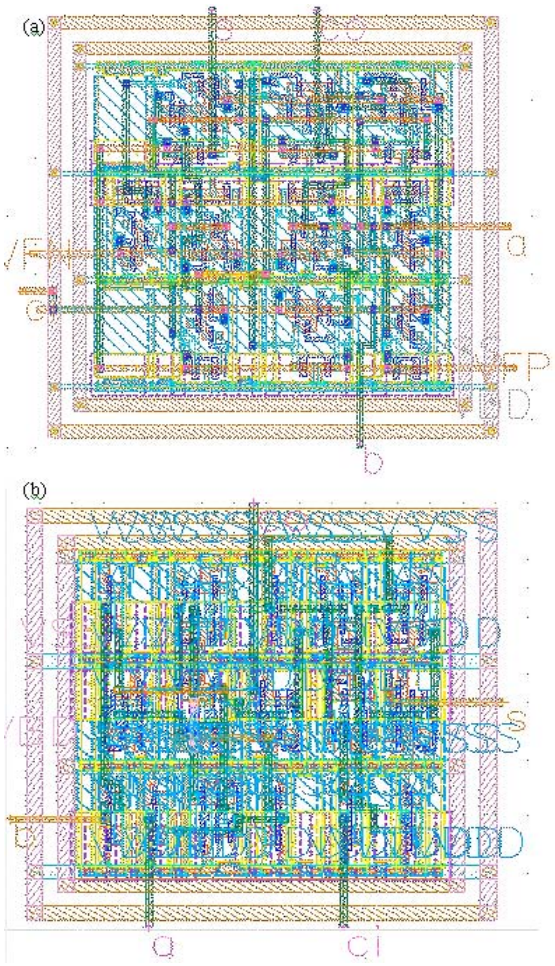


Fig. 12(a-b): 1-bit full adder layout based on, (a) SRMCML and (b) the conventional CMOS

But this does not affect testing for the SRMCML standard cell library. The results show that the method of doing standard cell library is feasible.

Finishing the logical mapping, the next is the physical mapping-automatically place and route to layout. In this process, a timing library (lib) and physical library (.lef) is required in combination with the back-end tool such as SoC Encounter. And then it is carried out on the layout parameter extraction and post-layout simulation. After the verification, this step verifies that the cell library is really done and to be known that can be applied. Fig. 12(a) has shown the layout of SRMCML 1-bit full adder. Fig. 12(b) has shown the layout of conventional CMOS 1-bit full adder.

The layouts of Fig. 12 have extracted their Spice netlists and 1-bit full adder layout of DRMCML is drawn by hand. They are simulated with HSPICE at the SMIC

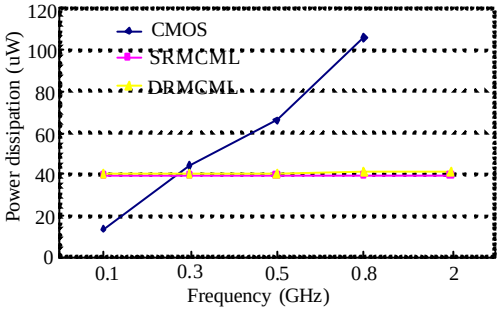


Fig. 13: The power dissipation of 1-bit full adder at different frequency

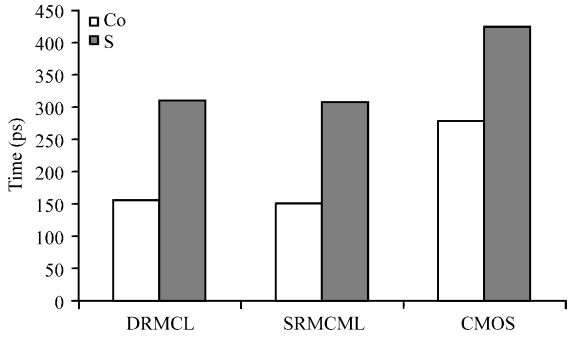


Fig. 14: The delay of 1-bit full adder of DRMCML, SRMCML and the conventional CMOS

130 nm CMOS technology. Fig. 13 shows the power dissipation of the three different type 1-bit full adders at different frequency of operation. From the figure, the power dissipation of the adder conventional CMOS is lower than SRMCML's at lower frequency. Although the curve of the SRMCML's is very flat, then conventional CMOS's is steep. So the SRMCML circuits' advantage is significant at high frequency of operation. Power dissipation of SRMCML circuit and DRMCML's roughly the same.

Fig. 14 shows the delay of S port and Co port of three different types 1-bit full adder. Co port delay is less than the S port's; this is because the path of the Co will shorter than the path of sum. Co port delay of DRMCML, SRMCML and the conventional CMOS is 49.9ps, 50.2ps, 104.8ps, respectively. The latter delay is more than twice of the first two.

CONCLUSION

In this study, the power dissipation and delay of SRMCML circuits have been compared with the

conventional CMOS and DRMCML circuits, respectively. The standard cells based on MCML for high-speed applications are developed and introduced into SMIC 130nm CMOS libraries. The optimizations and designs for basic standard cells based on SRMCML are carried out. A full adder is verified with the proposed standard cells by using commercial EDA tools. The results indicate the proposed SRMCML standard cells are a good choose in high-speed applications. MCML circuit fully reflects his advantage in the high frequency.

ACKNOWLEDGMENT

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