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ITJ

ISSN 1812-5638

INFORMATION TECHNOLOGY JOURNAL

ANSInet
Asian Network for Scientific Information
308 Lasani Town, Sargodha Road, Faisalabad - Pakistan

Information Technology Journal 12 (22): 6513-6518, 2013
ISSN 1812-5638 / DOI: 10.3923/itj.2013.6513.6518

Leakage Reduction Techniques of P-type Adiabatic Circuits Based on Dual-threshold and Gate-length Biasing

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Abstract: The leakage dissipation catches up with the dynamic power consumption gradually and it is becoming an important factor in low-power CMOS circuits. In this work, a p-type complementary pass-transistor adiabatic logic (P-CPAL) using DTCMOS and gate-length biasing techniques is proposed. In order to reduce sub-threshold leakage dissipations, DTCMOS and gate-length biasing techniques are used for the P-CPAL circuits. An ISCAS benchmark circuit using DTCMOS and gate-length biasing techniques is verified. All circuits are simulated with HSPICE using a NCSU 65nm PTM (Predictive Technology Model) process. Results show that both leakage and dynamic dissipations of the P-CPAL circuits with dual-threshold CMOS and gate-length biasing techniques are reduced greatly compared with the normal P-CPAL circuits.

Key words: Nanometer circuits, p-type complementary pass-transistor adiabatic logic, low leakage power, gate-length biasing, dual-threshold CMOS

INTRODUCTION

Scaling down size of MOS transistors has resulted in dramatic increase of leakage currents. The leakage dissipation catches up with the dynamic power consumption gradually and it is becoming an important factor in low-power design for deep sub-micron. Therefore, to decrease leakage power dissipations is becoming more and more important in low-power nanometer circuits. The energy consumption of integrated circuits divided into dynamic energy and static energy. In previous studies of low-power integrated circuits, the dynamic power consumption is the most concern (Rabaey, 1996). In order to reduce dynamic power consumption, many new adiabatic logic circuits have been proposed, such as Complementary Pass-transistor Adiabatic Logic (CPAL) (Hu *et al*., 2005), Clocked Adiabatic Logic (CAL) (Liu and Lau, 1998) and Effective Charge Recovery Logic (ECRL) (Moon and Jeong, 1996). Through recycling the energy stored in circuit nodes, adiabatic logic obtained significant dynamic energy dissipations savings.

The total energy consumption per cycle E_{total} includes three components: switching energy E_{sw} due to charging and discharging for loads, short energy E_{short} due to a direct path from supply voltage to ground and static energy dissipation $E_{leakage}$ that is caused by leakage currents of MOS devices. The short energy losses can usually be ignored. E_{total} is expressed as:

$$E_{total}=E_{sw}+E_{leakage}=áC_LV_{DD}^2+V_{DD}I_{leakage}T \quad (1)$$

where, α is switching activity, C_L is the load capacitance, $I_{leakage}$ is average leakage current of MOS transistors through the V_{DD} and T is operation cycle, respectively (Yu *et al*., 2011), V_{DD} is source voltage.

With the improvement of technology leakage dissipation has potentially become a dominant component of total power dissipations in nano-circuits. There are three main leakage sources in nanometer CMOS processes: Sub-threshold leakage current, gate leakage current and band-to-band tunneling leakage current. Sub-threshold leakage currents are the main sources of static power consumptions in recent nanometer CMOS processes. Several leakage reduction techniques, such as Dual-Threshold CMOS (DTCMOS), Multi-Threshold CMOS (MTCMOS) power-gating technique, stacking transistor techniques, Variable Threshold CMOS (VTCMOS) and Input Vector Control (IVC) have been proposed in recent years to reduce sub-threshold leakage and achieved considerable energy savings (Zhang *et al*., 2011).

Recently, to reduce the static energy dissipation has become the hot research. The PMOS transistor has larger

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area than NMOS in the same performance, but its leakage power is smaller. As we know, a few companies and research institutes begin to study and make use of such new technology. To the best of our knowledge, the PMOS adiabatic logic circuits using DTCMOS and gate-length biasing techniques have not been presented.

In this study, a p-type complementary pass-transistor adiabatic logic (P-CPAL) using DTCMOS and gate-length biasing techniques is proposed. In order to reduce sub-threshold leakage dissipations, DTCMOS and gate-length biasing techniques are used for the P-CPAL circuits. An ISCAS c17 benchmark circuit using DTCMOS and gate-length biasing techniques is verified. All circuits are simulated with HSPICE using a NCSU 65nm PTM (Predictive Technology Model) process. Simulation results show that the P-CPAL c17 based on the DTCMOS and gate-length biasing techniques attains 1.9-19.9% energy savings compared with the basic P-CPAL from 2 to 200 MHz. Results indicate that the p-type adiabatic logic circuits using leakage reduction techniques can have a great improvement in low activity.

REVIEW OF P-CPAL CIRCUITS

The schematic of the basic p-type complementary pass-transistor adiabatic logic (P-CPAL) buffer/inverter is shown in Fig. 1. It is mainly composed of two parts: Logic function circuit that consists of four NMOS transistors (P5-P8) with Complementary Pass-transistor Logic (CPL) function block and the load drive circuit that consists of a pair of transmission gates (N1, P3 and N2, P4). The clamp transistors (P1 and P2) ensure stable operation by preventing from floating of output nodes. The cross-coupled NMOS transistors are used for pre-charge and evaluation. The P-CPAL uses four-phase power clocks to recover the charge delivered by the power clock. Each clock is followed the next clock with a 90° phase lag. For the purpose of discussion here, the power clocks use trapezoidal waveforms.

The operation of p-type of complementary pass-transistor adiabatic logic (P-CPAL) circuits can be divided four processes: Evaluation, hold, recovery and wait phases. For convenience, we assume IN is at high and INb is at low at the beginning of a cycle (Fig. 1) and so that OUT is clamped to clk. During the evaluation phase, as the clock clk goes down, the output OUTb goes high via P1 by the VDD. When clk reaches low, the outputs hold valid logic levels. These values are maintained during the hold phase and used as inputs for evaluation of the next stage. After the hold phase, clk goes up to VDD and outb node returns its energy to clk, so that the delivered charge is recovered. Thus, the power clock clk acts as both a clock and power supply. Wait phase is inserted for clock symmetry. In this phase, valid inputs are prepared in the previous stage. When the previous stage is in the hold phase, the next stage must evaluate logic value in the evaluation phase.

LEAKAGE REDUCTIONS OF P-CPAL CIRCUITS

Power dissipation is a key factor of nano-circuits. In previous studies of low-power integrated circuits the leakage dissipation is often neglected. However, with sizes of MOS transistors scaling down, the leakage dissipation caused by leakage currents catches up with the dynamic power consumption gradually and it is becoming an important factor in low-power design.

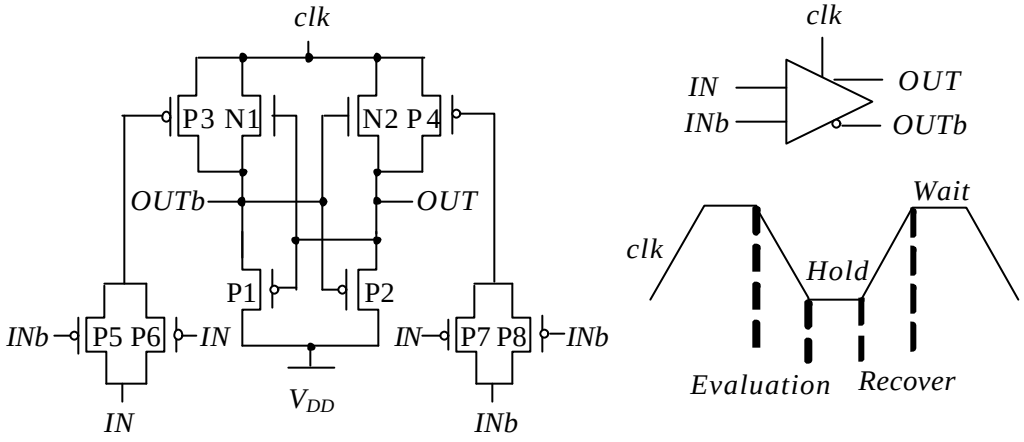

Fig. 1: P-CPAL buffer/inverter and its four-phase power clocks

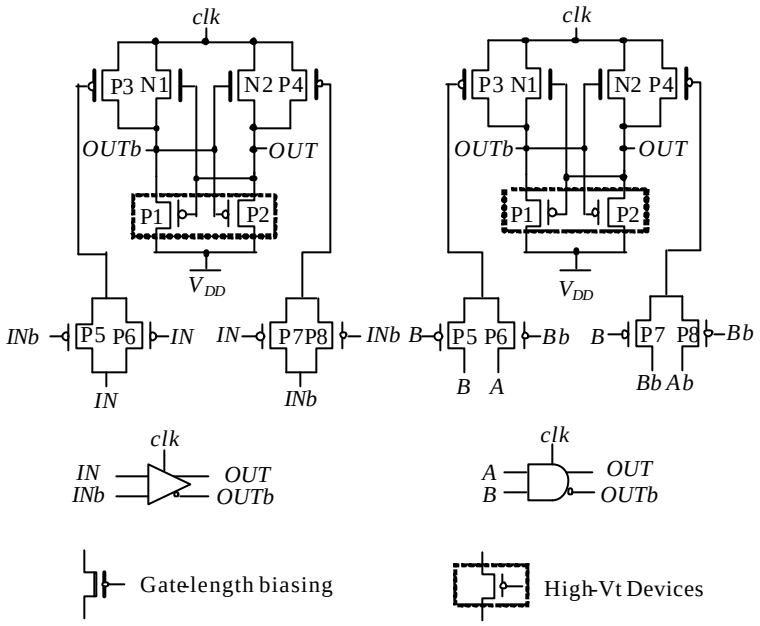

Fig. 2: INV/BUF, OR/NOR gates based on P-CPAL with gate-length

Gate-length biasing: For short channel transistors, with increasing of the gate length, the threshold voltage increases, so that the leakage power decreases exponentially and delay increases linearly. Therefore, it is possible to slightly increase the gate length to take advantage of the exponential leakage reduction while the performance is impaired only linearly. Therefore, increasing gate lengths slightly can decrease leakage dissipation effetely while circuit performance only has little effect. In a 130 nm industrial process, it is reported that an 8 nm increase in gate length yields 30% decrease in leakage with a 5% increase in delay for a minimum size inverter. Based on this principle, the gate-length biasing technique for PAL-2P basic gates can be realized, as shown in Fig. 2.

Dual-threshold CMOS: The sub-threshold leakage current increases exponentially with threshold voltage. For a typical technology with a sub-threshold slope of 100mV/decade, each 100mv reduction in Vt will cause an order of magnitude increase in leakage currents. Therefore, increasing the threshold voltage can reduce leakage dissipations. The dual-threshold CMOS technique uses high-Vt devices to reduce leakage currents while low-Vt devices are used to obtain high performance. Therefore, critical and non-critical regions must be identified.

The DTCMOS for P-CPAL basic gates can be realized, as shown in Fig. 2. In order to reduce sub-threshold leakage currents via the power clock, the PMOS transistors (P1, P2) use high-Vt devices. These DTCMOS gates can be used in non-critical regions of a circuit to reduce sub-threshold leakage dissipations.

Energy consumption comparisons: In order to compare the impact of the gate-length biasing and dual-threshold techniques on the power dissipations, the gate length of transmission gates (N1, P3 and N2, P4) is investigated using 67nm. The four-phase P-CPAL buffer and its simulated waveforms are in Fig. 3.

Table 1 shows the total energy losses of four-phase P-CPAL buffer using the gate-length biasing and dual-threshold techniques at 65 nm CMOS process in 2, 10, 25, 50, 100 and 200 MHz.

From the table we know for low activity, circuits using dual threshold and gate-length techniques are the lowest. Increasing the threshold voltage and the gate length both will increase gate capacitance. For low activity circuits, the leakage savings is more than the increase of dynamic power, those why the total power consumption is reduction. With increasing of activity, the gate capacitance will increase large dynamic power. We know from above that using dual threshold and gate-length techniques together the power dissipation is lower than others for low activity.

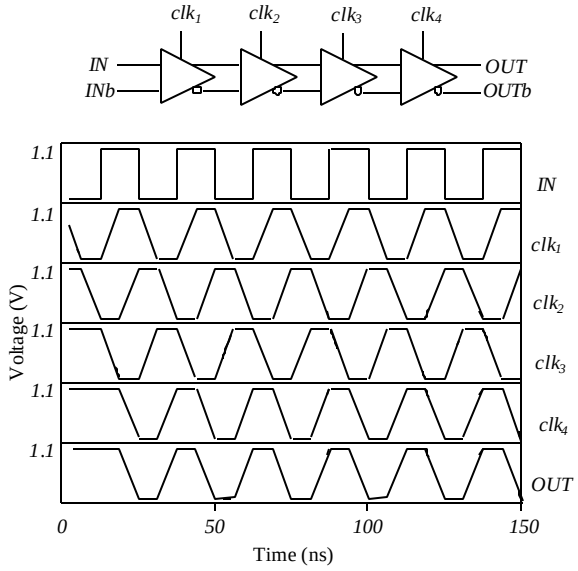

Fig. 3: Four-phase P-CPAL buffer and its simulated waveforms

ENERGY CONSUMPTION COMPARISONS

In this section, the energy dissipations of basic P-CPAL circuits and P-CPAL circuits using DTCMOS and gate-length biasing techniques compared. All circuits are simulated with HSPICE using a NCSU 65nm technology. The peak-peak voltage (VDD) of P-CPAL circuits is taken with 1.1V. Taken as an example, An ISCAS c17 benchmark circuit from ISCAS'85 is verified. The schematic of c17 benchmark circuit is shown in Fig. 4.

For P-CPAL, the schematic of c17 benchmark circuit what should be driven by four-phase power clocks is shown in Fig. 5. Simulated waveforms for the benchmark c17 based on P-CPAL are shown in Fig. 6.

P-CPAL circuits with gate-length biasing and DTCMOS techniques: The leakage currents are highly relates with the threshold voltage of MOS devices. For short channel transistors, the threshold voltage increases with increasing of the gate length. The energy dissipations of the benchmark c17 based on P-CPAL have compared with one using gate-length biasing and is tabulated in Table 2. Simulation results show that the P-CPAL with gate-length biasing attains 3.9-17.2% energy savings compared with the basic one from 10 to 100 MHz. The energy dissipation beyond the basic P-CPAL circuits when the frequency reaching the 200 MHz.

In addition to gate-length biasing the dual-threshold CMOS also can reduce leakage dissipations; the result is shown as Table 3. From the table we known the

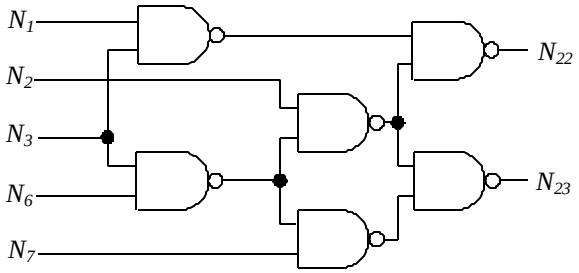

Fig. 4: Benchmark circuit s17 of ISCAS'85

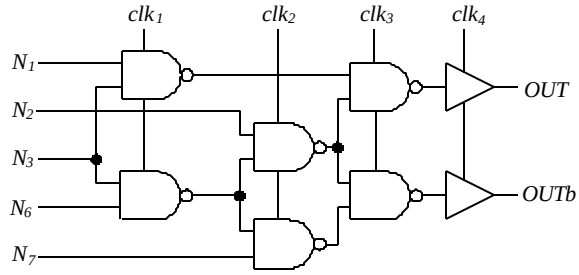

Fig. 5: Benchmark s17 based on PAL-2P circuits

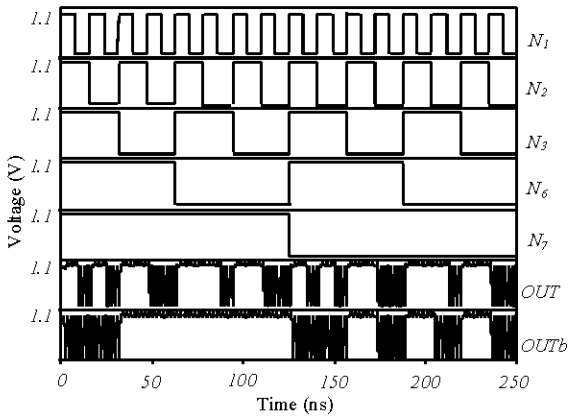

Fig. 6: ÇSimulated waveforms of benchmark c17 based on P-CPAL

dual-threshold CMOS technique attains 1.9-11.8% energy savings compared with the basic one from 10 to 100MHz.

Therefore, both dual-threshold CMOS and gate-length biasing can reduce leakage dissipations. When use these techniques together, the energy savings will be larger than one technique using respectively.

The power consumption comparisons have been carried out for the benchmark c17 based on basic P-CPAL, P-CPAL with one technique and P-CPAL both gate-length

Table 1: Energy consumption comparisons of the four-phase P-CPAL buffer using the gate-length biasing and dual-threshold techniques at 65nm

	Energy consumption per cycle (fJ)			
Frequency (MHz)	Basic P-CPAL	Gate-length biasing	Dual threshold	Gate-length biasing and dual threshold
2	10.94	9.84	10.16	8.91
10	2.93	2.70	2.66	2.42
25	1.64	1.55	1.56	1.53
50	1.38	1.33	1.33	1.27
100	1.21	1.22	1.25	1.25
200	1.42	1.45	1.52	1.53

Table 2: Energy consumption comparison of the C17 based in basic P-CPAL and gate-length biasing

	Energy consumption per cycle (fJ)		
Frequency (MHz)	Basic P-CPAL	Gate-length biasing	Saving rate (%)
10	5.47	4.53	17.2
25	2.97	2.50	15.8
50	2.23	2.03	9.0
100	2.07	1.99	3.9
200	1.64	2.46	--

Table 3: Energy consumption comparison of the C17 based P-CPAL and DUAL-THRESHOLD

	Energy consumption per cycle (fJ)		
Frequency (MHz)	Basic P-CPAL	Dual-hreshold	Saving rate (%)
10	5.47	4.92	10.0
25	2.97	2.62	11.8
50	2.23	2.14	4.0
100	2.07	2.03	1.9
200	1.64	2.34	--

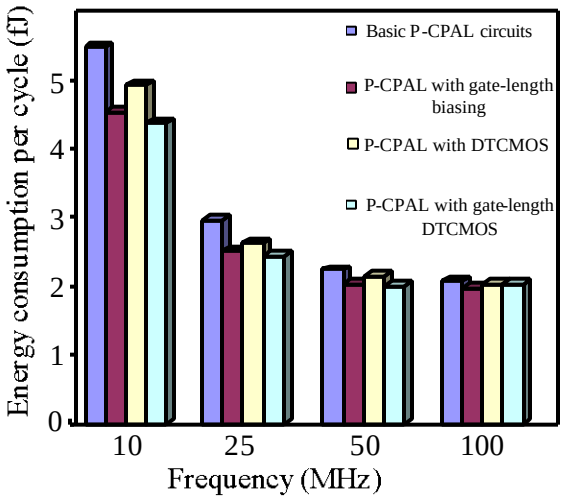

Fig. 7: Energy consumption comparisons of the benchmark c17 based on basic P-CPAL, P-CPAL with gate-length biasing, P-CPAL with DTCMOS technique and P-CPAL with both gate-length biasing and DTCMOS techniques

biasing and DTCMOS techniques, as shown in Fig. 7. For gate-length biasing, the gate length of the transistors is chosen as 67 nm.

Among four implementations, the power consumption of the P-CPAL c17 using dual-threshold CMOS and gate-length biasing techniques is the lowest. Simulation results show that the P-CPAL c17 based on the DTCMOS and gate-length biasing techniques attains 1.9% to 19.9% energy savings compared with the basic P-CPAL, attains 0% to 3.3% energy savings compared with the gate-length biasing P-CPAL and attains 0% to 11.0% energy savings compared with the DTCMOS P-CPAL.

CONCLUSION

This study focuses on dynamic and leakage consumption reductions of p-type complementary pass-transistor adiabatic logic (P-CPAL) circuits by using dual-threshold CMOS and gate-length biasing techniques. In order to reduce sub-threshold leakage dissipations, DTCMOS and gate-length biasing techniques for the P-CPAL circuits have been proposed.

The HSPICE simulation results show the leakage dissipation of the P-CPAL circuits with dual-threshold CMOS and gate-length biasing techniques is the lowest in all circuits. For low activity circuits, the leakage savings is more than the increase of dynamic power. With increasing of activity, the gate capacitance will increase large dynamic power. Results show that both leakage and dynamic dissipations of the P-CPAL circuits with dual-threshold CMOS and gate-length biasing techniques are reduced greatly in low activity.

ACKNOWLEDGMENTS

Project is supported by National Natural Science Foundation of China (No. 61071049), Zhejiang Science and Technology Project of China (No. 2010C31G2070017), Scientific Research Fund of Zhejiang Provincial Education Department (No. Z200908632), Ningbo Natural Science Foundation (No. 2009A610066), Scientific Research Fund of Zhejiang Provincial Education Department (Y201120962).

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