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A Case Study on the Scan Architecture of DFT Technique

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Abstract: As circuit sizes grow ever larger, test data volume and test application time grow unwieldy even in the very efficient scan based designs. Adaptive scan architecture of Design for Test (DFT) technique is used to reduce test application time and test data volume. In our research, we analyze the technique of the scan test architecture. Based on the analysis, the adaptive scan of DFT technique is succeeding applied to a SOC chip. Experimental results show that the test cost of the SOC chip is greatly reduced. Compared with the original program, the fault coverage is reached 97%, the test data volume is decreased 8.79 times, the test time is reduced almost 6 times.

Key words: Adaptive scan, design for test, test data volume, test application time

INTRODUCTION

Currently almost all of the DFT techniques start with a baseline of scan technology. However, the deep submicron Integrated Circuits (IC) design complexity continuously increases which results in excessive test data even for detect stuck-at fault (Wang *et al*., 2004; Mullane *et al*., 2008). In conventional external testing, the huge amount of test data must be stored on the external Automatic Test Equipment (ATE) and be transferred to and from the test circuit through the limited test channels (Gonciari *et al*., 2002; Ziaja and Gala, 2008). This poses a serious problem on manufacturing test. As test data volume increases, it takes more tester buffer space to hold the complete test set and larger test simulation time to verify the correctness of the test data, both leading to higher test cost. Therefore, reduction in tester storages and tester channels for the deep submicron IC design is recognized as extremely important requirements (Hamzaoglu and Patel, 2000). Instead of reduced cost ATE, scan compression technology provided a way to reduce test application time and test data volume on the expensive ATE (which is shown as Fig. 1).

A technique using a single input supporting multiple scan chains had been introduced in study (Nadeau-Dostie *et al*., 2009; Devanathan *et al*., 2007; Kim and Zhang, 2008). However, its application was limited to test multiple independent full scan circuits in parallel method, study (Hsu *et al*., 2001) proposed a scan architecture overcomes this limitation by using two modes of scan operation, parallel scan and serial scan. Study (Arslan and Orailoglu, 2004) configured a scan chains in a circular form enabling the generation of the next pattern from the captured response. While it efficiently overcomes the tester channel bandwidth limitation, it introduced a new problem on the test diagnosis process due to the uncertainty of the test response. Studys (Rao *et al*., 2004) explored the logic dependencies of the internal scan chains to construct a simple logic gates based decompression network so that a great number of scan chains could be driven by a limited number of external scan channels and test cost was reduced.

In this study, the adaptive Scan of DFT technique is discussed which drastically reduces test cost for scan based designs. The adaptive scan structure is shown as Fig. 2. In order to get the maximum fault coverage, the binding portion of the external scan pins and the internal scan chain will automatically adapt to the needs of the Automatic Test Pattern Generation (ATPG) in the scanning unit. Main benefit of the technique is a small amount of on-chip circuitry that reduces both test data storage and test application time (Iyengar and Chandra, 2003; Alampally *et al*., 2008; Chandra *et al*., 2009; Kapur *et al*., 2008). Fully specified test vectors provided by the core vendor are stored in compressed form in the tester memory and transferred to the IC where they are decompressed and applied to the core module. Instead of having transferred entire test vector from the tester to the core module, a smaller amount of compressed data is transferred. Conversely, this reduces the amount of compressed data that must be stored on the tester and the amount of test time required for transferring the data with a given test channels (Lingappan *et al*., 2006).

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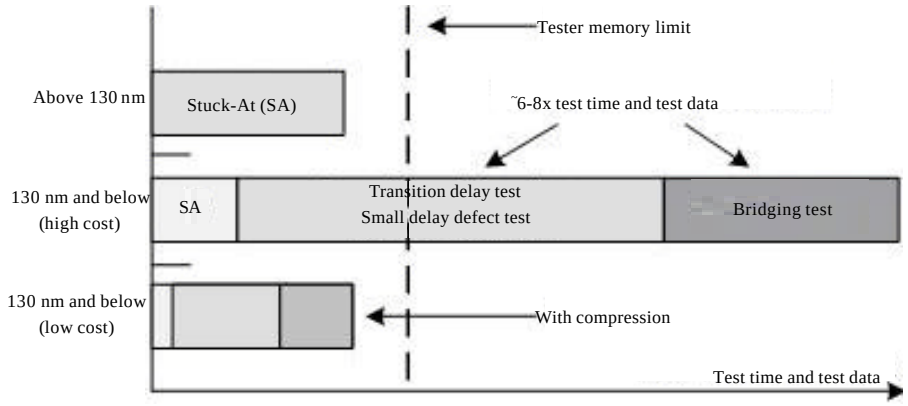

Fig. 1: Test data and test time of different technology

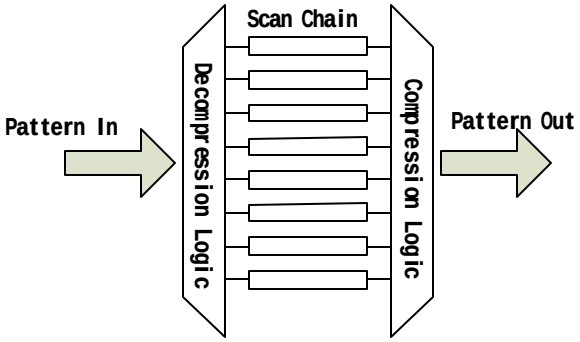

Fig. 2: Adaptive scan of DFT technique

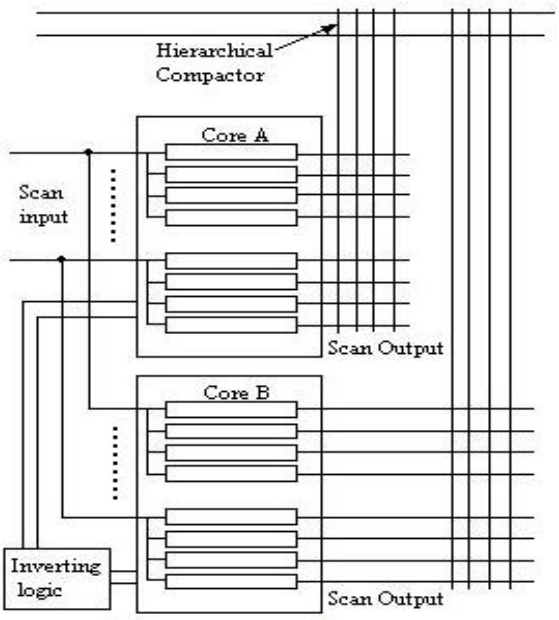

Fig. 3: Hierarchical Compression for Idential Cores

EXPERIMENTS

In complex SoC designs, Hierarchical system architectures exploit the inherent properties of the system architecture compared to the modular approach, it utilizes lesser DFT area and has a faster production time,and it also consumes less power on tester, as blocks can be tested individually or in small groups. Limitation of this approach is that it requires an upfront test plan for the test architecture (Mrugalski *et al*., 2009). The proposed test plan for hierarchical test architecture was based on the interactive model,which is shown as in Fig. 3.

Based on the CCM3201 SOC chip, the adaptive scan structure is designed. Due to the limited input/output pins, the scan ports and the functional ports are designed into the form of reuse (Srinivasan and Farrell, 2010; Chandra *et al*., 2009; Wohl, 2007). In order to meet certain timing condition, some special module are made of Intellectual Property (IP) core and formed some separate scan chains. The scan chains are composed of five kinds of modules, such as a "clock_ctrl" clock module, two "measure_unit" analog modules, a "fd_aif" analog module, a "bch" error correction module and "others_module" module. The adaptive scan of IC design is shown as Fig. 4.

In order to improve the test efficiency of the chip, the hierarchical structure of the hybrid process is designed on the top layer and the flattening structure is designed on the sub module.

Design of top layer: To protect circuit functions and meet the timing case, the optimal scan compression is designed. The DFT design process of the top layer is shown as Fig. 5. First, the module Core Test Language (CTL) file need to be read, the scan compression process is enabled and the scan compressed mode ports are

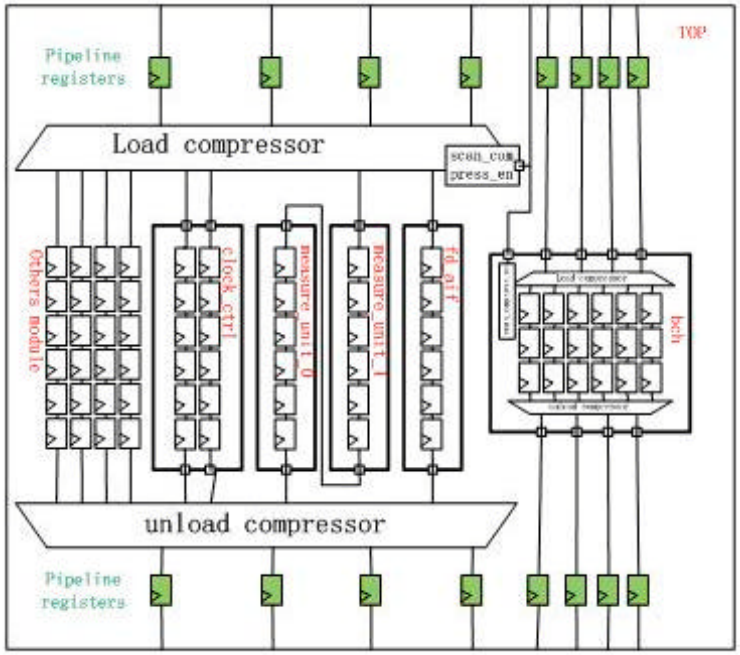

Fig. 4: Adaptive scan design of CCM3201

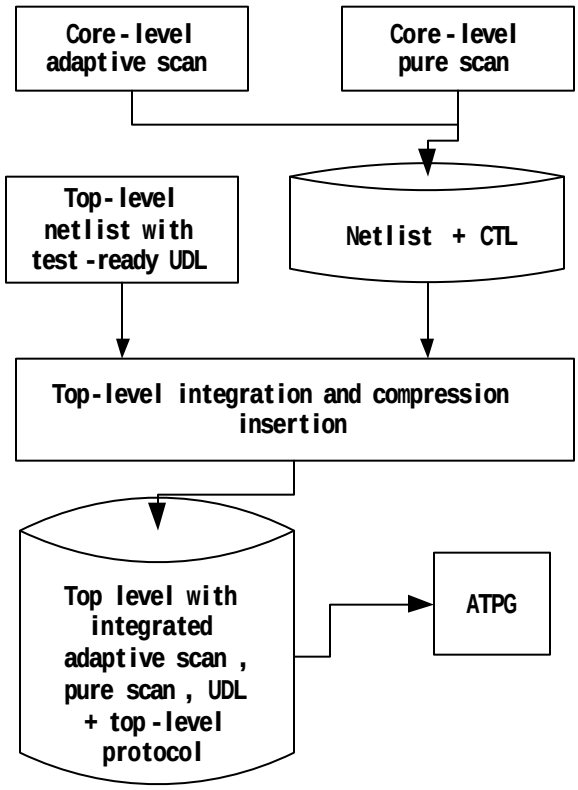

Fig. 5: Top layer design flow

defined. Then, the number of scan chain and scan compression ratio are defined. Special module in the design, such as the "clock_ctrl" module, needs to be limited in order to guarantee an independent chain. Finally, the netlist file, the test protocol and the test vectors for Tetramax ATPG are generated.

The compressor and decompressor logic structure figure are shown as Fig. 6, the scan circuit mode is controlled through "scan_compress_en" signal, the circuit enters scan compress mode when "scan_compress_en" signal is 1 and the circuit enters internal scan mode when the "scan_compress_en" signal is 0.

The following methods can save the power consumption of the test circuit. the control signal "pwr_save_n" is produced by the signal "scan_en" AND the signal "scan_compress_en". when the signal "pwr_save_n" is HIGH, the test circuit enters scan shift state and the compressor is being normal operating state. On the contrary, when the signal "pwr_save_n" is LOW, the test circuit enter the scan capture state and the compressor is turned off.

Design of "bch" module: Using fewer registers, the full-scan structure is designed for sub module except "bch" module. The adaptive scan technique is applied on "bch" module that reduces both test data storage and test

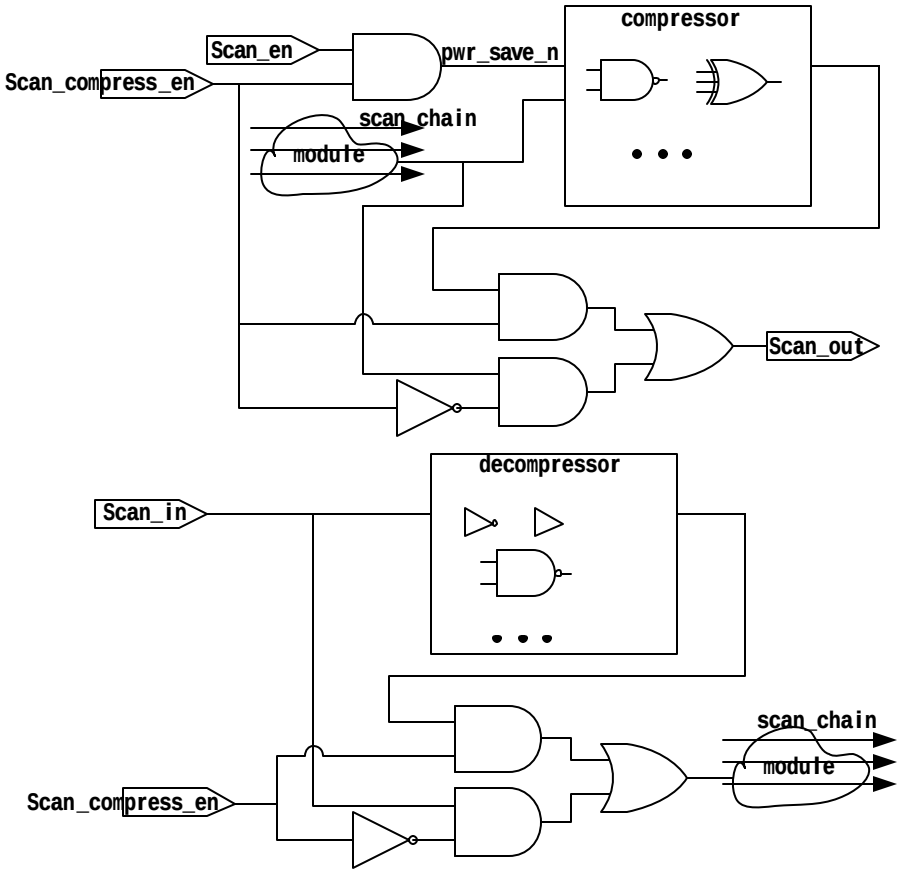

Fig. 6: Compression and decompression logical structure

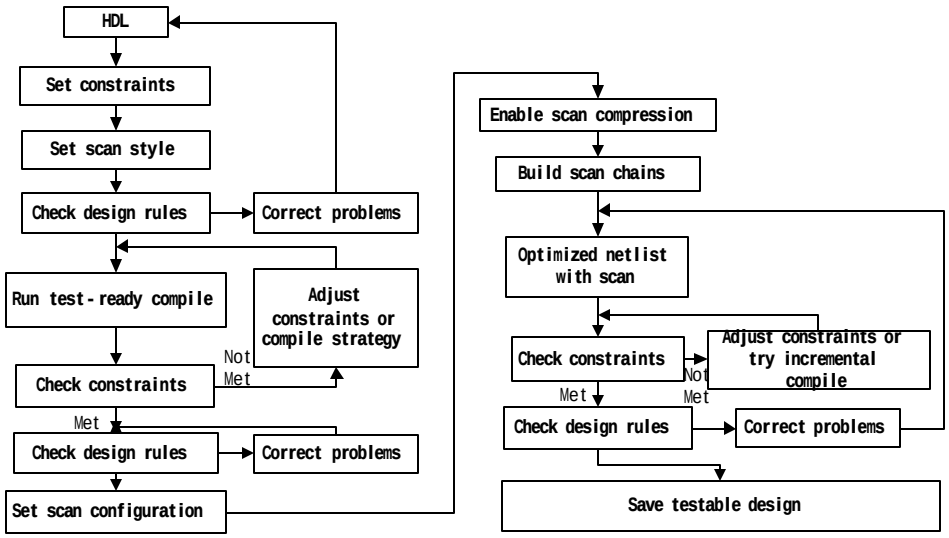

Fig. 7: Adaptive scanning process of "bch" module

application time. The process of adaptive scan design of "bch" error correction module is shown as Fig. 7.

Before compressed, the scan chain of "bch" error correction module is 5, each chain has 1378 registers and

2369 test vectors. After compressed, the test time is saving about 9 times. The effect relationship between compressed level and fault coverage is shown in Table 1.

RESULTS

Results of the chip simulation: The Tetramax fault test report is shown in Table 2. The test data volume of the adaptive scan mode design is 585760 and the test data volume of the full scan mode is 5149456. The test data volume of the full scan mode is about 8.79 times of the former.

The test vector simulation is obtained by using Ncverilog EDA tools. The simulation results is shown in Fig. 8, the adaptive scan simulation time is 18 h 30 min 8 sec and the full scan simulation time is 110 h 20 min 59 sec, approximately 6 times of the former.

Table 1: Relationship between compression ratio and fault coverage

Compression ratio	2	3	4	5	20
Number of Scan Chain (compressed)	12	18	24	30	120
Registers of each chain	573	383	288	230	58
Fault Coverage	99.60%	99.60%	99.40%	99.40%	98.60%
Number of Pattern	2525	1757	1539	1532	801

The report of the chip area and power is shown in Table 3. As we can see, the area of the adaptive scan structure is only increase 0.11% than that of the full scan structure and the power consumption of the chip is almost equal.

Integrated circuit verification: The adaptive scan test technique has been applied to a very large scale integration circuit (VLSI) (CCM3201, C*Core Technology Co., Ltd.) design. With a great reduction in the chip

Table 2: Tetramax simulation report

	Full-Scan	Adaptive-Scan	Unit
Area	5979301	5986129	μm^2
Dynamic power	25.2776	25.2471	mW
Leakage power	383.8512	384.9433	μW

Table 3: Area and power simulation report

	Full-Scan	Adaptive-Scan
DT	1980871	1983219
PT	1959	2253
UD	9829	9834
AU	49117	46193
ND	1446	1723
Total faults	2043222	2043222
Fault coverage	97.00%	97.12%
Patterns	2606	2092

```
ncverilog: 08.20-s024: (c) Copyright 1995-2010 Cadence Design Systems, Inc.
TOOL: ncverilog  08.20-s024: Started on Oct 09, 2012 at 18:23:46 CST

ncsim> run
//           50.00 ns : Begin patterns, first pattern = 0
//           50.00 ns : ...begin scan load for pattern 0
//        35550.00 ns : ...begin scan load for pattern 5
//        71050.00 ns : ...begin scan load for pattern 10
//       106550.00 ns : ...begin scan load for pattern 15
//       142050.00 ns : ...begin scan load for pattern 20
//       177550.00 ns : ...begin scan load for pattern 25
//       213050.00 ns : ...begin scan load for pattern 30
                .         .        .        .        .
                .         .        .        .        .
                .         .        .        .        .
//     14306775.00 ns : ...begin scan load for pattern 2060
//     14342400.00 ns : ...begin scan load for pattern 2065
//     14378025.00 ns : ...begin scan load for pattern 2070
//     14413650.00 ns : ...begin scan load for pattern 2075
//     14449275.00 ns : ...begin scan load for pattern 2080
//     14484900.00 ns : ...begin scan load for pattern 2085
//     14527600.00 ns : ...begin scan load for pattern 2090
//     14556050.00 ns : Simulation of 2092 patterns completed with 0 errors

Memory Usage - 17.0M program + 353.8M data = 370.8M total
CPU Usage - 64.1s system + 66458.7s user = 66522.8s total (100.0% cpu)
Simulation complete via $finish(2) at time 14556050 NS + 0
../pattern/sa_chip_scan.v:149026       if (verbose >=2) $finish(2);
ncsim> exit
TOOL: ncverilog 08.20-s024: Exiting on Oct 10, 2012 at 12:53:54 CST (total: 18:30:08)
```

Fig. 8: Adaptive scanning simulation results

Fig. 9: Chip scan technology test board

simulation time, test coverage has been improved which greatly reduces the cost of the chip testing. The chip has been manufactured by TSMC 90 nanometer processing technology and now it is being done FPGA verification, the preliminary test results show that the desired effect is achieved. The chip scan technology test board is shown in Fig. 9.

CONCLUSION

The DFT technique of logic circuit on CCM3201 SOC chip is studied. The adaptive scan technique is succeeded in solving practical problem. Compared with the original program, the fault coverage is reached 97%, the test data volume is decreased 8.79 times, the test time is reduced 6 times and the chip area and power consumption is only a small increase. The test cost of the SOC chip is greatly reduced.

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