http://ansinet.com/itj

ITJ

ISSN 1812-5638

INFORMATION TECHNOLOGY JOURNAL

ANSInet
Asian Network for Scientific Information
308 Lasani Town, Sargodha Road, Faisalabad - Pakistan

Information Technology Journal 12 (23): 7331-7335, 2013
ISSN 1812-5638 / DOI: 10.3923/itj.2013.7331.7335

Reliability Influences of Substrate Pick-up and Well Engineering of LV Nmosts in Communication Modules

Shen-Li Chen and Min-Hua Lee
Department of Electronic Engineering, National United University, MiaoLi City 36003, Taiwan

Abstract: Usually an MOST of I/O cells in integrated circuits will be in the form of multi-finger type. However, the non-uniform turned-on phenomenon in an MOST is deeply affecting the ESD reliability robustness. Here, the impacts of substrate pick-up stripe variation and a pWell structure adding are investigated in this stduy. ESD performance of these nMOSTs fabricated by a 0.35-μm CMOS process is evaluated in this work. Nevertheless it is desirous to improve the ESD capability of ESD elements. After a systematic analysis it is found that no matter what kind of channel length of nMOSTs, the P^+ pick-up structure of source side and p-well structure in the 0.35-μm LV process are poor contributors to I_{t2} robustness of elements, i.e., the substrate pick-up/ p-well structures will obviously lower the I_{t2} level. Therefore, the source ends should avoid adding any P^+ pick-up stripe and any p-well structure in the 0.35-μm process for communication systems.

Key words: Electrostatic discharge (ESD), latch-up (LU) effect, holding voltage (V_h), pick-up, metal-oxide-semiconductor transistor (MOST), secondary breakdown current (I_{t2}), trigger voltage (V_{t1}), transmission-line-pulse (TLP)

INTRODUCTION

In recent years with advances and scaling the information transmission system, the small volume of electronic products brings convenience but also cause instability on the reliability. For all ICs in handhold electronic products, LCD screen, ipad and other products are required to pass ESD/EMI and LU test specifications (Huang and Ker, 2013), therefore, the electrostatic discharge (ESD) protection has become very important. All in all, ESD affects the reliability of ICs appeared to be increasingly serious and may result in a low yield of electronic products which results in some huge losses. According to the statistic analysis, more than 50% failures in silicon semiconductor integrated circuit are due to ESD/EOS damages (Amerasekera and Duvvury, 2003). In the multi-finger structure of MOST ESD devices as shown in Fig. 1, a non-uniform turned-on phenomenon is an important issue. However, due to a fact that the nMOST has a significant snapback characteristic, from Fig. 2, the distinguished difference of P-type parasitic base resistance (R_B) on each finger in the layout which will result in an nMOST with a multi-finger type can't uniform turn on to discharge the ESD current, thus caused a low ESD level, even if the MOSFET has a large device dimension.

In order to effectively solve the non-uniform turned-on problem, a considerable number of literatures (Lee *et al*., 2009; Ker *et al.,* 2010; Zhou *et al*., 2012;

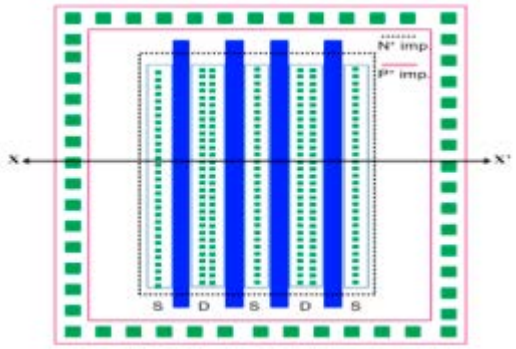

Fig. 1: Layout top view of a traditional multi-finger-type nMOST

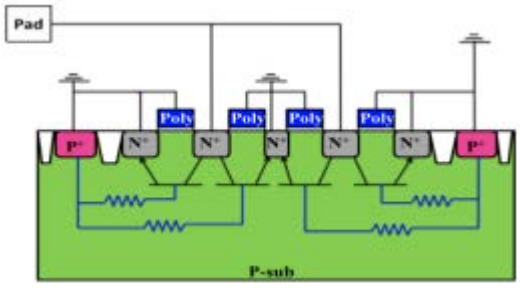

Fig. 2: Cross-section view of a traditional multi-finger-type nMOST

Corresponding Author: Shen-Li Chen, Department of Electronic Engineering, National United University, MiaoLi City 36003, Taiwan

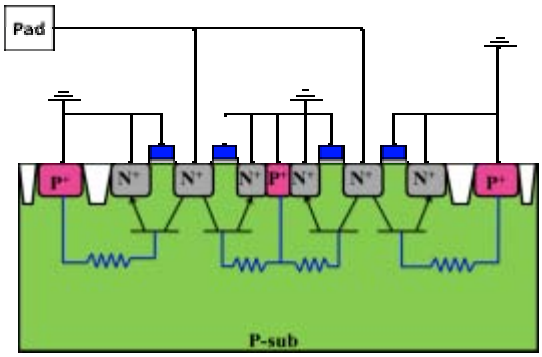

Fig. 3: Cross-section view of a GGnMOS with adding one substrate p^+ stripe in the source side

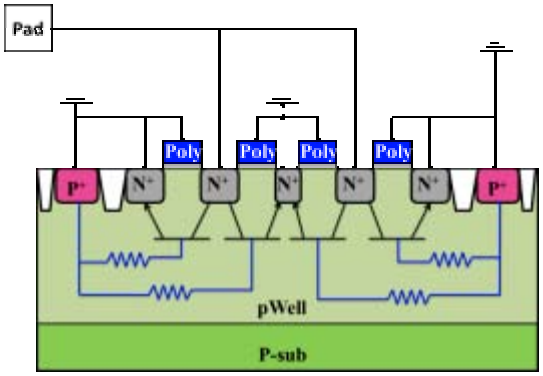

Fig. 4: Cross-section view of a GGnMOS with adding a pWell structure

Chen and Lee, 2013) to investigate the substrate pick-up process to solve the problem. And, in the 0.35-μm low voltage (LV) 3.3-V/5-V design rules of T-Fab (2007), they described that the I/O nMOST should be evenly added the P^+ pick-up stripe in a large area nMOST device, for enhancing ESD ability to overcome the non-uniform turned-on phenomenon. However, the physical mechanism really is that? Therefore, this stduy will aim at: (1) The substrate P^+ pick-up stripe inserted in the source side shown in Fig. 3, (2) Adding a pWell structure above the P-substrate shown in Fig. 4. Then, a TLP measurement system will be used to investigate the influence of these structures on the ESD capability.

The entire test DUTs were fabricated by a 0.35-μm LV 3.3-V process. The multi-finger structure of a gate-grounded nMOST (GGnMOS) used in this work, the channel length (L) are set to be 0.5 and 0.8-μm, channel width of unit finger (W_f) is set to be 50-μm. And, the total channel width (W_{tot}) is kept to be 400-μm (total finger number M= 8). Then, the following description will aim at non-uniform turned-on studies of these two portions and explore the variation of trigger voltage (V_{t1}), holding voltage (V_h) and secondary breakdown current (I_{t2}) between these different structures.

LAYOUT DESIGN OF DUTS

Non-uniform Turned-on Issue in an nMOST: In a general nMOST structure, a guard ring is one of the structures to reduce latch-up sensitivities. Unfortunately, owing to this surrounding structure, the parasitic resistance R_B of the middle finger of a transistor becomes larger. Thus it is causing it earlier and easier triggered on which is susceptible to ESD damage.

In order to effectively solve the non-uniform turned-on problem, some literatures were suggesting by inserting the substrate P^+ pick-up process to solve this problem. Substrate P^+ pick-up process will provide an average substrate parasitic resistance (R_B). It allows to effectively achieve the goal of uniformly conducting in each finger as an ESD noise occurred, avoiding only few fingers turned on it thereby increases its ESD immunity level and also can increase its latch-up immunity.

Type-1: P^+ Pick-up Stripe Inserted in the Source side: In this stduy, some substrate P^+ pick-up stripes from the middle finger area begin to add the P^+ pick-up structure in the source region and uniformly increase the P^+ pick-up stripes gradually from the center to outer. Sequentially, as M= 8 in an nMOST, the number of P^+ pick-up strap is one stripe, three stripes and five stripes, respectively. It is used to observe whether can increase the uniform turned-on ability, so that the whole chip of an MOST can achieve a more efficient use of the area. Here, an nMOST without adding any substrate P^+ pick-up stripe called the standard reference group. And, the influence of these four kinds of DUTs on ESD immunity level with different channel lengths (L), from the original L = 0.5-μm increasing to L = 0.8-μm, are also investigated.

Type-2: Adding a pWell structure: In Fig. 4, a pWell structure will be added into a traditional GGnMOS above the P-type substrate. Due to the concentration of a pWell is heavier than a P-type substrate. Then, by adding this structure is equivalent to increase the concentration of substrate. Therefore, the parasitic resistance (R_{sub}) will be become smaller as compared with a traditional GGnMOS. Then, what's happened in this situation as during the P^+ pick-up adding in the source side?

Similarly, as M = 8 in an nMOST, the number of P^+ pick-up strap is one stripe, three stripes and five stripes, respectively. And, the influence of these four kinds of

\DUTs with different channel lengths (L), from the original L = 0.5-µm increasing to L= 0.8-µm, are also investigated on ESD /LU parameters.

TESTING EQUIPMENT SYSTEM

A Transmission-Line-Pulse (TLP) system for experimental testing is controlled by the LabVIEW software which managed the electronic instrument of subsystem such as the ESD pulse generator, the high-frequency digital oscilloscope and the digital power electric meter instruments, in order to achieve the automatic measurement. This machine can provide a continuous step-high square wave to a DUT and shortly raise time of the continuous square wave can also simulate transient noise of an ESD.

TESTING RESULTS AND DISCUSSION

Channel length (L)= 0.5-µm: Type-1 and type-2 samples as for L= 0.5-im had been zapped; the TLP data can be obtained and shown in Fig 5~ 6 and Table 1. Regardless of the base resistance, when the stripe number of P^+ pick-up increased, the holding voltage V_h will begin to increase, however, the stripe number of P^+ pick-up is not remarkable to ESD capability. Although the P^+ pick-up averaged each parasitic resistor R_B of the MOST fingers, the body effect would be suppressed by these structures. So that, the V_{t1} value will be increased with the strip number, the ESD element will becomes not easy to trigger conduction. And, the holding voltage (V_h) will also increase; the P^+ pick-up can effectively enhance the latch-up immunity.

When GGnMOS devices adding a pWell structure makes the base resistor R_B value smaller, the trigger voltage V_{t1} increased significantly which makes devices become difficultly to trigger conduction. Thus, reducing the base resistance value does not effectively enhance the ESD ability. In addition, the holding voltage (V_h) of a type-2 DUT is larger than that of none adding pWell device, therefore, by adding a pWell can effectively enhanced the latch-up immunity.

Table 1: Snapback key parameters of nMOST DUTs with substrate P^+ pick-up and L= 0.5-µm (σ were sampled by 5 DUTs)

nMOS (L = 0.5um)	V_{t1}(V)	V_h(V)	L_{t2}(A) Mean±σ
wopWell			
No pickup (Ref.DUT)	7.009	5.435	5.185±267
Pickup*1	7.857	5.6	5.009±0.42
Pickup*3	8.898	6.198	5.202±0.285
Pickup*5	9.203	6.516	5.140±0.179
wopWell			
No pickup (Ref.DUT)	7.846	5.528	5.07±0.284
Pickup*1	8.063	5.666	5.011±0.195
Pickup*3	9.041	6.235	5.24±0.127
Pickup*5	9.207	6.473	5.194±0.259

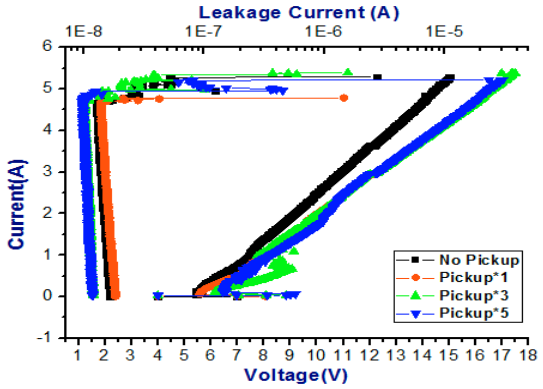

Fig. 5: Snapback I-V curves and leakage currents of GGnMOS DUTs with substrate P^+ pick-up stripes (L= 0.5-ìm and none with a pWell structure)

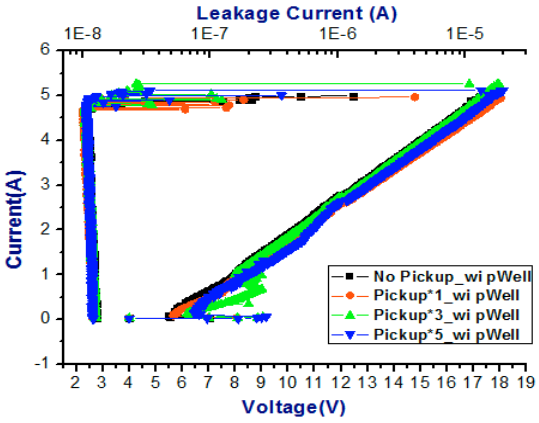

Fig. 6: Snapback I-V curves and leakage currents of GGnMOS DUTs with substrate P^+ pick-up stripes (L= 0.5-ìm and adding a pWell structure)

Channel length (L)= 0.8-µm: As for the test nMOSTs were fabricated with the L = 0.8-µm, the TLP data of these DUTs can be obtained and shown in Fig 7~ 8 and Table 2. Regardless of the base resistance, when the stripe number of P^+ pick-up increased, the I_{t2} value will begin to decrease. But the trigger voltage (V_{t1}) and holding voltage (V_h) will gradually become larger same as the L= 0.5-µm DUTs. These behaviors were similar to the previous 0.5-um DUTs. But one thing was extremely effective improved the ESD immunity especially for the referenced DUT as compared with the corresponding L= 0.5-µm DUTs.

Figure 9~ 10 show the V_{t1}, V_h and I_{t2} characteristics as the pick-up varied among these nMOSTs. There is not evident for the ESD robustness improvement with adding

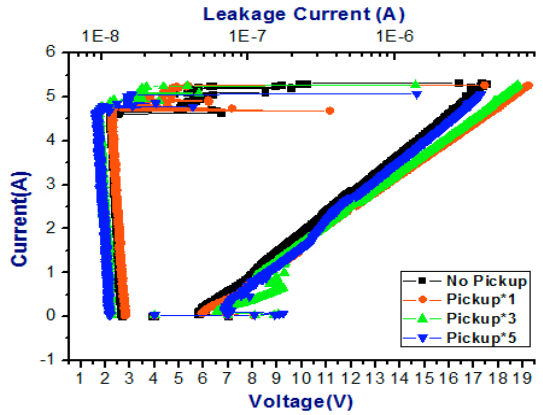

Fig. 7: Snapback I-V curves and leakage currents of a GGnMOS with P^+ pick-up stripes (L= 0.8-µm and none with a pWell structure)

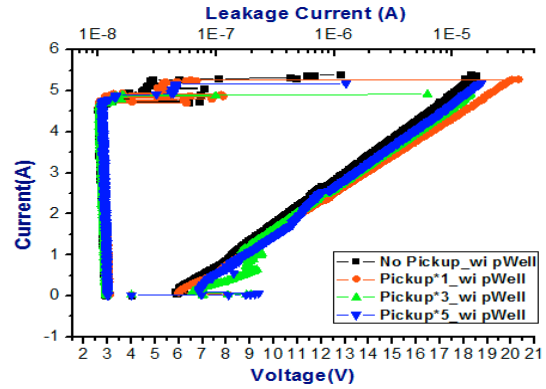

Fig. 8: Snapback I-V curves and leakage currents of a GGnMOS with P^+ pick-up stripes (L= 0.8-µm and with adding a pWell structure)

Table 2: Snapback key parameters of nMOST DUTs with substrate P^+ pick-up and L= 0.8µm (σ were sampled by 5 DUTs)

nMOS (L = 0.5um)	V_{t1}(V)	V_h(V)	L_{t2}(A)Mean±σ
wi pWell			
No Pickup (Ref. DUT)	7.238	5.793	5.321±0.056
Pickup*1	9.219	5.971	5.187±0.265
Pickup*3	0.956	6.6	5.17±0.283
Pickup*5	9.287	6.848	5.11±0.201
wi pWell			
No Pickup (Ref. DUT)	6.97	5.844	5.259±0.145
Pickup*1	8.068	5.985	5.218±0.255
Pickup*3	9.039	6.575	4.915±0.264
Pickup*5	9.265	6.837	5.031±0.2

any P^+ pick-up stripe among the DUTs of channel length L = 0.5-µm and 0.8-µm. The I_{t2} value increased lightly somewhere but it will lower the accuracy due to with a strong standard deviation and variation range. The trigger voltage (V_{t1}) increased obviously resulting in the

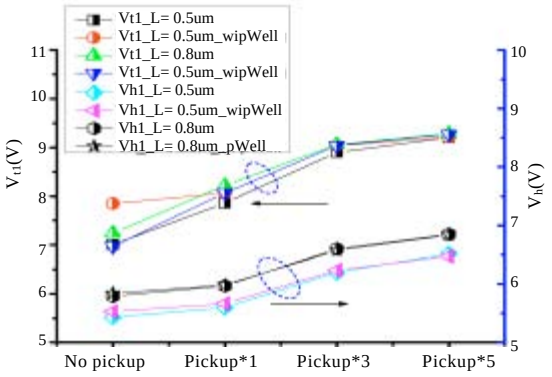

Fig. 9: V_{t1} and V_h diagrams as the pick-up stripes varied in nMOST DUTs

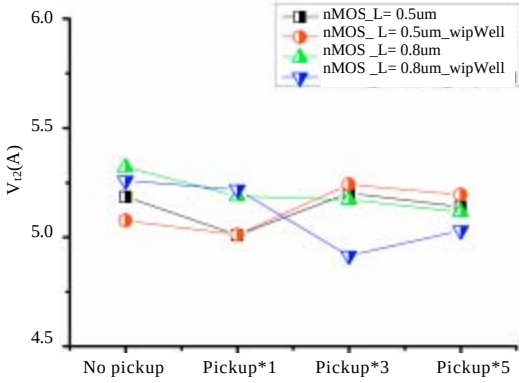

Fig. 10: I_{t2} diagram as the pick-up stripes varied in nMOST DUTs

Table 3: Comparisons of snapback key parameters for the full adding of P^+ pick-up stripes with the corresponding Ref. DUT (where reference DUTs is none with any P^+ stripe)

		About V_{t1}	About V_h	About I_{t2}
0.5µm	wo pWell	31.3% ↑	20% ↑	0.9% ↓
	wi pWell	17.3% ↑	17% ↑	2.3% ↑
0.8µm	wo pWell	28.3% ↑	18.2% ↑	3.8% ↓
	wi pWell	32.9% ↑	17% ↑	4.3% ↓

hardness of increasing ESD robustness. It's worth mentioning that the V_h increased obviously with adding P^+ pick-up stripes. From the TLP testing results of this work, the ESD reliability benefits of the 0.35µm nMOSTs as for the P^+ bulk pick-up stripes even adding compared with none adding (Ref. DUT) can be summarized as in Table 3.

CONCLUSION

Non-uniform turned-on phenomena in nMOSTs are seriously impacted the ESD reliability capability. Two

groups of GgnMOS DUTs are investigated in this work: 1) the channel length L issue: 0.5 and 0.8-μm; 2) different substrate concentrations, one is the normal p-type substrate; the other is the substrate with adding a pWell structure, so that it will have a higher substrate concentration. The benefit of I_{t2} values with a full pick-up stripes in nMOST DUTs is not evident due to body-effect suppression happened. Therefore it can be concluded that the influence of the I_{t2} values with even pick-up stripes in nMOSTs is not evident. The benefit range of I_{t2} of Pickup×5 compared with the WoPick-up (Ref. DUT) increased about -4.3 +2.3%. And, the average shifting range of V_h increased about 17~20% related to the WoPickup (Ref. DUT). Therefore, an nMOST device in this 0.35μm LV process with a pick-up structure is only one advantage that could increase latch-up immunity effectively in the reliability considerations.

ACKNOWLEDGMENT

In this work, authors would like to thank the National Chip Implementation Center in Taiwan for providing the process information and fabrication platform.

REFERENCES

Amerasekera, A. and C. Duvvury, 2003. ESD in Silicon Integrated Circuits. 2nd Edn., John Wiley and Sons Ltd., USA., pp: 1-3.

Chen, S.L. and M.H. Lee, 2013. Layout strategy of P^+ pick-up on the LV MOST ESD reliability in 600nm to 180nm CMOS processes. Proceedings of the IEEE International Symposium on Next-Generation Electronics, February 25-26, 2013, Kaohsiung, pp: 51-54.

Huang, Y.C. and M.D. Ker, 2013. A latchup-immune and robust SCR device for ESD protection in 0.25im 5V CMOS process. IEEE Electr. Device Lett., 34: 674-676.

Ker, M.D., Y.R. Wen, W.Y. Chen and C.Y. Lin, 2010. Impact of layout pickups to ESD robustness of MOS transistors in sub 100-nm CMOS process. Proceedings of the IEEE International Symposium on Next-Generation Electronics, November 18-19, 2010, Kaohsiung, pp: 100-103.

Lee, J.H., J.R. Shih, S. Guo, D.H. Yang, J.F. Chen, D. Su and K. Wu, 2009. The study of sensitive circuit and layout for CDM improvement. Proceedings of the 16th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, uly 6-10, 2009, Suzhou, Jiangsu, pp: 228-232.

T-Fab, 2007. 0.35 ?m mixed signal polycide 3.3 V/5 V. Design Rule, 2007, pp: 53-58.

Zhou, A., Y. Wang, K. Zhu and X. Jin, 2012. Investigation of pickup effect for multi-fingered ESD devices in 0.5um 5V/18V CDMOS process. Electr. Lett., 48: 911-913.