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Core Test Wrapper Design for Unicast and Multicast NOC Testing

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Abstract: A novel design of a core test wrapper for NoC-based SoC is proposed in this study and the wrapper is adaptive to unicast and multicast testing. A test response comparator is particularly added to the wrapper and it improves testing efficiency and supports various test modes. Moreover, the additional parallel bypass circuit further optimizes the design. A 2D Mesh NoC was constructed with these wrapped IP cores and implemented unicast and multicast testing. The experimental results show that the wrapper can effectively realize embedded IP test access and isolation and has the good adaptability to support various NoC test strategies.

Key words: Wrapper, NoC, testing, multicast

INTRODUCTION

The design of NoC is based on reuse of IP cores in the same way as SoC and the reuse is related to logic design and testing scheme as well (Ciordas *et al*., 2005). However, IP cores produce the great challenge for testing. Effective test structure design is urgently expected for NoC testing (Nourmandi-Pour *et al*., 2011).

IEEE 1500 is the standard aimed to test access and isolation of embedded IP core. It has three important parts: test source/sink, TAM (Test Access Mechanism) and wrapper. Among them, wrapper is the component which surrounds the core and makes various IP cores homogenous for test integration. The IEEE 1500 wrapper need to be modified for NoC because the standard is mainly concerned with SoC. Amory *et al*. (2007), Hussin *et al*. (2007, 2008), Aghaei and Babaei (2009) proposed several NoC wrappers with different constraints and optimization objectives. However, none of them is applied to multicast, while multicast is increasingly employed to parallel testing (Stefan *et al*., 2012).

The IP cores wrapper for unicast and multicast NoC testing is proposed in this study. A test response comparator is added to the wrapper and the comparison of actual response and ideal response can be accomplished directly, which accelerates the testing process and increases the flexibility of test architecture. A 2D Mesh NoC is constructed and applied to unicast and multicast testing. The simulation results and performance analysis indicate that the wrapper can effectively transmit test data and has good adaptability for various testing modes.

TEST PROCESS OF EMBEDDED IP CORES ON NOC

Basic NoC topologies include Mesh, Torus, BFT, Ring (Benini and De Micheli, 2002) and our design is based on 2D Mesh structure for its simplicity and good scalability. Each IP core is connected to the corresponding router. The transmission data usually in packet format and they are packed and unpacked by the Network Interface (NI), which connects each IP and its router.

A data packet is composed of a header flit and payload flits. When the NoC is in unicast testing, test stimulus is firstly translated into flits and added the corresponding header flit (includes the destination address) to be a packet. Then the packet is set into FIFO of the router from the test source. Routing module determines the path direction based on the information of the header flit. After that, the packet is transferred between routers and eventually sent to the destination node. Finally, test response is added to the header flit, formed the result packet and sent to test sink. Unicast testing process is shown in Fig. 1a.

Multicast testing mode is to send multicast packets from test source to multiple embedded IP cores for parallel testing. There are multi node addresses in the multicast packets. The packets that belong to the IP core are received and kept by its NI, while other packets are discarded. Then the test stimulus is sent to the wrapper and the core testing is processing. The ideal test response is sent to the response comparator of the wrapper and then the comparison result will be directly generated.

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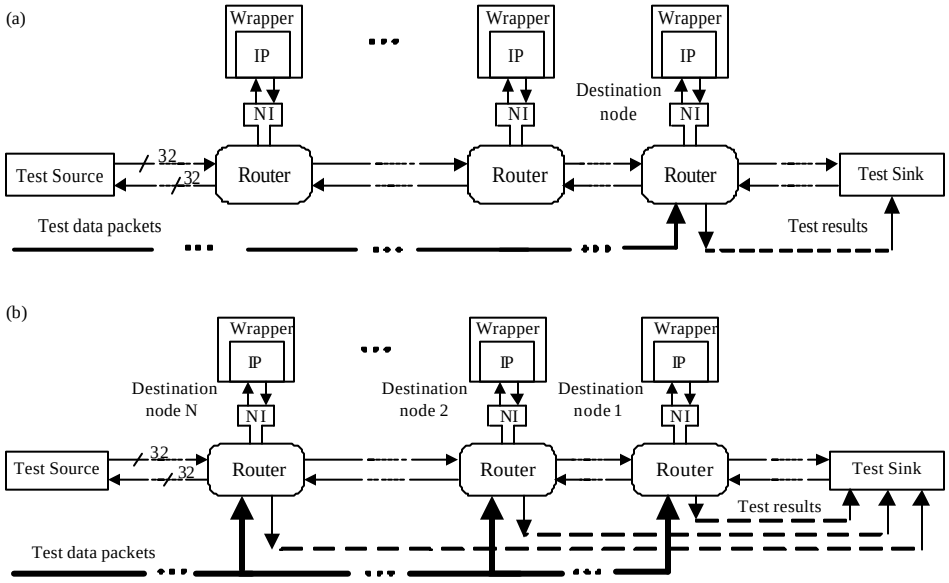

Fig. 1(a-b): Testing processes for unicast and multicast mode, (a) Unicast testing and (b) Multicast testing

Finally, the test result is sent into the NI and then transmitted into the test sink. Multicast testing process is shown in Fig. 1b.

The black solid lines in Fig. 1 behalf of test data packets and the dotted lines show the transmission of test results. Result packets are eventually transferred to test sink according to the routing information. The testing process will not finish until all test results are sent to the test sink.

WRAPPER DESIGN

Taken the ISCAS '89 reference sequence circuit S444 as the example, the wrapper implementation will be described in detail. Moreover, the process of wrapper loading and testing data transmission will be illustrated. The circuit S444 with the proposed wrapper is shown in Fig. 2.

The small blank boxes in Fig. 2 represent Wrapper Boundary Cell (WBC), Si, So are serial input/output signal, Pi [2: 0], Po [2: 0] are parallel input/output; In [2: 0], Out [5: 0] are normal function input and output. The XOR gate adjacent to the m7 in Fig. 2 is the test response comparator and there are the parallel comparison data input (Com_pi [2: 0]) and the serial comparison input (Com_si) added in the wrapper. At the end of IP core testing, the ideal test response is transferred through the Com_si or Com_pi into the wrapper and compared with the actual test response by the XOR gate. If the IP is fault-free, the output of XOR gate will be all zero, otherwise not. The test result will be stored in bit 13 to bit 0 of the head flit. Since only one flit needed to be transferred through the TAM, the burden of network is reduced and the transmission efficiency is improved.

WBY (Wrapper BYpass register) provides a rapid transmission channel for data that no need to transfer through the IP core. WBY structure diagram is shown in Fig. 3a. When the data need to transfer through the WBY, Signal Hold_en is high level and data is transmitted from Wby_in, through D flip-flop and directly output to Wby_out. In addition, there is parallel bypass register added in the wrapper to provide high speed bypass.

WBC is basic component of WBR (Wrapper Boundary Register). There should be a WBC in input/output ports (not including clock, reset signal) for observability and controllability. A WBC should include four components: Cell Function Input/Output (CFI/CFO), Cell Test Input/ Output (CTI/CTO). The WBC can be inserted into multiplexer and connected with other WBCs to form a WBR. The realization of the WBC model is shown as Fig. 3 (b). When signal *Hold_en* and *Scan_en* are low level, function data transmits to CFO from CFI; while Hold_en and Scan_en are high level, test data transmits to CTO from CTI.

The wrapper supports seven operation modes: normal function, serial bypass, parallel bypass, serial in-test, serial ex-test, parallel in-test and parallel ex-test. So there need to be signal Data_function[2:0] in the

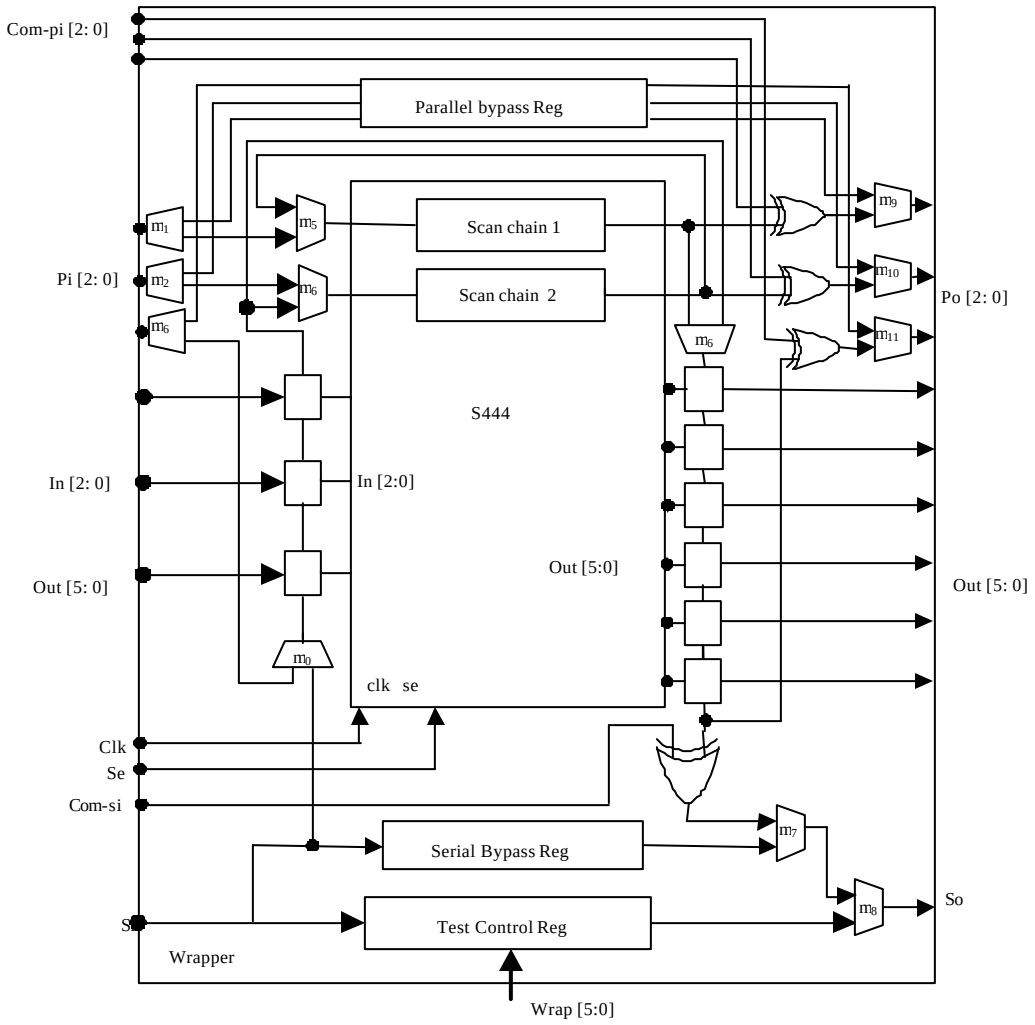

Fig. 2: Block diagram of the designed wrapper

instruction code to encode the operation modes. Instruction code transfers from Si to WIR (Wrapper Instruction Register) serially when the control signal ShiftWR is high level. While ShiftWR is low level, the instruction code is latched in WIR. When UpdataWR signal is high level, the data in the WIR is decoded and 12-bit multi-channel selector enable signal (m0 to m11), WBR enable signal Scan_en and Hold_en are generated. These signals will control the data transmission of multiplexer and WBR, so as to realize different testing modes. WIR configuration flow diagram is shown in Fig. 4.

Besides the wrapper, there are other modules needed to connect to the network. They are NI, NA (Network Adapter) and WIC (Wrapper Interface Circuit). Among them, NI is responsible for packing or unpacking the data and connecting to the router, as mentioned in Section II. NA is positioned between the Wrapper and NI and the NA also sends state information to local IP core. WIC module is applied to connect the wrapper and NA.

EXPERIMENT RESULTS

The basic function of a wrapper is to accomplish correct testing on different function modes with the prescribed timing sequences. To evaluate functions of the proposed wrapper, different function modes are configured one after another according to the standards WIP sequence and then the configuration of WBC and output results are verified. The function simulation platform is Synopsys VCS tools.

Table 1: Size comparison results

Circuit	Original size (μm^2)	With wrapper (μm^2)	Increase ratio (%)
S344	2119.917	2898.139	36.71
S382	2518.085	3410.242	35.43
S386	2005.819	1552.883	36.87
S400	2617.877	3527.851	34.76
S420	2496.756	3384.852	35.57
S444	2717.669	2801.091	34.67
S510	2624.530	3538.129	34.81
S526	3263.198	3019.160	31.97
S713	2750.933	3696.154	34.36
S953	5611.637	7377.619	31.47
S1196	6200.410	8115.717	30.89
S1238	6706.023	8761.419	30.65

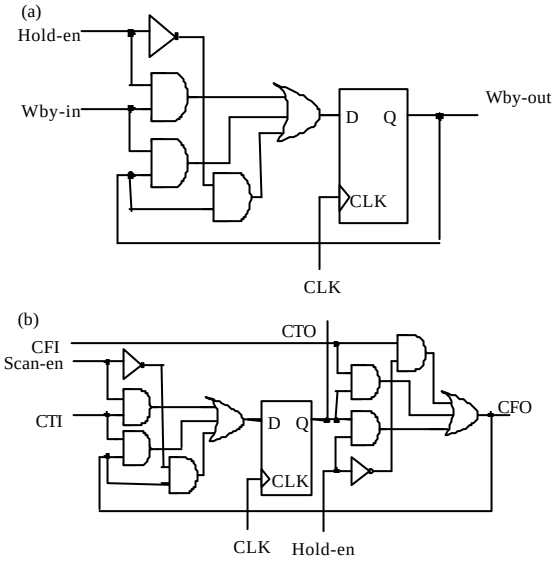

Fig. 3(a-b): Architecture of WBY and WBC, (a) WBY circuit and (b) WBC circuit

The wrapper size overhead is evaluated on ISCAS '89 circuits and comparison results over original size and with proposed wrapper are shown in Table 1. The size is increased by 1/3 on the average and the growth rate decreases with the increase of the original IP core area. Nevertheless, considering the increase of the testablity and the flexibility for various testing modes, the size overhead is acceptable.

The under test NoC is a 4×4 Mesh NoC constructed with ISCAS '89 circuits. The circuit S386, S444, S526 and S1238 are randomly inserted and formed NoC 1 and its architecture is shown in Fig. 5. The circuit S344, S400, S510 and S1196 correspond to NoC 2. The circuit S386, S420, S713 and S953 are formed NoC 3. These NoCs will be applied to validate the advance of proposed wrapper. Our wrapper is designed for support unicast and multicast testing. For comparing with the multicast, the unicast testing applies subnet to realize parallel test. The NoC can be dynamically divided into two, four or eight subnets

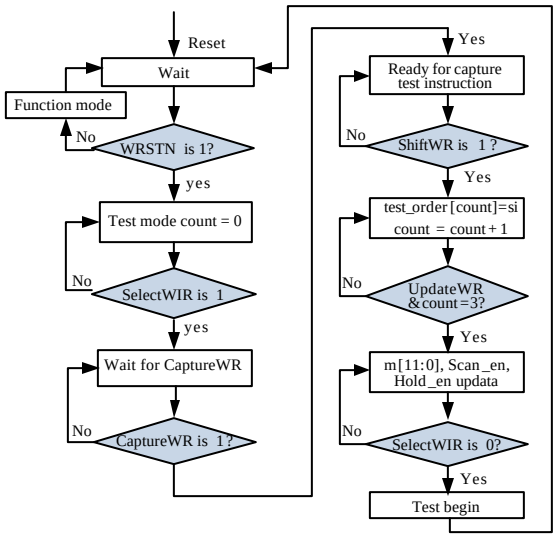

Fig. 4: WIR configuration flow chart

according to the configuration. The block diagram of subnets and peripheral circuit is shown in Fig. 6. The input/output modules directly connect to edge ports of Mesh structure.

In order to compare with subnet model test, the numbers of multicast destination nodes are set to 2, 4, 8 and 16, while the destination addresses are the same addresses of corresponding subnet. Moreover, the test data of multicast mode and subnet mode are also the same.

For subnet (unicast) testing, scheme a, b, c, d respectively means the NoC is divided into 8 subnets, 4 subnets, 2 subnets and no partition pattern; for multicast testing, scheme a, b, c, d means broadcast packets with 2 addresses, 4 addresses, 8 addresses and 16 addresses.

The transmission power of NoC test data packet is mainly related to the number of test data packets and the length of the transmission path (Cota *et al*., 2003).

Assumed that the total IP cores number is n, number of test data flits for $Core_i$ is C_i, the total number of router and channel number in testing data transmission path is NR_i and NC_i. There is $NR_i = NC_i + 1$.

The consumption powers when a test data flit is transmitted through a router or channel are T_R and T_C. Then total testing power can be calculated as follow:

$$\begin{aligned} T_{all} &= \sum_{i=1}^{n} C_i \times (N_{Ri} \times T_R + N_{Ci} \times T_C) \\ &= \sum_{i=1}^{n} C_i \times [(N_{Ci} + 1) \times T_R + N_{Ci} \times T_C] \\ &= \sum_{i=1}^{n} C_i \times [(T_R + T_C) \times N_{Ci} + T_R] \end{aligned} \quad (1)$$

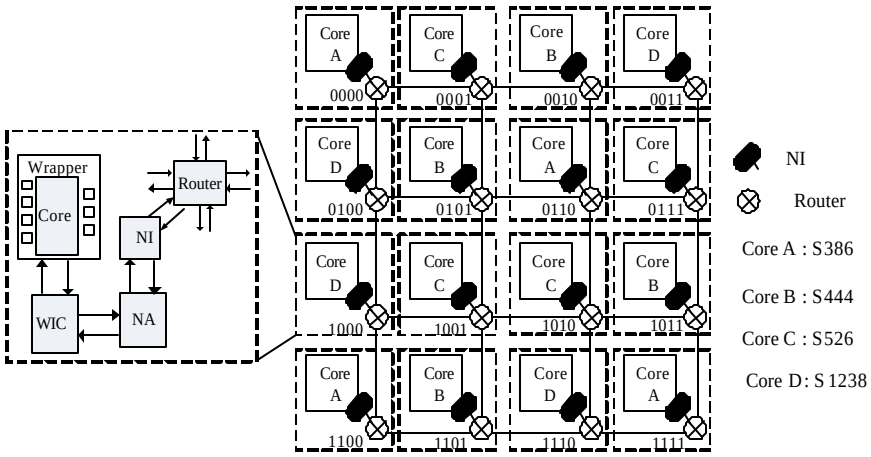

Fig. 5: NoC structure with inserted IP cores

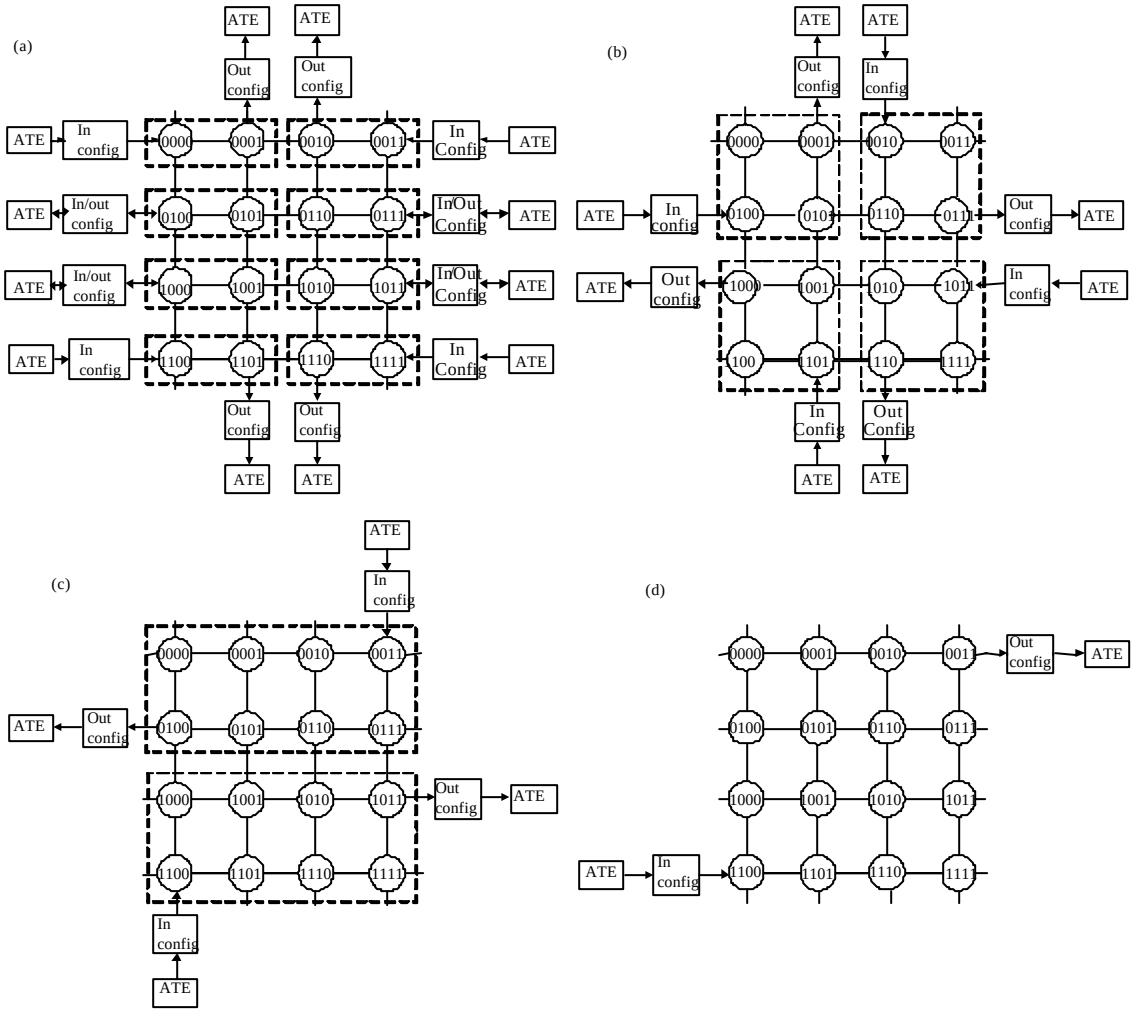

Fig. 6(a-d): Structure of subnets and peripheral circuits, (a) 8 Subnets, (b) 4 subnets, (c) 2 subnets and (d) no subnet

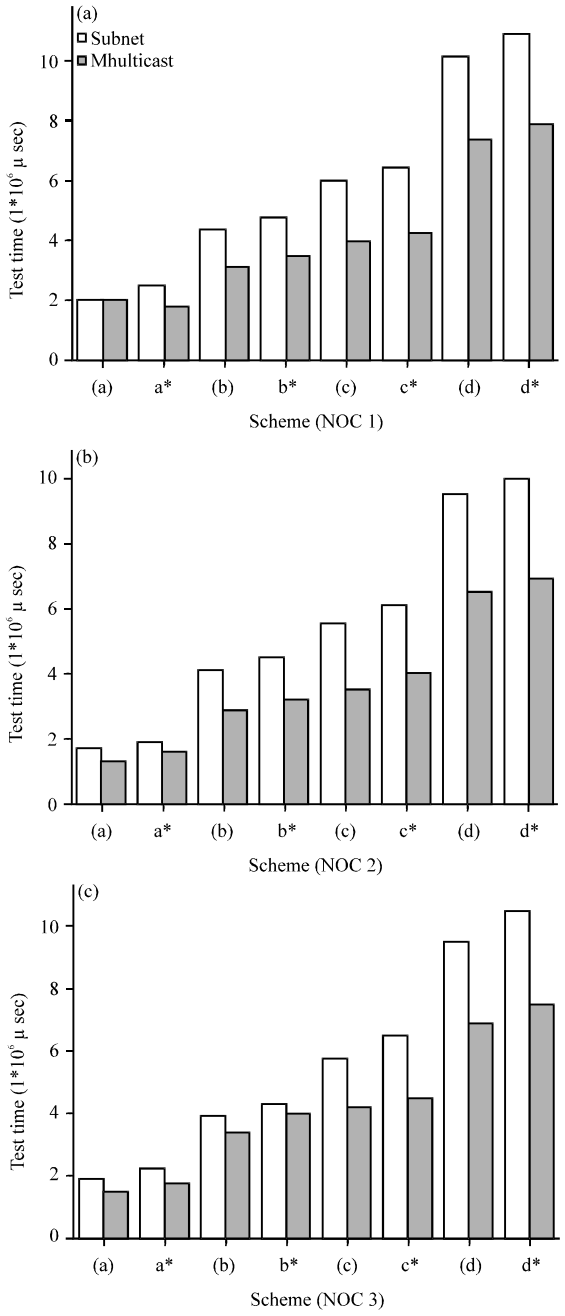

Fig. 7(a-c): Comparision of test time on different schemes

In Eq. 1, T_R and T_c are both constants, so the test transmission power T_{all} can be measured by:

$$\sum_{i=1}^{n} C_i \times N_{ci}$$

Therefore, the total number of hop counts can measure power consumption. Total hop counts and used port numbers of subnet and multicast mode with 4 schemes are shown in Table 2. The hop counts gradually increase from scheme a to scheme d, while the port numbers decrease. In addition, it is obvious that the power consumption of multicast mode is much lower than subnet mode.

Table 2: Hop and port number comparison

	Hop No.		Port No.	
Scheme	Subnet	Multicast	Subnet	Multicast
(a)	16	16	12	12
(b)	32	28	8	8
(c)	64	52	4	4
(d)	96	63	2	2

Based on the designed wrapper, testing time of subnet and multicast modes can be evaluated. Moreover, the test time on wrapper without comparator are also provided to evaluate the advancement of designed wrapper. Applying eight schemes of two testing modes on NoC 1, NoC 2 and NoC 3, test time results (CLK is 50MHz) are shown in Fig. 7. Among them, scheme a*, b*, c*, d* are applied with no comparator wrappers.

Some conclusion can be drawn from the experiment results as follows:

- The test time of schemes with designed wrapper is shorter than with the no comparator wrapper, which shows the additional comparator is effective to decrease the test time
- The subnet (unicast) mode is more time-consuming than the multicast mode. Although the subnet test mode as a whole is parallel, the data transmission in each subnet is still serial. On the other side, multicast testing for each IP core is really concurrent
- The test time of scheme (a) is the shortest but its hardware overhead is the most for using 12 peripheral ports. The peripheral port number of scheme (b) is twice as much as scheme (c), while the test time of scheme (b) is not significantly reduced comparing with scheme (c). The subnet of scheme (d) is totally serial, so the test time is the longest. Even for multicast mode, scheme (d) is much time-consuming because the number of parallel test port is too small

CONCLUSION

This study described an improved wrapper of embedded IP core on NoC. The wrapper can effectively support unicast and multicast testing. The particular test response comparator in the wrapper can directly confirm whether the IP core is faulty, so that greatly improves the testing efficiency and flexibility. Unicast and multicast testing on 2D Mesh NoC are implemented with the

proposed wrapper. Test power consumption and test time on these NoCs are evaluated and experiment results indicate that the wrapper has correct functions and is flexible to different testing modes. Currently, a scheme aimed to maximize NoC testing parallelism based on designed wrapper is being studied.

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REFERENCES

Aghaei, B. and S. Babaei, 2009. The new test wrapper design for core testing in packet-switched micro-network on chip. Proceedings of the 2nd International Conference on Power Electronics and Intelligent Transportation System, Volume 2, December 19-20, 2009, Shenzhen, China, pp: 346-352.

Amory, A.M., K. Goossens, E.J. Marinissen, M. Lubaszewski and F. Moraes, 2007. Wrapper design for the reuse of a bus, network-on-chip, or other functional interconnect as test access mechanism. IET Comput. Digital Tech., 1: 197-206.

Benini, L. and G. De Micheli, 2002. Networks on chips: A new SoC paradigm. IEEE Comput., 35: 70-78.

Ciordas, C., T. Basten, A. Radulescu, K. Goossens and J.V. Meerbergen, 2005. An event-based monitoring service for networks on chip. ACM Trans. Design Autom. Electron. Syst., 10: 702-723.

Cota, E., L. Carro, F. Wagner and M. Lubaszewski, 2003. Power-aware NoC reuse on the testing of core-based systems. Proceedings of the International Test Conference, September 30-October 2, 2003, Charlotte, CA., USA., pp: 612-621.

Hussin, F.A., T. Yoneda and H. Fujiwara, 2007. Optimization of NoC wrapper design under bandwidth and test time constraints. Proceedings of the 12th IEEE European Test Symposium, May 20-24, 2007, Freiburg, Germany, pp: 35-42.

Hussin, F.A., T. Yoneda and H. Fujiwara, 2008. On NoC bandwidth sharing for the optimization of area cost and test application time. IEICE Trans. Inform. Syst., 91: 1999-2007.

Nourmandi-Pour, R., N. Mousavian and A. Khadem-Zadeh, 2011. BIST for network on chip communication infrastructure based on combination of extended IEEE 1149.1 and IEEE 1500 standards. Microelectron. J., 42: 667-680.

Stefan, R., A. Molnos, A. Ambrose and K. Goossens, 2012. A TDM NoC supporting QoS, multicast and fast connection set-up. Proceedings of the Conference on Design, Automation and Test in Europe, March 12-16, 2012, Dresden, Germany, pp: 1283-1288.