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A Soft-switching Full-bridge Inverter Working in the Current and Voltage Combination Fed Mode

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Abstract: In this study a new soft-switching full-bridge dc-ac inverter working in the combination of current-fed mode and voltage-fed mode is proposed. The proposed circuit is inserted by two small flyback transformers to reduce the current spike, minimize switching loss at the turn-on instance and eliminate the interference on the non-working MOSFET from the working MOSFET, thus leading to high efficiency and reliable benefit over traditional full-bridge dc-ac inverters. At the same time, the implementation of control schemes is very simple. In this study, the proposed dc-ac inverter operating principle is analyzed and simulation and experimental results are given to demonstrate the validity and features of the soft switching and lower current spikes.

Key words: Pulse width modulation inverters, circuit optimization, electromagnetic interference

INTRODUCTION

The crisis of energy promotes the exploit of new energy and the research on energy savings and dc-ac inverter is the key factor for the energy storage. The voltage-fed full-bridge inverter topology is widely used for high-power inverters and the inverter usually works in Continuous Current Mode (CCM) in order to reduce the harmonics and the impact on the grid. The basic voltage-fed full-bridge inverter circuit is shown in Fig. 1. According to the modulation principle, there are two kinds of Sinusoidal Pulse Width Modulation (SPWM) as unipolar SPWM and bipolar SPWM. The basic full-bridge working in CCM and unipolar SPWM is more popular in engineering applications because of its high efficiency and low ripple. Assuming that MOSFETs S2 and S4 work in the low-frequency switching state, MOSFETs S1 and S3 work in the SPWM switching state. To drive in the forward direction, during the half period of the line frequency MOSFETS S1 and S4 hold off and MOSFET S2 holds on, MOSFET S3 is switched with a SPWM signal, while the MOSFET S4 body-drain diode D4 acts as the free-wheeling diode during MOSFET S3 is off. An alternative arrangement is to MOSFETS S1 and S4 and the body-drain diode D2. Grant and Gowar (1989) presented a detail description about the working principle.

Hirachi *et al.* (1998) presented the disadvantage of the inverter working in the voltage-fed mode, voltage-fed mode implies that the source impedance of whatever drives the topology is low and hence there is no way of limiting the current drawn from it during unusual conditions at power switch turn "on" or turn "off," or under various fault conditions in the topology . At the turn-on moment of MOSFETs S1 or S3 a current spike comes into being because of the capacitance of the MOSFET and body-drain diode D2 or D4 reverse-recovery-current. The current of MOSFET S1 or S3 is:

$$i_D = C_{DS}\frac{dV_{DS}}{dt} + V_{DS}\frac{dC_{DS}}{dt} \quad (1)$$

The current spikes are so severe to cause the MOSFETs gate oscillation, excessive power dissipation and high electromagnetic interference. To limit the current mutations an external choke may be added in series with the MOSFETS and the most direct way is the current-fed converter topology. Mohan *et al.* (2002) presented a way to reduce current spike using an inductor in series with a resistor-capacitor snubber but it is not suitable for high-power inverter because of the excessive power dissipation.

The full-bridge converter working in current-fed mode is shown as Fig. 2. It is an effective way to reduce or eliminate the current spikes because the high instantaneous impedance of an inductor L1 is interposed between the power source and the topology. This provides a number of significant advantages, especially in high power supplies, high output voltage supplies and multi-output supplies as descripted Pressman *et al.* (2009). Weinberg (1974) proposed a new converter, Weinberg converter and such circuit has many of the valuable attributes as descripted Pressman *et al.* (2009). But in practice, this current-fed PWM inverter has a significant disadvantage in dc-ac inverter current power supplies.

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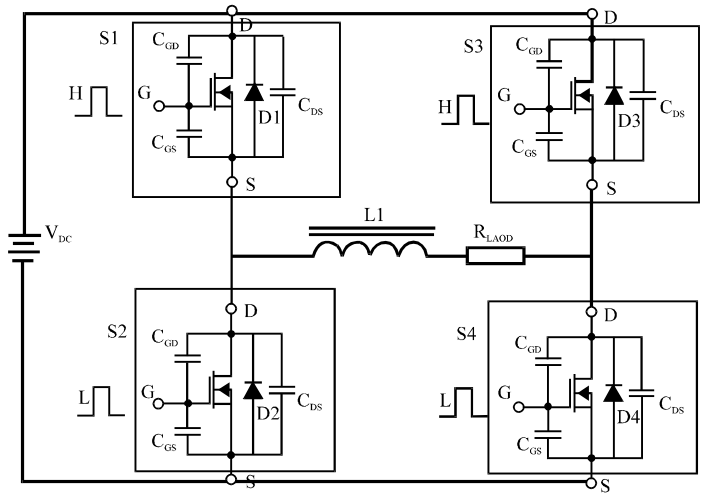

Fig. 1: Basic voltage-fed inverter

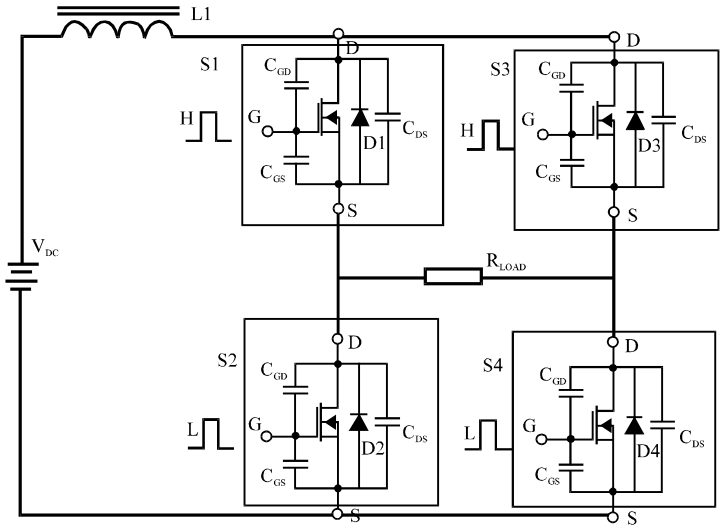

Fig. 2: Current-fed converter

The output current of this inverter includes large harmonic contents when the inductance of smoothing reactor in its DC side is not large enough to eliminate its current ripple components of this inverter as descripted in the literature (Delshad and Farzanehfard, 2011).

For the above problems, this study has proposed a Current and Voltage Combine Fed Mode inverter circuit (CVCFM Inverter) based on the analysis of the conventional current-fed full-bridge converter and the voltage-fed full-bridge inverter. Compared with the conventional bridge inverter the CVCFM inverter circuit has the following improvements: (1) it can effectively prevent the current mutation to reduce the current spike and electromagnetic interference, (2) it bring about the MOSFET soft-switching of the inverter to get higher power efficiency of the inverter, (3) it eliminates basically the interference on the non-working MOSFET to enhance the stability of the circuit and (4) it is able to prevent a short-term dead short-circuit of a bridge arm to enhance the stability and gain the necessary action time of the protection circuit.

CVCFM INVERTER

The proposed CVCFM inverter is shown as Fig. 3, two flyback transformers are interposed between the power source and the full-bridge topology composed of four MOSFETs S1, S2, S3 and S4. The whole circuit works in CCM and unipolar SPWM mode. Assuming that MOSFETs S2 and S4 work in the low-frequency switching state, MOSFETs S1 and S3 work in the SPWM switching state, respectively with the body-drain diode D2 and D4.

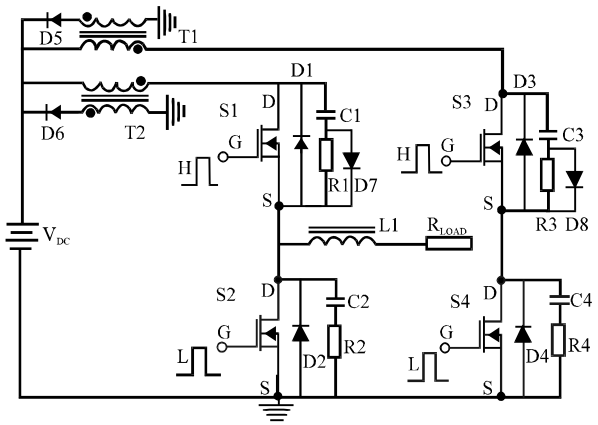

Fig. 3: CVFM inverter

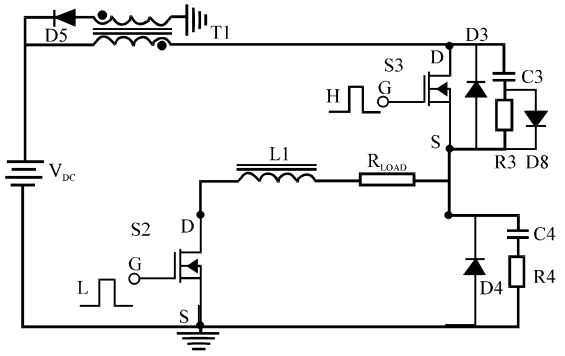

Fig. 4: CVCFM inverter working in the positive half period of line frequency

The CVCFM inverter works almost in voltage-fed mode but the flyback transformer make the inverter work in the current-fed mode at turn-on moment which can play an effective suppression of the current spike and the interference on the non-working MOSFETs from the working MOSFETs. The Resister, Capacitor and Diode snubber circuits (RCD snubber) absorb the voltage spike caused by the flyback transformer leakage inductance and the oscillation caused by the MOSFET parasitic capacitance. Inductor L1 as inverter filter inductor make the output current continuous and smooth and the load R_{LOAD} may be resister or connecting to the grid.

The CVCFM inverter has the similar working principle with the conventional voltage-fed inverter and then it has the same control strategy. The flyback transformer T1 works when the MOSFET S2 and S3 and body-drain diode D4 work during the positive half cycle of the line frequency and on the other hand the flyback transformer T2 works in the other half cycle. According to the symmetry of the circuit structure and working principle the following analysis are presented only for the positive half cycle of the line frequency. To make the circuit more clearly, the CVCFM inverter working in the positive half cycle is simplified as Fig. 4.

THE WORKING PRINCIPLE OF CVCFM INVERTER

Assuming that at the moment t_0 the initial state is that the freewheeling current flowing through the MOSFET S2 and diode D4 and the filter inductor is the output current, at the same time no current flows through the flyback transformer T1 and the MOSFETs S1, S3 and the body-drain diode D4 holds off.

Mode 1 (t_0-t_1): This interval starts by turning S3 on; at the Moment t_0 the voltage V_{GS3} increases from low level and the voltage V_{DS3} decreases rapidly from DC bus voltage and the voltage V_{DS3} became almost zero when the voltage V_{GS3} reaches the threshold voltage of the MOSFET at the Moment t_1. The transformer T1 acts as an inductor, so the current flowing T1 and S3 keeps almost zero in this interval, while the current flowing through diode D4 remains nearly unchanged. Therefore, due to the presence of the flyback transformer the inverter achieves soft-switching and the switching loss is greatly reduced compared with the conventional inverter.

Mode 2 (t_1-t_2): In this interval the voltages V_{DS3} and V_{DS4} keep zero because the diode D4 remains conductive. Thus the voltage of the DC bus is applied to the primary side coil of the transformer T1 and the diode D5 holds off because of the reverse voltage of the secondary side coil. The current i_{DS3} flowing through the MOSFET S3 and the primary side coil of the transformer T1 increases gradually because of the primary side inductance L_{T1P} of the transformer T1 until the current i_{D4} flowing through the diode D4 decreases to the reverse-recovery current and now the transformer T1 begins to store energy. Because the capacitance CM of the MOSFET parasitic capacitor and the capacitor in the RCD snubber is very small compared with the primary side inductance L_{T1P} of the transformer T1, that is $X_{LT1P} \gg X_{CM}$, such capacitance can be negligible. The current i_{DS3} and i_{D4} are:

$$i_{DS3} = i_{T1P} = \frac{V_{in}}{L_{T1P}} \cdot (t - t_1) \tag{2}$$

$$i_{D4} = -i_{L1} + \frac{V_{in}}{L_{T1P}} \cdot (t - t_1) \; i_{D4} = -i_{L1} + \frac{V_{in}}{L_{T1P}} \cdot (t - t_1) \tag{3}$$

where, i_{L1} is the current flowing through the filter inductor L1. Thus, according to the Eq. 2 the current spikes depend on the primary side inductance of the transformer T1 and the current spikes are much smaller than that in the conventional inverter with comparing Eq. 1 and 2.

Mode 3 (t_2-t_3): This interval starts by the switching-off of the diode D4 and the current i_{DS3} and i_{D4} begin to decrease. The voltages across the transformer coil reverse and the diode D5 begin to be conductive, the transformer

dissipates the energy to the DC source, thus, the voltage across the second side coil of T1 is the input DC bus voltage, V_{DC} and the voltage across the primary side coil of T1 is V_{DC}/n, where n is the transformer winding turns ratio. The voltage across the drain and source of S3 become nearly zero and the voltage across the drain and source of S4 is:

$$V_{DS4} = V_{in} + V_{in}/n = (1+1/n)V_{in} \tag{4}$$

The current flowing through the inductor L1 is:

$$i_{L1}(t) = i_{L1}(t_2) + \frac{(1+1/n)V_{in}}{L_1}\cdot(t-t_2) \tag{5}$$

At the moment t_3, the current flowing through the second side coil of T1 decrease to zero, the diode D5 cut off and now $V_{DS4} = V_{in}$, $i_{L1}(t_3)$, $i_{D4} = 0$.

Mode 4 (t_3-t_4): Due to the inductance of the primary coil is much smaller than that of the inductor L1, that is $L_{T1P} << L1$ and so the role of the transformer can be negligible and the circuit works as the voltage-fed inverter in this interval. So:

$$\begin{aligned} &V_{DS3} = V_{DS2} = 0, i_{D1} = i_{D4} = 0\\ &i_{D2} = i_{D3} = i_{L1} = i_{L1}(t_3) + \frac{V_{in}}{L_1}\cdot(t-t_3)\\ &V_{DS1} = V_{DS4} = V_{in} \end{aligned} \tag{6}$$

Mode 5 (t_4-t_5): At the moment t_4 the voltage V_{GS3} began to decrease and when V_{GS3} drops to the MOSFET threshold the RCD snubber circuit takes over the decreasing current that has flown through the MOSFET S3 to avoid voltage spikes. The voltage V_{GS3} increases gradually due to the capacitance in the RCD snubber circuit and thus makes the MOSFET turn-off losses lower. The voltage V_{GS3} is:

$$V_{DS3} = V_{in} + V_{in}/n = (1+1/n)V_{in} \tag{7}$$

Now the voltages of the transformer coil reverse and the diode D5 get conductive to send back the energy from the transformer to the DC bus through the second side coil which is effective energy-saving way compared with the way using resister in the literature (Mohan *et al*., 2002).

Up to the moment t_5 the current flowing through the diode D5 decreases to zero and now $V_{DS4} = 0$ and $V_{DS3} = V_{in}$. Through the entire interval the inductor L1 release of energy and the current decreases:

$$i_{DS2} = i_{L1} = i_{L1}(t_4) - \frac{V_{out}}{L_1}\cdot(t-t_4) \tag{8}$$

Mode6 (t_5-t_6): During the interval the transformer T1 doesn't work, the inductor L1 release the energy through the MOSFET S3 and the diode D4. Now:

$$\begin{aligned} &V_{DS4} = V_{DS2} = 0, V_{DS1} = V_{DS3} = V_{in}\\ &i_{D1} = i_{D3} = 0\\ &i_{DS2} = i_{D4} = i_{L1} = i_{L1}(t_4) - \frac{V_{OUT}}{L_1}\cdot(t-t_4) \end{aligned} \tag{9}$$

SIMULATION AND EXPERIMENTAL RESULTS OF THE CVCFM INVERTER AND THE CONVENTIONAL VOLTAGE-FED INVERTER

In order to verify the validity of the proposed circuit, a simulation has been carried out the CVCFM inverter through the software OrCAD Capture 16.3. In the simulation the MOSFETs adopt the SPW35N60C3_L1 model from the Infenion Company. Because the junction capacitance of the diodes D5 and D6 should be as small as possible, they utilize the model of two diodes MUR850 in series and the diode D7 and D8 use the MUR890 model, respectively. The primary side coil inductance of the transformer T1 and T2 is 15 μH, the secondary side coil inductance is 90 μH. Table 1 shows the parameters of other devices.

In order to make a better description of the improvement of the CVCFM inverter, a simulation was also carried out on the conventional voltage-fed inverter. In the two circuits the devices and their parameters are exactly the same in addition to no flyback transformer T1 and T2 in the conventional circuit.

Figure 5 shows the waveforms and the comparison at some critical points of the two circuits. With Fig. 5a and b being compared, it is clear that the peak value of the current spike has decreased from 110 to 38 A which slows down the EMI (Electric Magnetic Interference) greatly due to the lower current changes and

Table 1: Device parameters list of the inverter

Symbol	Description	Quantity
V_{DC}	DC bus voltage	400 V
L_1	Output filter inductor	1.6 mH
C_1	RCD snubber capacitor	10 nF
C_2	RC snubber capacitor	10 nF
C_3	RCD snubber capacitor	10 nF
C_4	RC snubber capacitor	10 nF
R_1	RCD snubber resister	200 Ω
R_2	RC snubber resister	200 Ω
R_3	RCD snubber resister	200 Ω
R_4	RC snubber resister	200 Ω
R_{LOAD}	Resister as load	20 Ω

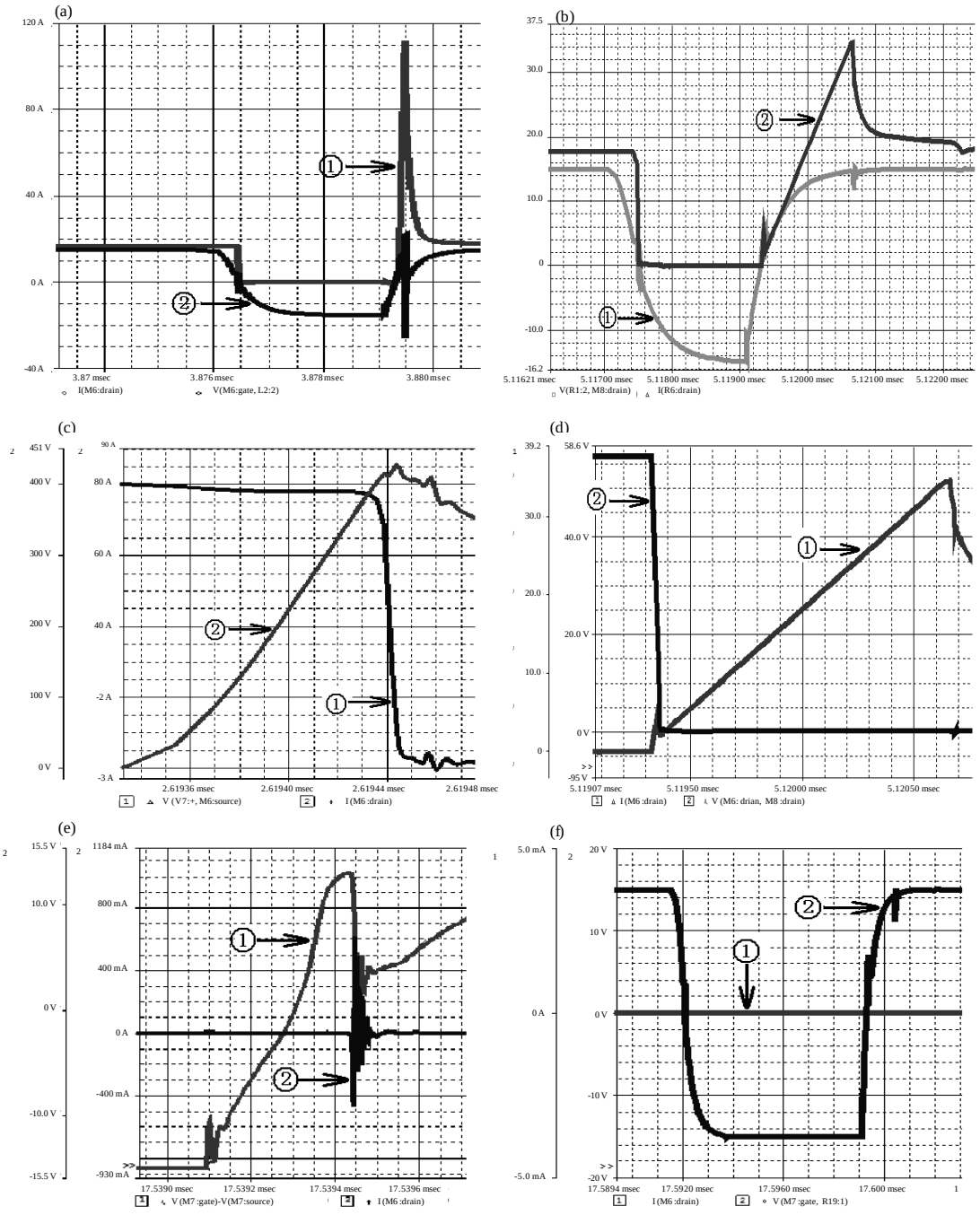

Fig. 5(a-f): (a) The waveforms and the comparison at some critical points of the two circuits, (②) the voltage VGS and (①) the current IDS, (b) Waveforms in the conventional inverter, (①) the voltage VGS and (②) the current IDS, (c) Waveforms in the CVCFM inverter, (①) The voltage VDS and (②) the current IDS, (d) Waveforms at the turn-on moment in the conventional inverter, (②) The voltage VDS and (①) the current IDS, (e) Waveforms at the turn-on moment in the CVCFM inverter, (①) The voltage VDS in working MOSFET and (②) the current IDS in nonworking MOSFET, (f) Waveforms at the turn-on moment in the conventional inverter and (②) the voltage VDS in working MOSFET and (①) the current IDS in nonworking MOSFET waveforms at the turn-on moment in the CVCFM inverter

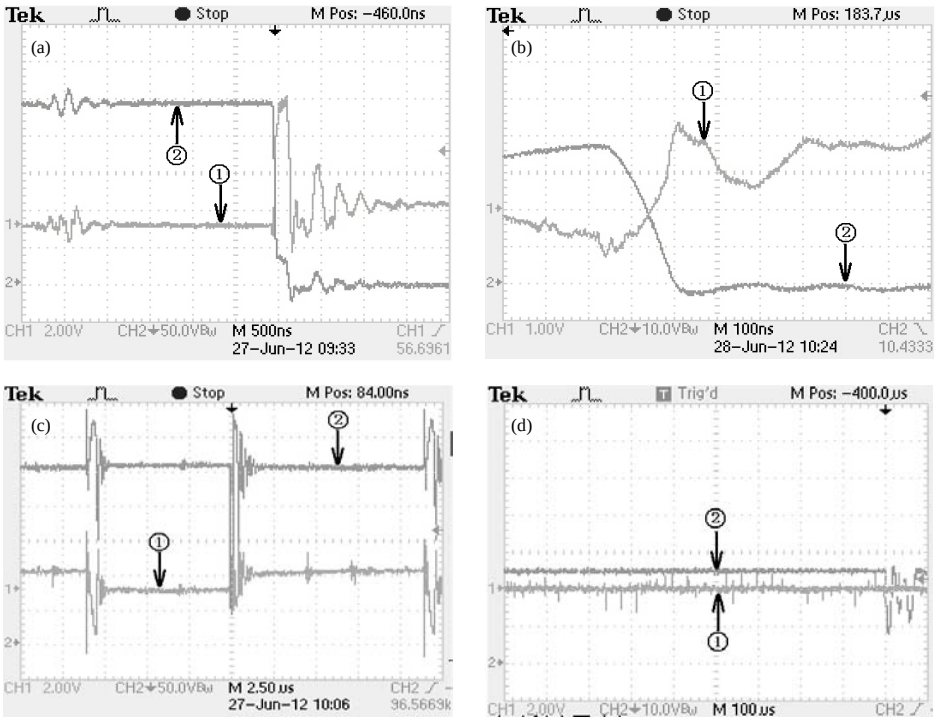

Fig. 6(a-d): (a) The waveforms at some critical points of the two circuits in the prototype, (②) The voltage VGS and (①) The current IDS, (b) Waveforms in the conventional inverter, (②) The voltage VGS and (①) the current IDS, (c) Waveforms in the CVCFM inverter, (②) The voltage VDS in working MOSFET and the current IDS (orange) in nonworking MOSFET and (d) Waveforms in the conventional inverter and (②) The voltage VDS and (①) the current IDS waveforms in nonworking cycle in the CVCFM inverter

its impact on the voltage V_{GS} waveforms has also got an improvement. With the comparison of Fig. 5c to d, the current spike leads to high loss in the conventional circuit, while the CVCFM inverter has greatly reduced the power loss with the zero current switching. With the comparison of the Fig. 5e to f, in the CVCFM inverter the interference on the nonworking MOSFET from the working MOSFET has almost vanished because of the flyback transformer T1 and T2 and at the same time the CVCFM inverter reduces the short-circuit possibility to enhance the reliability of the inverter.

A prototype was also made to verify the proposed CVCFM inverter. The proposed inverter is designed for 270 V input voltage, 2 kW output power and switching frequency of 50 kHz. The same components are used in the experimental prototype as that in the simulation but the leakage inductor should never be neglected in the experimental prototype. The current is measured by the voltages through six paralleled resistors of 0.5 Ω. Experimental results are shown from Fig. 6. The actual value should be 10 times of the value in channel 2 in Fig. 6c and d because of the attenuation. The comparison of Fig. 6a and b shows the characteristics of lower current spikes and better ZCS in the CVCFM inverter. With the comparison of the Fig. 6c to d, it is clear that there is less interference on the nonworking MOSFET in the CVCFM inverter.

CONCLUSION

Combined with the current fed inverter and the voltage fed inverter circuit characteristics, this study proposed an improvement program to the conventional full-bridge inverter with the analysis of engineering problems and the problems of the traditional continuous current output of the inverter circuit. The proposed inverter greatly reduces the current spike of the power MOSFET with the lower EMI and high reliability and has increased the power conversion efficiency with the soft switching. On the other hand, the proposed circuit breaks

the boundary between the voltage-fed mode and the current-fed mode and it has laid a good foundation for the combination mode. The proposed CVCFM program applies not only to the inverter circuit working in the continuous current mode but also can be extended to other bridge converter.

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