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Near-threshold Computing and Performance Optimization of MOS Current Mode Logic Circuits

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Abstract : This study presents near-threshold computing and performance optimization for MCML circuits to attain both low power dissipation and high speed. Unlike the traditional MCML circuits, the output swing of the MCML circuits used in this paper is larger than the threshold voltage of NMOS transistors and the NMOS logic blocks of the MCML circuits operate on linear region, so that their source voltages can be effectively reduced. A near-threshold decimal counter is optimized in term of power dissipation and delay by using the proposed optimization algorithms. All circuits are simulated using SMIC 130 nm technology by varying supply voltage from 1.3 V to 0.4 V with 0.1 V step. The results show that the power consumption of the optimized MCML circuits can effetely be reduced by lowering the supply voltage over a wide range of frequencies.

Key words: MOS current-mode logic, near-threshold computing, optimization algorithm

INTRODUCTION

In MOS Current-Mode Logic (MCML) circuit, source voltage V_{DD} represents logic 1, while V_{DD}-ΔV (ΔV represents output voltage swing) means logic 0. Obviously, its swing is much little than conventional CMOS circuits and thus the circuits designed with the MCML techniques can operate over a higher speed (Yamashina and Yamada, 1992; Alioto and Palumbo, 2003). Therefore, MCML is widely used for high-speed applications such as high-speed processors and Gbps multiplexers for optical transceivers (Tanabe *et al*., 2001; Musicer and Rabaey, 2000). Another interesting advantage of this technique is that their speed and power consumption can be simply adjusted by altering the bias current of the gates without the need for resizing the devices (Anis and Elmasry, 2002; Hi and Li, 2013).

However, the power consumption of a MCML circuit with given voltage and current is a constant. Therefore, the power consumption of the MCML circuit is independent of frequency (Hi and Li, 2013). This means that the MCML circuits have large static power due to their constant operation currents, especially for low-frequency operations (Anis and Elmasry, 2002). Nowadays, energy has become one of the most valuable sources. With the increasing demand for battery-operated mobile platforms like portable computers, laptops, cellular phones, wireless sensors and biomedical applications that require ultra-low energy dissipations, energy-efficient designs have become more and more important for nanometer CMOS circuits (Zhang *et al*., 2011).

In nanometer CMOS digital circuits, power dissipation consists mostly of dynamic and static components. One direct solution for reducing energy consumption of conventional CMOS circuits is to scale supply voltage. In the conventional CMOS circuits, scaling supply voltage to sub-threshold region can reach minimum energy consumption (Markovic *et al*., 2010). However, sub-threshold circuits only fit low-performance (50 kHz-5 MHZ) application (Markovic *et al*., 2010). For conventional CMOS circuits, scaling supply voltage to medium-voltage region can not only keep reasonable speed but also reduce energy consumption (Hu and Chen, 2012).

Similarly, the power consumption of the MCML circuits can also be reduced by lowering the supply voltage (Wu and Hu, 2011). To the best of our knowledge, the performance optimization on near-threshold MCML circuits has not been presented. In order to attain both low power dissipation and high speed, near-threshold computing for MCML circuits is addressed in this work. The performance optimization for near-threshold MCML circuits is also proposed.

MCML CIRCUITS

The basic MCML inverter/buffer and its bias circuit are shown in Fig. 1 (Yamashina and Yamada, 1992; Hassan *et al*., 2005). The MCML inverter is composed of three main parts: the load transistors P1 and P2, the full differential pull down switch network consisting of N1

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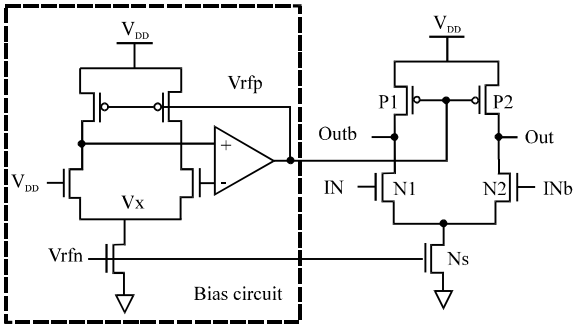

Fig. 1: MCML inverter/buffer and its bias circuit

and N2 and the current source transistor Ns. The load transistors are designed to operate at linear region with the help of the control voltage V_{rfp} produced by the bias circuit, which also controls the output logic swings. The Pull-down Network (PDN) NMOS N1 and N2 are used to perform logic operation. The NMOS Ns is used to provide the constant current source, which is mirrored from the current source in the bias circuit. In the MCML, the two signals V_{rfp} and V_{rfn} are generated from the bias circuit to ensure the proper operating for output voltage swings and to provide the constant bias current. This construction decide that $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD}$-I_{BRD}, where R_D is the PMOS load resistance. The logic swing:

$$\Delta V = V_{OH} - V_{OL} = I_B R_D.$$

The traditional MCML circuits make the pull-down network operate in saturated region. To achieve this goal, the output swing must be controlled below threshold voltage. With the scaling-down of technology dimension, the threshold voltage of transistors is reduced. The typical threshold voltage of transistors is between 0.2 and 0.3 when dimension is below 130 nm. In order to make the pull-down network operate in saturated region, the output swing must be smaller than this threshold voltage, which may lead to bad performance on noise margin. In order to solve this problem, the pull-down network operates in linear region. In other words, the output swing is larger than threshold voltage. All MCML circuits mentioned in this work are worked with an output swing of 0.3 V.

MCML is a type of differential logic with differential input logic tree. Therefore, the design of the MCML PDN is similar to other differential logic styles such as DCVSL and DSL. The complex logic functions can be realized by replacing N1 and N2 with NMOS logic trees. When we design a MCML circuit, two parts can be divided. One part is Bias Circuit and another part is logic circuit. The MCML basic gate cells such as AND2/NAND2, OR2/NOR2, XOR2/XNOR2 and AND3/NAND3 are shown in Fig. 2.

The power consumption of MCML circuits can be expressed as:

$$P = V_{DD}I \quad (1)$$

where, I is source current. Easily, energy consumption per cycle can be expressed as:

$$E = V_{DD}I / f \quad (2)$$

where, T is operation period and f is frequency. In Eq. 2, a direct solution for reducing energy consumption is to scale down supply voltage, since the total energy is reduced linearly as supply voltage scales down. Scaling supply voltage to near-threshold region is an attractive approach.

ANALYSIS MODELING OF MCML CIRCUITS

The design variables in MCML circuits include mostly the circuit bias current (I), PMOS load transistors sizes (W_p and L_p), transistors sizes of the NMOS differential pull-down network (W_n, L_n), transistors sizes of current source (W_s, L_s) and the current source bias voltage (V_{rfn}).

The performance parameters in MCML circuits include mostly circuit delay t_d, total power dissipation P, voltage swing ΔV, voltage gain A_v, noise margin NM, voltage swing ratio VSR and the signal slope ratio SSR. In order to carry out performance optimization for near-threshold MCML circuits, the relations between performance parameters and design variables should be established (Musa and Shams, 2010).

Delay: The PMOS transistors are worked as ideal resistances with a value of R. The total capacitance can be departed into two parts, the internal one and the external one. Internal one consists of C_{gd} and C_{db}, they are the gate-drain overlap and drain diffusion capacitances of the MOS, respectively. The external load capacitance is C_L that consists of the sum of wiring and total fan-out capacitances of circuits. Using first-order circuit analysis, circuit delay t_d is approximated by:

$$t_d = 0.69\ RC \quad (3)$$

where, C is expressed as:

$$C = C_{db1}+C_{db2}+C_{gd1}+C_L \quad (4)$$

DC voltage gain: The DC voltage gain A_v is a key parameter for the regeneration and stability in a MCML circuit. It should not be smaller than 1.4. A_v can be expressed as:

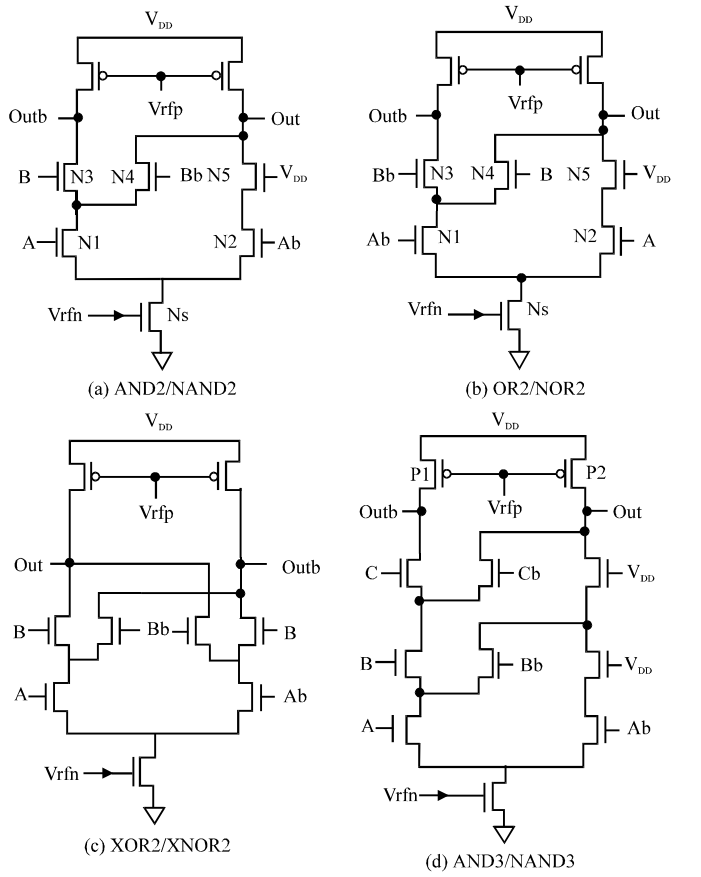

Fig. 2: Basic gate cells based on MCML

$$|A_V| = \frac{R\mu_n C_{ox}\frac{W_3}{L_3}(V_y - V_x)\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I}}{\mu_n C_{ox}\frac{W_3}{L_3}(V_y - V_x) + \sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I}} \quad (5)$$

where, μ_n is the electron mobility, C_{ox} is the oxide capacitance of the MOS transistor, V_y and V_x are the voltages between internal nodes.

Noise margin: It is significant to achieve a sufficiently large noise margin in MCML circuits because of its reduced voltage swing. But with a unique frame, MCML circuits can accept a small value for NM (Noise Margin). Theoretically, the maximum NM is ΔV, as A_v is large enough. Practically, 0.4 ΔV is sufficient to ensure proper circuit operation.

Voltage swing ratio: In reality, not all the current I generated by the NMOS transistor Ms is steered to the ON branch, a part of the current I flows to the OFF branch and thus the output voltage swing reduces. This issue is more severe in cascaded circuits because the quality of current switching will continue to drop. To solve this problem, the current flowing through the OFF branch must be constrained to a limited percent of total current. VSR (Voltage Swing Ratio) is defined as the ratio between the current in the ON branch Ion and the total current. It can be expressed as:

$$VSR = VSR_u \times VSR_l \quad (6)$$

where, VSR_u and VSR_l are the values of VSR at the upper and lower levels of the MCML circuit, respectively. In order to achieve a VSR of 95%, VSR_u and VSR_l should not be smaller than 97%.

Signal slope ratio: Speed is an important issue in MCML circuits. A metric is needed to ensure that their output response will not have long rise/fall time t_{rf} with respect to t_d. SSR (Signal Slope Ratio) is defined as the ratio between t_{rf} and t_d and it is expressed as:

$$SSR = t_{rf}/t_d \quad (7)$$

To get a reasonable output waveform, SSR is limited to a maximum of 5.

Device size of differential pair transistors: A large width of differential pair transistors increases A_v and at the same time adds up to the load capacitance. Hence, in order to get a reasonable channel width, a compromise between C_L and A_v must be made.

As is known to all, an increasing channel length adds up to the parasitic capacitance and thus results in a longer time delay. Therefore, for differential pair transistors, the channel length should be chosen as minimum size of the technology.

Current source design variable: The current source transistor Ms has two main influence factors. One is the current source common-mode rejection ratio (CMRR) and another is the value I of the current source. Increasing the length of the transistor Ms can add up to the output resistance R_{out} of the bias current source, which will lead to an advance on CMRR. The minimum R_{out} is determined by setting the CMRR of the circuit to a value above 20.

The bias voltage V_{rfn} controls the amount of current supplied to the circuit.

Optimization of MCML circuits: As mentioned in section 3, the design of MCML circuits is a complex and challenging task. Every variable or parameter can influence the performance of the whole circuit. In order to get proper operation and a good performance of the MCML circuits, the limits that should be satisfied are listed in 8-19 according to the above discussions:

$$t_d = t_{required} \tag{8}$$

$$V_{DD}-\Delta V-V_{th} \le V_x \le V_{DD}-V_{th} \tag{9}$$

$$V_{DD}-V_{th1}-\Delta V \le V_y \le V_{DD}-V_{th1} \tag{10}$$

$$V_{th} \le V_n \le V_x+V_{ths} \tag{11}$$

$$\Delta V_{min} \le \Delta V \le V_{th1} \tag{12}$$

$$I = W_s v_{sat} C_{ox} (V_n-V_{ths}-A_{bulks} V_{dsats}) \tag{13}$$

$$NM \ge 0.4\ \Delta V \tag{14}$$

$$SSR \le 5 \tag{15}$$

$$CMRR \ge 20 \tag{16}$$

$$VSRl \ge 97\% \tag{17}$$

$$VSRu \ge 97\% \tag{18}$$

$$A_v \ge 1.4 \tag{19}$$

Based on the conditions listed in (8-19), the optimization procedure for near-threshold MCML circuits is illustrated in Fig. 3. In optimization procedure, the channel width of MOS transistors varies from $2\times W_{min}$ to 2 um with 65 nm step, while the channel length of MOS transistors varies from $2\times L_{min}$ to 0.65 μm by 65 nm step.

Simulations of MCML circuits: In this work, the performance and energy consumption of the static CMOS logic decimal counter is acted as a criterion. As it mentioned carlier, if the pull-down network of MCML operate in saturated region, it may result in bad performance with the scaling-down of technology dimension. We explored that whether the pull-down network can work in linear region or not. With the simulation of some basic MCML gates, the outcome is certain. All the MCML circuits mentioned below are worked with an output swing of 0.3 V.

Power dissipation of MCML circuits with a standard source voltage: In order to investigate the performance of the MCML circuits in near-threshold region, the simulation of different MCML cells in various frequencies with standard source voltage is needed. HSPICE simulations for AND2/NAND2, OR2/NOR2, XOR2/XNOR2 and decimal counter have been carried out with SMIC 130 nm technology as is shown in Fig. 4.

Form Fig. 4, the power consumptions of MCML circuits is nearly independent of frequency. It verifies that MCML circuits have a great advantage in high-speed applications. Power consumptions of the decimal counter based on MCML are compared with the decimal counter based on conventional static CMOS in Fig. 5 for various frequencies with 1.3 V standard source voltage.

Near-threshold computing of MCML circuits: In order to attain both low power dissipation and high speed, near-threshold computing for MCML circuits is addressed in this section.

The near-threshold decimal counter has been optimized in term of power dissipation and delay by using the proposed performance optimization algorithms. The circuits are simulated by varying supply voltage from 1.3 V to 0.4 V with 0.1 V step. The power dissipations of the near-threshold decimal counter using the performance optimization algorithm are shown in Fig. 6 with various supply voltages at 500 MHZ.

```
for (0.5 uA≤I≤300 uA)
{
for (ΔV= =0.3)
{
        find the smallest W1 which satisfies
2Wmin≤W1, W2≤2um
td=trequired,
NM≤0.4ΔV,
Av≤1.4,
VSRn≤0.95,
SSR< = 5.
if above is possible, record R, ΔV, W1, W2, I, Vy
}
for (2Wmin=W3=10um)
        {
        for all the values of 1, Vy obtained above
{
find the smallest W3, Vx that satisfy
Av≤1.4,
VSRl≥0.97.
if above is possible, record W3
}
}
for (700 mv≤Vrfh≤1.1V)
{
for all the values of the variables obtained above
{
find the smallest Ws, Ls, Vrfh that satisfy
2Wmin≤Ws≤10um,
2Lmin≤Ls≤5um,
Idss = I,
CMRR≥20.
}
}
}
```

Fig. 3: Optimization procedure for near-threshold MCML circuits

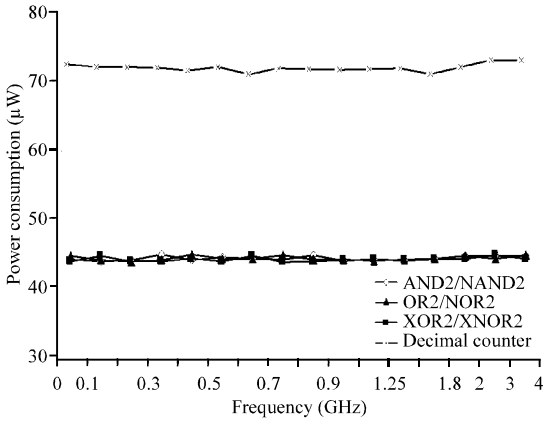

Fig. 4: Power consumptions of the AND2/NAND2, OR2/NOR2, XOR2/XNOR2 and decimal counter based on MCML in various frequencies with standard source voltage

Scaling down the supply voltage can save energy consumptions effectively. The power consumption of the

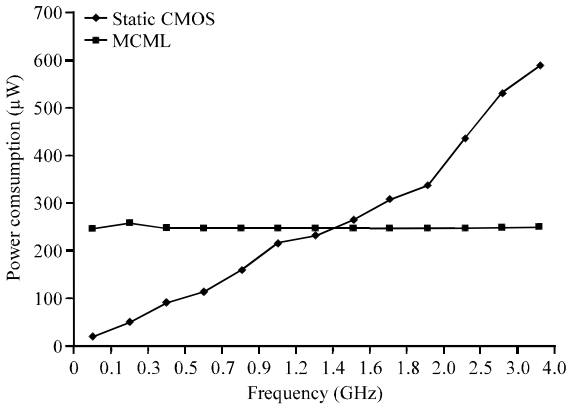

Fig. 5: Power consumption comparisons of the decimal counters based on MCML and conventional static CMOS in various frequencies with 1.3V standard source voltage

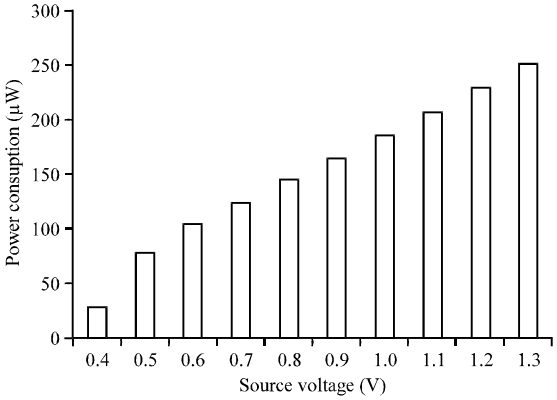

Fig. 6: Power consumptions of the decimal counter based on MCML in near-threshold regions

counter at 0.4 and 0.7V supply voltage is only 11.16 and 50.1% of 1.3V supply voltage, respectively.

In order to give a visual contrast between standard MCML and near-threshold MCML decimal counters, their power consumptions with different source voltages in various frequencies are given in Fig. 7. In Fig. 7, the decimal counter based on MCML operates from 0.4 V to 1.3 V source voltage and the working frequency is from 100 MHz to 1.4 GHz.

From Fig. 7, Power consumption reduces dramatically as the source voltage decreases, while the change of frequencies nearly have no influence in power dissipations.

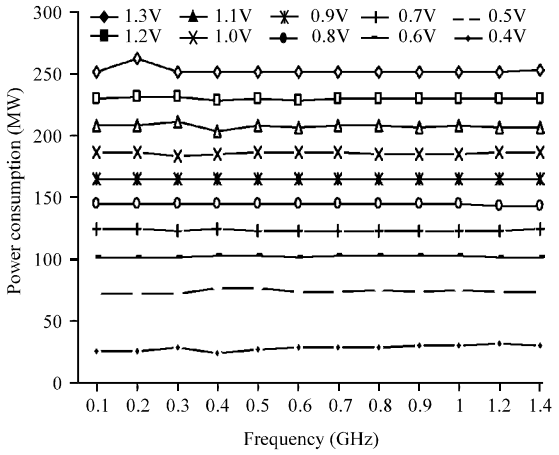

Fig. 7: Power consumptions of the MCML decimal counter with different source voltages in various frequencies

CONCLUSION

MOS Current-Mode Logic (MCML) is usually used for high-speed applications. However, the MCML circuits have large static power because of their constant operation currents. The power consumption of the MCML circuits can also be reduced by lowering the supply voltage. To the best of our knowledge, the performance optimization on near-threshold MCML circuits has not been presented. In order to attain both low power dissipation and high speed, near-threshold computing for MCML circuits has been addressed in this work. The performance optimization for near-threshold MCML circuits is also proposed.

A near-threshold decimal counter has been optimized in term of power dissipation and delay by using the proposed performance optimization algorithms. The results show that the power consumption of the optimized MCML circuits can effetely be reduced by lowering the supply voltage over a wide range of frequencies.

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