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Design of a Highly Integrated Front-End K-Band TR Module Based on LTCC Technology for Phased-Array System

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Abstract: A novel highly integrated front-end TR (Transmit-Receive) module with four RF (Radio Frequency) channels for the application of a K-Band transceiver is introduced. The housing cavity of the proposed TR module is based on the LTCC (Low Temperature Co-Fired Ceramics) technology with embedded passive RF circuit, control signal circuit and bias power supply circuit. Due to the employing of the LTCC technology, it allows to reduce the overall size and weight of the designed TR module. Furthermore, such design improves the overall performance of the TR module with a lower cost and high efficiency.

Key words: TR module, K-band transceiver, LTCC (low temperature co-fired ceramics)

INTRODUCTION

Driven by the significant worldwide demand for small-size, light-weight, high-performance and low cost satellite communication apparatus, the development of TR modules with respect to those constrains become an inevitability trend. In order to meet such demanding, new technologies have been developed, such as the Monolithic Microwave Integrated Circuit (MMIC) technologies introduced in recent published paper (Boles *et al*, 2010; Masuda *et al*., 2011). Low Temperature Co-Fired Ceramics (LTCC) technology for the using of the TR module packaging also has been proposed (Ji *et al*., 2010; Dai *et al*., 2006). The MMIC technology allows all of the passive components to be fabricated on the same substrate along with the active devices which avoids the assembly of the passive components compare with the using of hybrid circuits. It is therefore the designing of the active chipset such as Power Amplifier (PA), Low Noise Amplifier (LNA), phase shifter and amplitude attenuator utilize less area which lead to smaller size with respect to high integration density, high reliability due to the avoiding the assemble technology used by hybrid technology and low cost (Kopp *et al*., 2009; Marsh, 2006). The LTCC technology is widely used in the automotive industry which has the properties of low dielectric losses at microwave frequencies, parallel manufacturing process with high yield and low cost, adequate thermo-mechanical, good characteristics of utilizing highly conductive and inexpensive metallization etc (Devlin *et al*., 2001; Sutono *et al*., 2001; Jantunen *et al*., 2003). Base on the performance of MMIC and LTCC technologies, the proposed TR modules have utilized the advantages of both. It contains a set of active chipset which includes a GaAs Vector Modulator (VM) chip for phase shift and amplitude attenuation, a GaAs based bi-functional driver amplifier, a GaAs based PA and LNA, two GaAs based multifunctional switch and a Complementary Metal Oxide Semiconductor (CMOS) control chip. All of those chipset are mounted on the surface of a LTCC based housing cavity. Such design arrangement allows the proposed TR module has the properties of high integration which leads to smaller size, low transmission loss that results a higher efficiency. Furthermore, a high overall performance and low cost are achieved as well.

In the following the overall system design is illustrated in section 2. Section 3 details the sub-system design and simulation of the proposed LTCC housing cavity. Finally, the conclusion is given section 4.

OVERALL SYSTEM DESIGN

The overall TR module system includes a four channel LTCC housing cavity and chipset for each channel. The LTCC housing cavity utilizes with Ferro A6M multilayer substrate which has 16 layers. The purpose of choosing the Ferro A6M multilayer substrate is the tradeoff between the performance and the fabrication price. The RF signal path includes passive components such as power combiner/splitter, control signal pad and power supply pad. Each channel contains a set of chipset which consists of a VM, a bi-functional DRV, a PA for transmitting mode, a LNA for receiving mode, a Switch and antenna unit.. The block diagram of the design TR module is illustrated as following. In Fig. 1,

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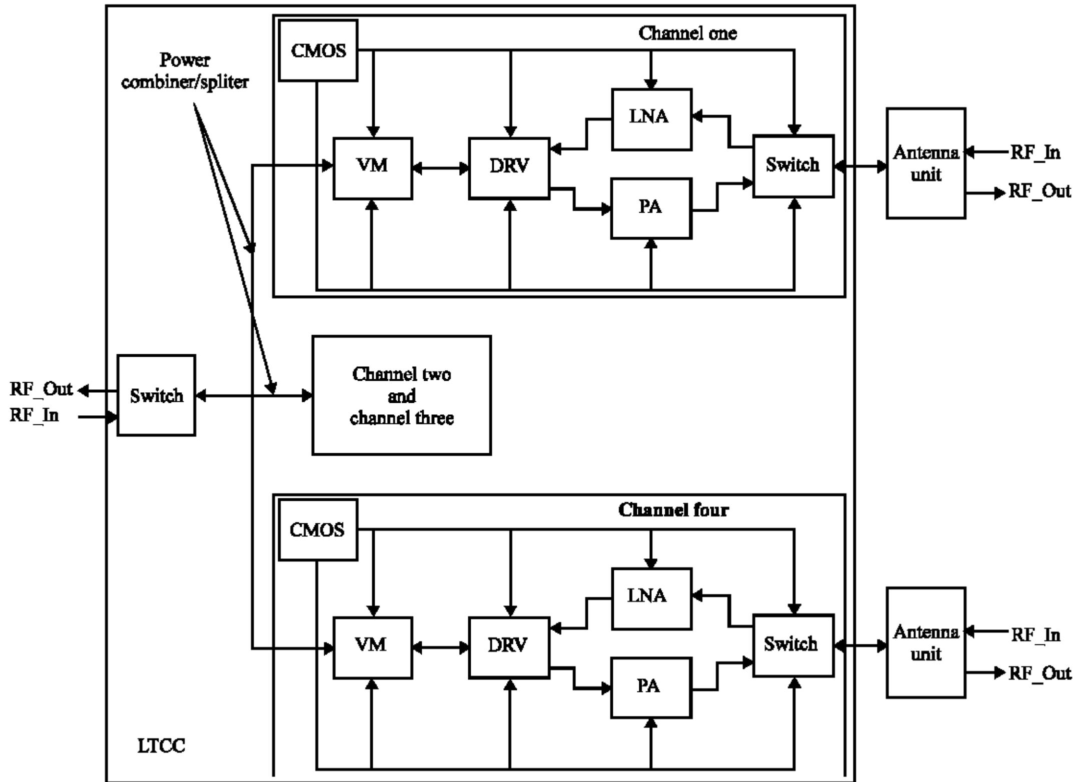

Fig. 1: Block diagram of the proposed TR module

the transmitted signal is distributes to different channels with respect to the control signals produced by the upper computer via an embedded passive power splitter. Then the signal is modulated by the VM and amplified by the bi-functional DRV and PA; and then it is delivered to the antenna unit passing through a switch. The receiving from the switch and antenna unit is amplified by the LNA and bi-functional DRV. Then the modified receiving signal is modulated by the VM and combined by the embedded power combiner. Finally the received signal is send back to the processing unit through a switch. The CMOS chip is used for controlling the GaAs switches and distributing the bias power supply to the corresponding active devices.

LTCC CAVITY LAYER DESIGN

The designed LTCC housing cavity has 16 layers which 6 layers are for bias power supply, control signal (switch signal) and RF signal. The rest of 10 layers are the ground and isolation layers. A schematic diagram of different layers for the designed LTCC cavity is illustrated in Fig. 2.

In Fig. 2, layer 1 and 3 are the gate bias for the transmitting and receiving mode, between them is an isolation layer which separates those two signal layers. The control or switching signal comes out from the CMOS chip to the active GaAs chipset is placed at layer 5. The power supply for the active chipset is set in layer 7 and 8. The RF path is placed at layer 12 which is a power combiner at receiving mode and splitter at transmitting mode. The RF layer is protected by two ground layers, layer 8 and 15 with layer 9 to 11, layer 13 to 14 as substrate fillings around the RF layer. Such design ensures that there is enough ground around the RF signal which provides a shell to cut the interference from the environment. Layer 16 is same as layer 15, which is the ground plane. It strengthens the overall TR module LTCC cavity and provides an extra safety to the ground. There do not have isolation layers between the control signal layer (layer 6) and power supply layers (layer 7 and 8) compared with the gate bias layer (layer 2 and 4). The reason is that the analogue signal for the gate bias signals are provided by the DACs of the CMOS chip, it is therefore easy to be interfered; conversely, the control signal is a digital signal provided by the CMOS

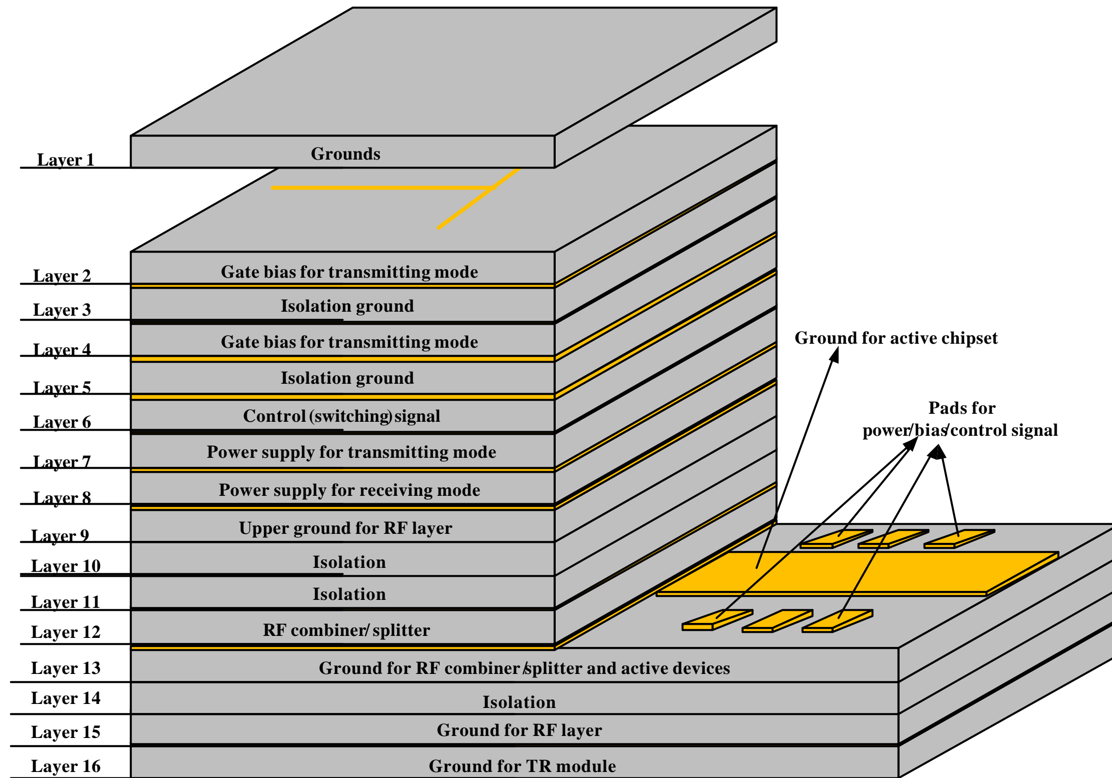

Fig. 2: Schematic diagram for the LTCC layout

and the power supply is provided the outside power supply which are hardly to be obstructed. The isolation layers (layer 10, layer 11 and layer 14) between the signal layers can be increased for better isolation with higher price. However, the proposed design is well balanced between the performance of the LTCC cavity design and the cost for fabrication. The upper RF ground (layer 9) and lower RF ground layers (layer 15 and layer 16) are designed with a net of metal line, such arrangement is to fit with the fabrication standard which only a maximum of upto 50% of the overall area can be placed with metal and also reduces the overall cost by reducing the quantity of metal to be used (normally is gold or silver). It also has the advantages of allowing the ceramic mterial can be filled into the gaps and making better contact. The details of the embedded system design and simulation are stated in the following section.

EMBEDDED SYSTEM DESIGN

As introduced in the previous section that there are total of 6 layers contains of the designed circuit. Five of them are for DC power supplies and analog control signal and one for RF signal. The design of the DC signal layers are straight forward. One thing has to be taking care of is that the viaholes from the signal layers to the corresponding pads which are on the layer 13. During the design, not only the positions have to be considered in order to avoid the DC signals leak to other isolation ground layers and RF layer, but also paths from the viaholes to the corresponding pads have to be carefully designed in order to reduce the integration area without interference with the RF signal such as the causing of self excitation within the RF channel. The RF layer is the most important part of the LTCC design due to that it directly affects the output and input RF signals. The embedded component is 1 to 4 power splitter at transmitting mode or 4:1 power combiner at receiving mode. The power combiner using a Wilkinson power combiner structure which is illustrated as below:

Wilkinson power splitter/combiner is a well know structure for such purpose in the field of RF research. It has the advantages of prefect input and output matching, high isolation and low loss (Kao *et al*., 2012). In Fig. 3, the red block represents a 50 Ω microstrip line, which is the input port for a power splitter (or the output port for

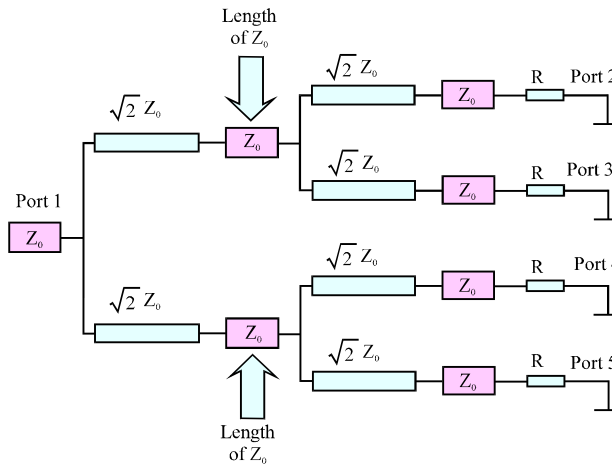

Fig. 3: Schematic design of the wilkinson power splitter/combiner

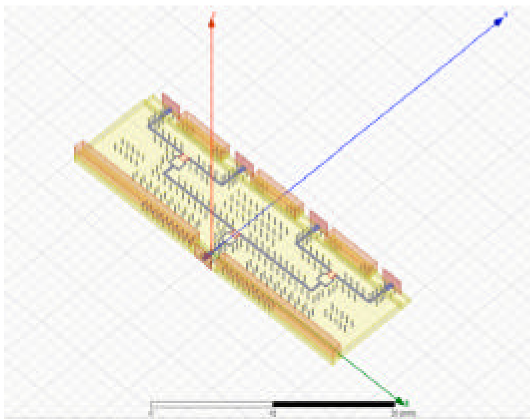

Fig. 4: 3D HFSS model for the designed power divider

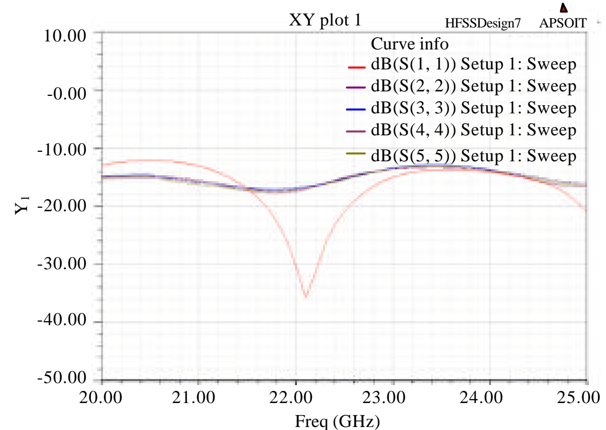

Fig. 5: Return loss of the power divider

power combiner). The left hand side of the Z_0 and right hand side of the four Z_0 are designed for the matching of 50 Ω at the port1 to port 5. The middle section of the Z_0 is the joint section between the first and section stage of the power combiner which is most troublesome part. The precision of its characteristic impedance highly affects the overall frequency response of the power divider which more attentions have to be paid during the design. The 3D simulation model in HFSS tool is illustrated in Fig. 4.

Figure 4 demonstrates the 3D HFSS model for the designed power divider. At transmitting mode, the input port is at the origin and the output ports are placed at x-y plane in the y-axis direction. The red block in the figure indicates the isolation resistor between each two branches of the power divider. The striplines are sealed by many viaholes which are connected to the ground plane. Such arrangement provides a shield for the RF signal that reduces the outside interference. The simulation of the return loss and insertion loss are shown in Fig. 5-7.

In Fig. 5, the legend shows the return loss of the corresponding port in the sequence of S11, S22, S33, S44 and S55. S11 indicates the return loss of the input port at transmitting mode. As illustrated, the return loss within the frequency band of 21.5 to 22.5 Ghz is less than 20 dB. The return loss for other ports, S22, S33, S44 and S55 are less than 15 dB which are around 3% of the total signal power transmitted.

In Fig. 6, the insertion loss between the one input port (Port 1) and the four output ports (Port 2, Port 3, Port 4 and Port 5) are shown. An approximately 7 dB loss are observed for the port pair S21, S31, S41 and S51. Compare with the ideal insertion loss of 6 dB from the structure of the divider, only 1 dB difference from it which

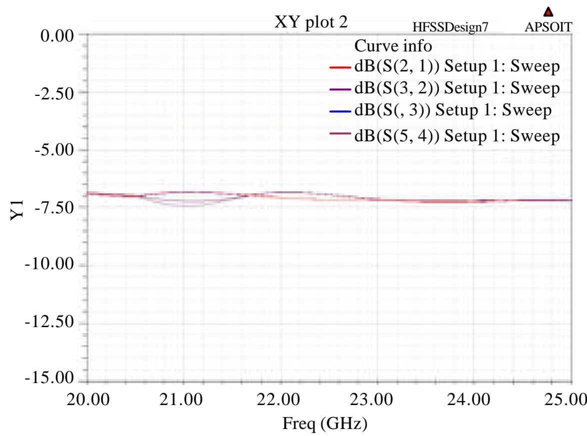

Fig. 6: Insertion loss

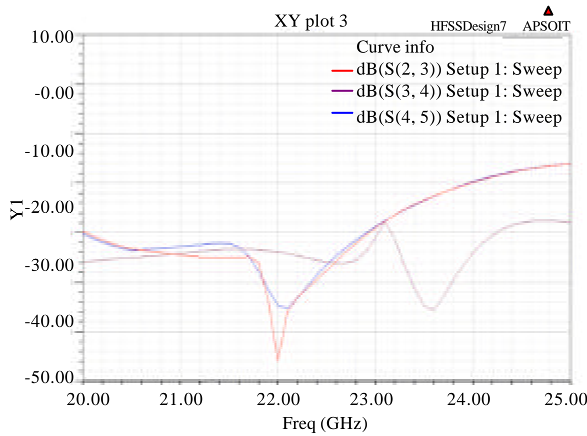

Fig. 7: Isolation between two adjacent ports

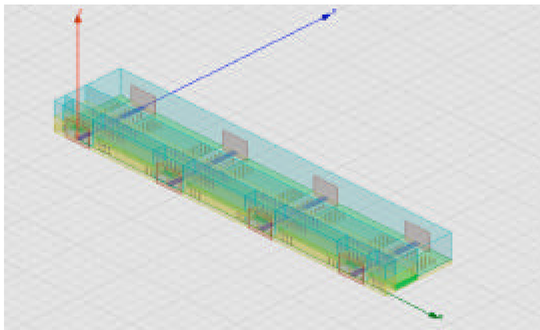

Fig. 8: 3D model of the transmission lines which connects the antenna units

is mainly affected by the tangent of dielectric loss angle. In other words, the material used in the for the LTCC housing.

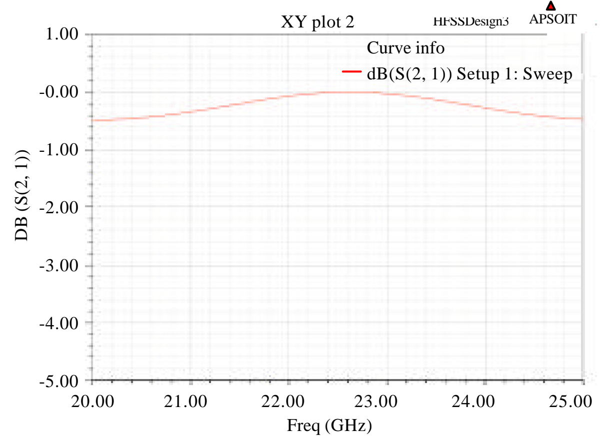

Fig. 9: Insertion loss for the transmission lines

The isolations between each two adjacent outputs are illustrated in Fig. 7. Within the designed working frequency band, the minimum isolation is around 30.2 dB which represents a less than 0.1% of power is able to leak into the neighbor port. In conclusion, the simulation results demonstrate that the design embedded power combiner/splitter is well suit for the application. The output part stripline of the LTCC is designed to connect the antenna unit to the output switch within each channel. Two factors have to be considered during the design, one is the insertion loss which has to be as small as possible; second are the return loss which has to match the output of the switch and the antenna unit perfectly to achieve a highest efficiency and best overall system performance. Its 3D HFSS simulation model is illustrated in Fig. 8.

In Fig. 8, there are four striplines are placed for four channels. One side of the transmission lines are connected to the output of the switch at the junction of transmit and receive path; the other side is connected with the antenna unit through a thin coax-cable (Channel line). For the purpose of shielding the transmitting signal, each of the transmission line is surrounded by a wall of holes which all the holes are connected with RF ground layer. The insertion loss and return loss of one of the transmission lines is shown in Fig. 9 and 10. Figure 9 illustrates that the designed strip line has an insertion loss of less than 0.2 dB within the working band. Following up, Fig. 10 shows the return loss of the transmission line is greater than 18 dB.

According to the simulation results, the designed passive RF elements within the LTCC housing cavity are well met the design requirements. The final realization of the designed TR module LTCC housing cavity is illustrated in Fig. 11.

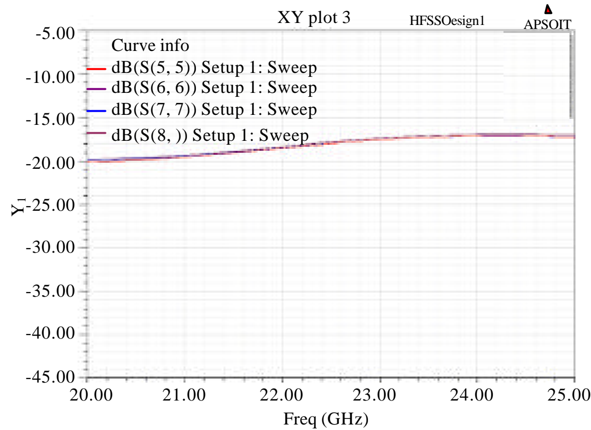

Fig. 10: Return loss for the transmission line

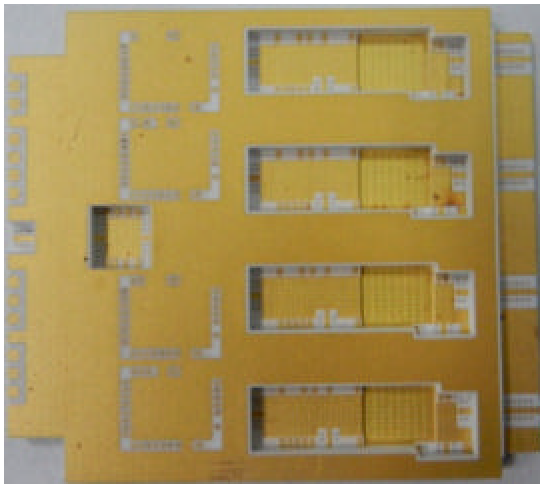

Fig. 11: Final realization of the tr module LTCC housing cavity

CONCLUSION

In this study, a highly integrated TR module for K-band phased array radar is introduced. It's LTCC based housing cavity design contains of 16 layers for the RF signal path, power supplies to the active chipset and the control signal. Extra ground layers are used for protecting the analog control signal from other interference. Through-holes connected with RF ground are used to construct a shielding wall for reducing the RF signal interference. Such arrangements allow the designed TR module has a smaller size which leads to the improving of efficiency, reducing of size, weight and cot. The simulation results of the embedded passive RF devices demonstrate that the designed well fit with the requirements. Furthermore, the future work will be the testing of the TR module with all the active chipset is assembled.

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