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A Novel Automated Testing System for a Reflection-type Vector Modulator

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Abstract: In this study, an automated testing system for a reflection-type Vector Modulators (VM) comprised of a Field Programmable Gate Array (FPGA) and a LabVIEW based testing software is presented. The testing system with a friendly Graphic User Interface (GUI) is able to evaluate all the functionality of the VMs and allows the user to test the FPGA module step-by-step or to automate the testing in a sequential way. In case of multiple VM testing, all the VMs can be tested in one time by automatically sending the control commands to manipulate the bias voltage of each VM. Only one FPGA based hardware is needed in the testing system for the bias voltage control. This present testing system is highly efficient for VM testing and can be easily generalized to the testing of other VMs.

Key words: Automated testing system, vector modulator, field programmable gate array, LabVIEW, graphic user interface

INTRODUCTION

Vector Modulator (VM) is a device used for the amplitude and phase modulating of the input signal. Many kinds of VMs have been developed in the past decades for the applications in communication systems and other microwave systems such as phased array radars (Hou *et al.*, 2008; Penn, 2005; Huang and Caron, 2009; Tosovsky and Valuch, 2010). In order to evaluate the performance of VMs, fully testing under all the possible condition is inevitable which includes the temperature performance as well. This requires huge data volume and thus an automated system is needed for the testing in order to improve the testing efficiency. A few testing system has been proposed by the researcher in the past. At the beginning of the spectrum, a complex testing system has been illustrated by Penn *et al.* (2006), the overall system consists of many equipments apart from the network analyzer, such as two function generators, a dual-trace scope. Later, Lux *et al.* (2009), the authors have introduced a simple automated testing system, in which a PC controlled DACs is used for the power supply of the VM and a LabVIEW based software is designed to control a network analyzer for measuring the RF signal of the VM. However, in both kinds of testing systems, the states of the VM, corresponding to specific bias voltages can only be tested one at a time which leads to a very low testing efficiency. Thus, when the states of a large scale of VMs need to be assigned, e.g., a 20000-channel phase-array radar aperture, the testing process is usually quite time consuming. In this

study, in order to increase the testing efficiency of VMs, a new automated testing system is designed with low cost, high accuracy and flexibility which contributes a reference design for potential researchers in this area due to the lack of articles in the area of testing system for VM testing and evaluation.

For the demonstration of our testing system, a set of reflection-type VMs is used as the sample. The block diagram of one reflection-type VM is illustrated in Fig. 1. The VM consists of three Lange couplers, a power combiner and two set of GaAs pMENT FETs acting as changeable loads when the two bias voltages applied are tuned. By tuning the two bias voltages, the reflection coefficient of the VM is changed accordingly which leads to different RF power reflected back to the output of the VM.

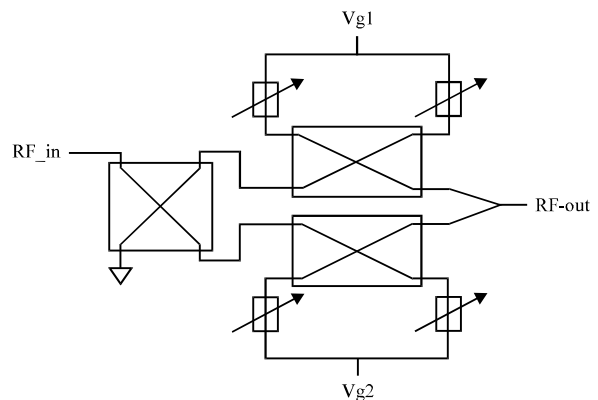


Fig. 1: Block diagram for the reflection-type VM

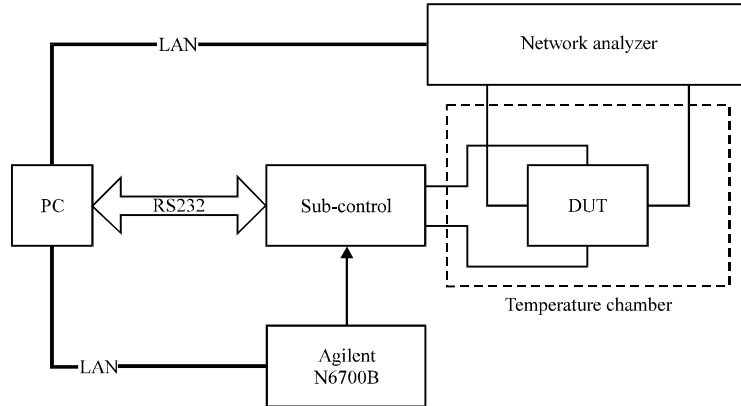


Fig. 2: Block diagram of the overall testing system

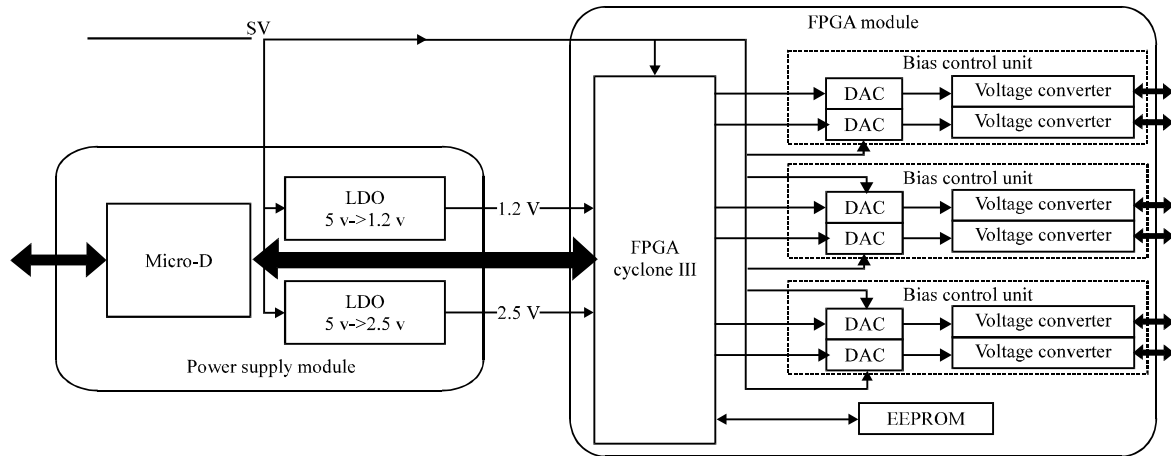


Fig. 3: Block diagram of the sub-control system

The overall testing system comprises of a desktop where the LabVIEW automated testing software is running, a FPGA based sub-control board which acts as the sub-computer between the VM under test and the testing software, an R and S network analyzer for performing the measurement and an Agilent N6700B programmable power supply. The temperature chamber introduced in the system is an optional device for further testing of temperature stability. The block diagram of the system connection is shown in Fig. 2.

FPGA BASED SUB-CONTROL SYSTEM DESIGN

FPGA based research has a wide applications such as the developments of ADC (Guo *et al.*, 2005), signal processing in (Wu *et al.*, 2009; Jevtic and Carreras, 2012; Jiao and Hong, 2013), motion estimation (Vasiljevic and Ye, 2012) and communication system (Ding *et al.*, 2013), so on. It has the advantages of fast processing, flexibility

for configuration which is ideal for a small system control. The proposed FPGA based sub-control system consists of two modules, the power supply module and the FPGA module. The block diagram of the sub-control system is illustrated in Fig. 3.

The power supply module has a self-modified 9-pin Micro-D connector which communicates with an Agilent N6705B power supply. Two LDO voltage converters are used to convert the 5V input voltage to 1.2V and 2.5V. All the three voltages are used to supply the FPGA module. The FPGA module, as the main control unit, consists of a set of bias control units, a FPGA chip and an EEPROM. Each bias control unit follows the command from the FPGA chip and outputs the two corresponding voltages, V_{g1} and V_{g2} , to one VM. With the help of the Digital Analogue Converters (DAC), both output voltages range from -2 to 0V with a minimum step-size of 0.5 mV. The EEPROM is used for storing the calibration data in an automated testing scenario. The FPGA is programmed to

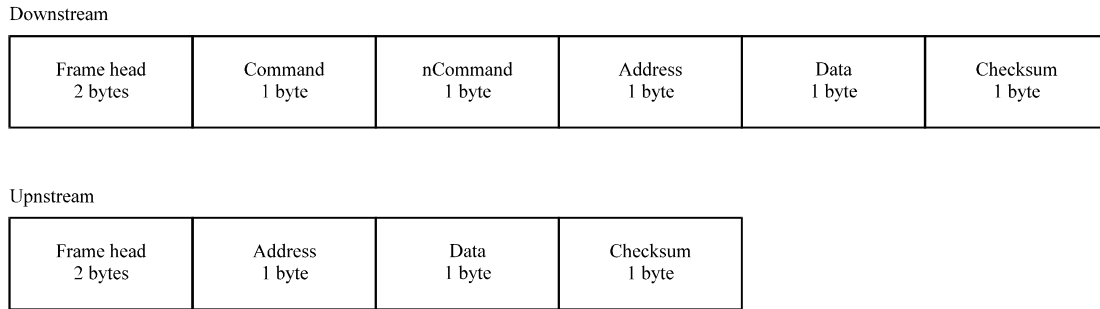


Fig. 4: UART frame structure

Table 1: UART command format

Command name	Command	nCommand	Description
Write register	0x01	0xfe	Write register, no return
Read register	0x02	0xfd	Read register, data return

control the voltage distribution of all the connected VMs, reading data from the EEPROM and translate the stored information to corresponding voltages for the VMs and communicate with PC through a Universal Asynchronous Receiver/Transmitter (UART) chip. The UART frame structure is defined as shown in Fig. 4.

In Fig. 4, the nCommand in the downstream is for the verification of the 1 byte command. And the Checksum in both downstream and upstream is for checking the summation of the whole UART command line. The UART command format is defined in Table 1.

LabVIEW BASED AUTOMATED TESTING SYSTEM

LabVIEW is a software language introduced by the National Instrument (NI) which consists of abundant instrument drivers and friendly Graphic User Interface (GUI) and is highly efficient for programming in the field of instrument control (Wang *et al.*, 2013a; Meng *et al.*, 2013; Wang *et al.*, 2013b). The GUI of the designed LabVIEW automated testing software comprises of seven blocks which is illustrated in Fig. 5 and detailed as following.

In Fig. 5, the general setting block is for COM interface setup between the desktop and FPGA sub-control system and reads the FPGA version used by the testing system. The “single register testing” block allows the testing of the registers of the FPGA one-by-one. The RF “setting and testing” block is for the automated testing setup of VMs. On the left of the block, it consists of the IP address of the network analyzer, file path of the calibration and the testing data and the Agilent N6700B’s IP address. The right side of the block is for defining the voltages ranges and step-size

for the power supply of the VMs. It also contains a start button and an indicator of the testing progress.

The “EEPROM testing block” allows the status checking of the EEPROM block-by-block. Alternatively, the EEPROM can be tested by the “EEPROM auto-testing block”. The phase and attenuation block allows the user to input the desired phase and attenuation information to the FPGA, then the FPGA translates the information into corresponding voltage values and provides to the VMs. By measuring the magnitude and phase of the RF output, the performance of the VMs can be evaluated step-by-step, especially at the debugging stage. Finally, the automated evaluation of the phase and attenuation of the VMs can be done by the last block, phase and attenuation (Auto) block.

TESTING DEMONSTRATION

At the first instance, the output voltage of the sub-control system is evaluated for both voltages, Vg1 and Vg2 during which a PXI measurement system from national instruments is used. It contains a Peripheral Component Interface (PCI), a PCI express module, a PXIe 6363 DAQ module and a PXIe 4140 Surface Measure Unites (SMU). The automated testing is conducted by sending the corresponding command to the FPGA sub-control system, then measuring the output of the two DAC values from the FPGA sub-control system and comparing it to the ideal value to evaluate the voltage output from the DACs through PXI. The photo of the PXI measurement system is shown in Fig. 6.

The measured output of DAC for the power supply of Vg1 and Vg2 are illustrated in Fig. 7-10.

In Fig. 7, the desired voltage range for the each VM is within the range from -1.7 to -0.4 V, thus the saturated sections at both ends of the curve, at the level of -1.95 and -0.1 V, will not affect.

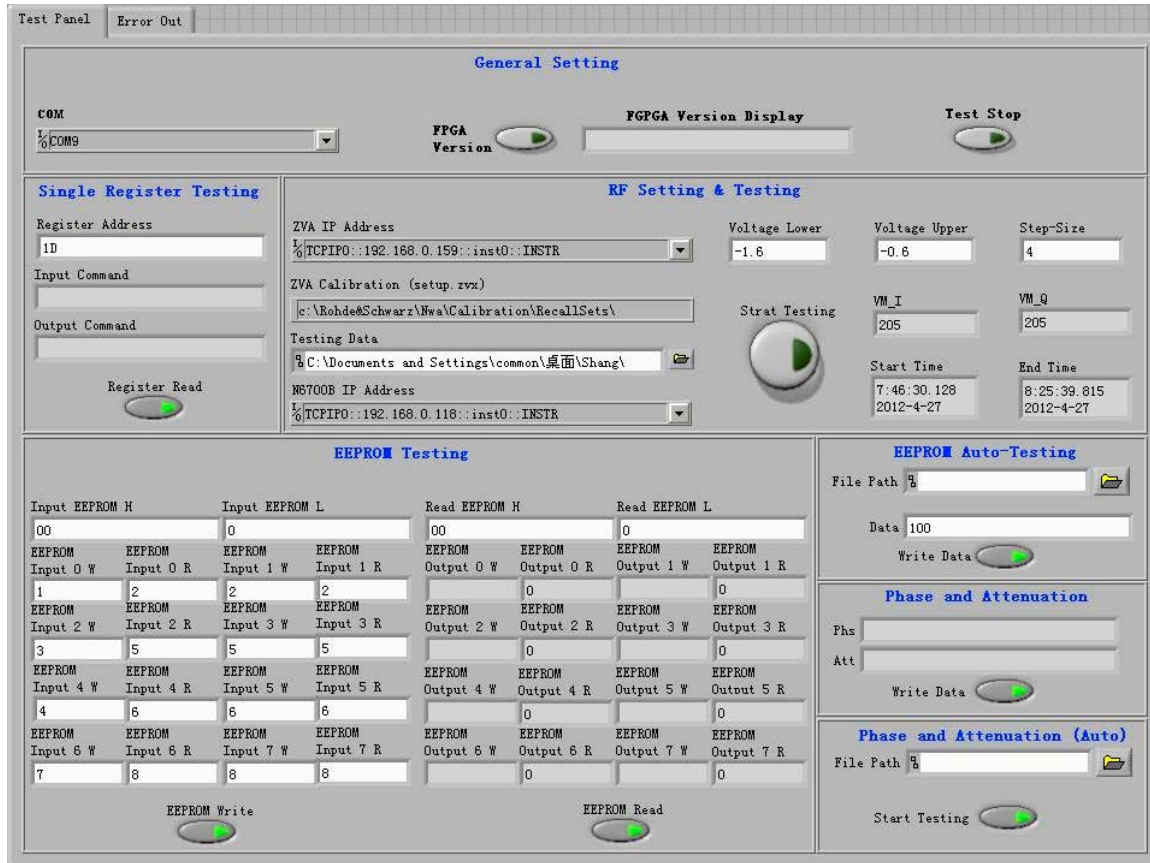


Fig. 5: GUI of the automated testing software



Fig. 6: PXI measurement system

The errors deviate from the ideal voltages for Vg1 is shown in Fig. 8. Within the voltage range from

-1.7 to -0.4 V, the slope of the deviation is linearly growing and the maximum deviation is around 0.07 V.

The corresponding testing results for Vg2 are illustrated in Fig. 9 and 10. Comparing with the testing results of Vg1, the voltage deviation is smaller but contains more distinctive discontinuous cause by cumulative error, thus has lower linearity.

After evaluating the sub-control system, we finally measure the RF response of the each VM. The measured constellation maps of the one VM using the proposed automated testing system are illustrated in Fig. 11. Each point indicates the magnitude and phase of the output RF signal of the VM working at specific Vg1 and Vg2. The left constellation map is tested with a testing fixture and the right constellation map is tested with a probe station. Comparing these two constellation maps, a rotation offset exists which represents a phase offset. This is caused by the difference of the phase offset between the testing fixture and the probe station. The few jitters in both

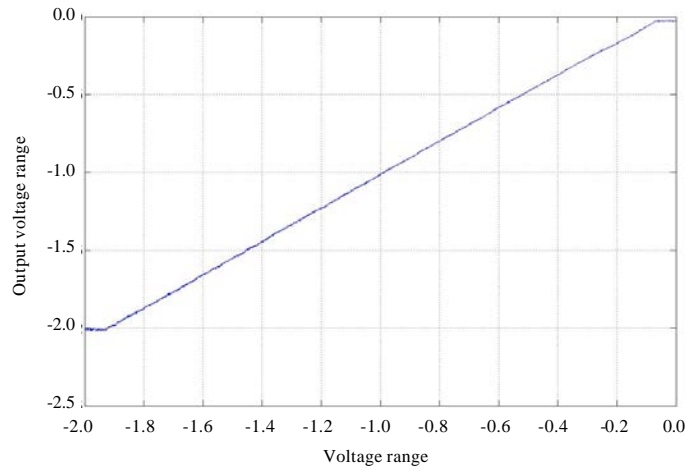


Fig. 7: Output voltage value from the sub-control system (Vg1)

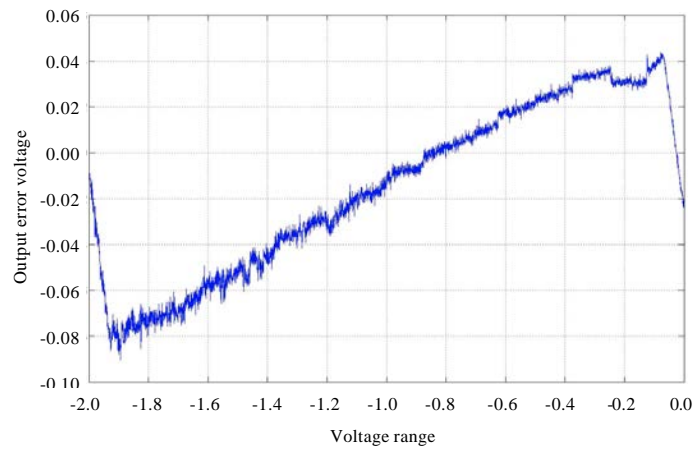


Fig. 8: Error voltage with respect to ideal voltage value (Vg1)

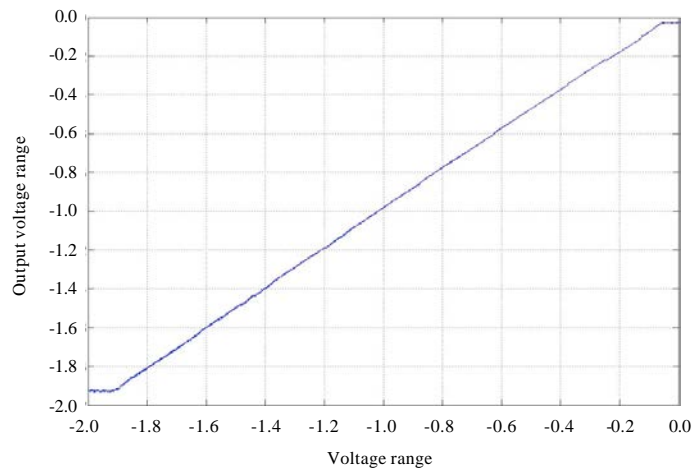


Fig. 9: Output voltage value from the sub-control system (Vg2)

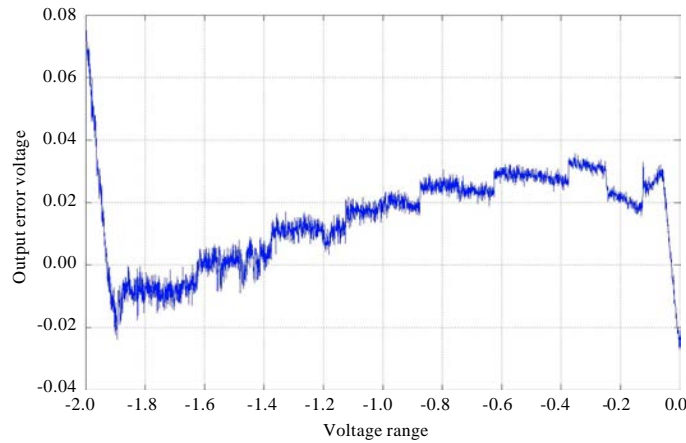


Fig. 10: Error voltage with respect to ideal voltage value (Vg2)

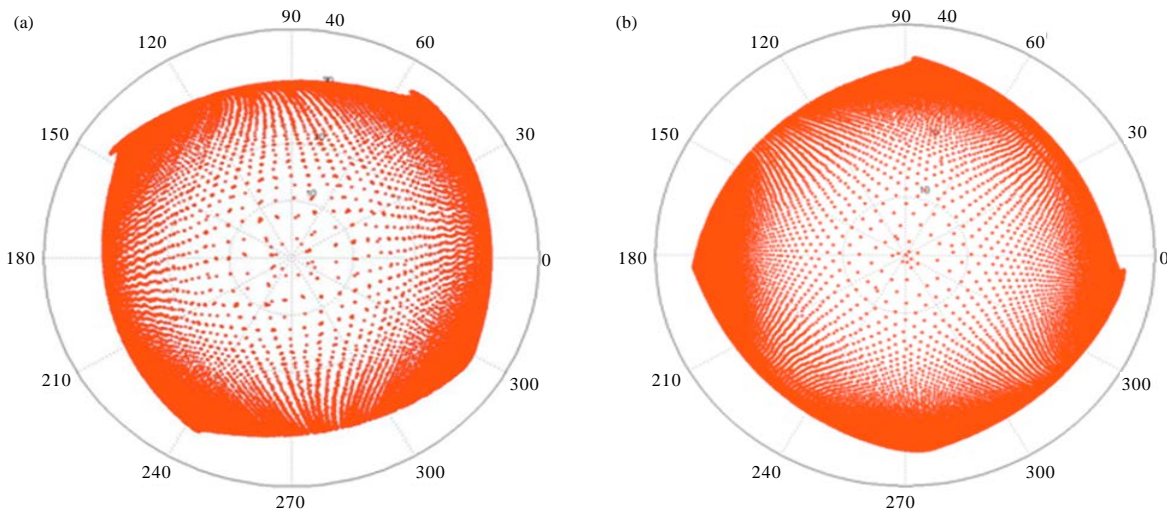


Fig. 11: Constellation map of one vm tested with a step-size of 2.5 mV

constellation maps are caused by the voltage variations of the DACs. From Fig. 11, we can see the distributions of the two data patterns match well, thus both testing scenarios are suitable for the extraction of the calibration data.

CONCLUSION

A novel testing system based on FPGA and LabVIEW is presented for the application of testing a reflection-type vector modulator. The sub-control hardware design using FPGA is detailed for communicating with the testing PC and providing the bias voltage to the VM under test. It allows the testing

engineer evaluates the VM step-by-step or automatically in a sequence. It also provides the final performance assessment of the VM after the calibration data is obtained and stored in the EEPROM. With respect to the LabVIEW based automated testing software, it offers the testing engineer tests all the modules of the sub-control system and sends the control commands to manipulate the bias voltage of the VM. The testing results have demonstrated that the proposed system is able to offer a high efficiency with that several VMs can be tested in one time; high flexibility which allows the user communicates with the sub-control system through a GUI interface and low cost with only a FPGA based hardware is needed for the design.

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