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A Highly Reliable SEU Hardened Shift Register

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ABSTRACT
This study presents a design of a highly reliable shift register based on TSMC 0.18 μm process which can efficiently fight against the Single Event Upset (SEU). A bilateral Power on Reset (POR) block, together with bit-line segregation and tri-mode redundancy technologies are applied in this design to comprehensively enhance the SEU hardening performance at both system level and circuit level. Assisted by the theory of transient circuit analysis, the shift register's SEU hardening performance is achieved from the aspects of both schematic and layout. A current pulse which is used to emulate the SEU effect, is injected in the circuit for verification. The result of simulation shows great improvement of the SEU tolerance. With its high reliability and radiation tolerance, the present shift register can be applied to CMOS chip designs in the field of aerospace.

Key words: Single event upset, bilateral power on reset, bit-line segregation, tri-mode redundancy, radiation tolerance

INTRODUCTION

Due to CMOS process's size shrinking, clock frequency increasing and supply voltage reducing, the stored charge in CMOS circuits which represents logical "high", keeps decreasing, However, the deposit charges induced by the high-energy particle bombardment remain unchanged. This makes the threatening of SEU phenomenon to the CMOS memory block become much more serious than before (Wissel *et al*., 2009; Narasimham *et al*., 2009; Maru *et al*., 2010). Therefore, the SEU-hardening of CMOS circuit at the deep submicron integrated level is of great importance.

Among all the digital blocks in the CMOS integrated circuit, the shift register is most widely applied which however is very fragile to the space radiation. The impact high energy particle will upset the information stored in the register. This wrong information will be kept in the register until new data is refreshed to the block. In recent years, in order to obtain the SEU-hardened design of registers, researchers have come up with many solutions at system and circuit level, like Tri-Mode Redundancy (TMR), error correction coding (Hentschke *et al*., 2002), Heavy Ion Tolerance unit (HIT) (Bessot and Velazco, 1993), dual interlock storage unit (DICE) (Calin *et al*., 1996) and so on. However, these analyses neglect the instability of the reset signal. In practical application, power on reset (POR) circuit can also be easily affected by the space radiation. The memory block will lose information due to the abnormal resetting signal which degrades the circuit performance seriously.

In this study, in order to comprehensively enhance the SEU hardening performance of CMOS circuit, we propose a highly reliable shift register design using bilateral resetting, bit-line segregation and tri-mode redundancy technologies. Based on TSMC 0.18 μm process, combining the theory of transient circuit analysis, the performance of the SEU-hardened shift register is elaborated from aspects of both schematic and layout. A current pulse source is added in the circuit in order to emulate the SEU effect. Simulation using Cadence Spectre is conducted for verification.

MATERIALS AND METHODS

Traditional shift register with POR: Traditional shift register's circuit structure diagram with POR is shown in Fig. 1. In order to prevent the unstable state happened in the power up process, a POR circuit producing a low voltage reset signal is needed to initialize the register. When the power supply voltage reaches the desired value, the reset signal changes from low to high which makes the register begin to work.

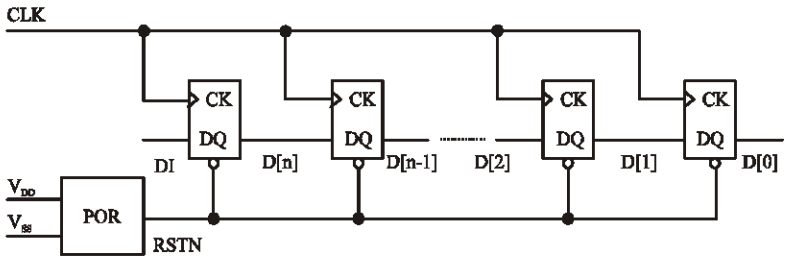

Fig. 1: Diagram of traditional shift register's circuit structure

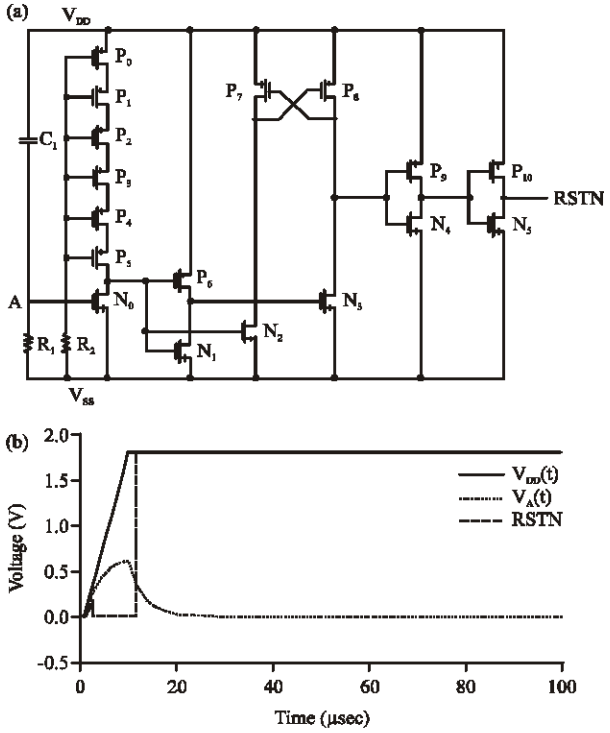

Fig. 2(a-b): (a) Traditional POR structure and (b) Voltage change of traditional POR during power up

To reinforce the register's SEU hardness, a bilateral resetting POR structure is proposed in this study. Meanwhile, the shift register's flip-flop cell is modified to SEU hardened DICE structure in order to obtain self-recovering ability.

SEU hardened POR structure: The structure of the traditional POR circuit is shown in Fig. 2a. When powering up, POR generates a resetting signal to initialize the shift register which ensures the circuit to start up correctly. During this period, because the changing rate of the supply voltage V_{DD} is much larger than capacitor C_1's time constant R_1C_1, the voltage of node A (V_A) will increase with the supply voltage. If V_A reaches a high enough voltage to turn on transistor N_0, the circuit outputs a low voltage resetting signal RSTN. After the supply voltage reaches the system's desired voltage V_{DD0}, the capacitor C_1 charges with the time constant R_1C_1 and V_A starts dropping. When V_A drops below the threshold voltage, transistor N_0 turns off and the POR circuit outputs a high voltage signal. Thereafter, the shift register enters working state.

During power up process, the charge, voltage and current change on capacitor C_1 satisfies the following relations:

$$\begin{cases} Q(t) = C_1 \cdot \left[V_{DD}(t) - V_A(t) \right] \\ V_A(t) = I(t) \cdot R_1 \\ dQ(t)/dt = -I(t) \end{cases} \quad (1)$$

where, Q(t) denotes the accumulated charge, I(t) denotes the current through R_1. Supposing $V_{DD}(t)$ increases linearly from t = 0 and settled at the desired voltage at $t = t_0$, we obtain the expression of $V_A(t)$ as:

$$V_A(t) = \begin{cases} (V_{DD0}/t_0) \cdot R_1C_1(1 - e^{-t/R_1C_1}) & t < t_0 \\ V_{A0} \cdot e^{-(t-t_0)/R_1C_1} & t > t_0 \end{cases} \quad (2)$$

where, V_{A0} denotes the voltage of node A at time t_0.

During the above power up process, $V_{DD}(t)$, $V_A(t)$ and RSTN change as shown in Fig. 2b. Without losing any generality, in this study, the supply voltage is set to be 1.8 V. In order to save simulating time, t_0 is reduced from general 1 msec to 9 μsec.

In the environment with space radiation, traditional POR circuits will be easily upset by the impact particles which results in the shift register's abnormal resetting and the lost of stored information. Therefore, in this study, a highly reliable shift register based on bilateral resetting POR circuit is proposed, as shown in Fig. 3a. Transistor N_0~N_5 and P_0~P_5 are formed by long channel MOSFETs which behave as very large resistors but possessing relatively small area. During powering up, V_A goes up with the supply voltage. While, V_B remains at low voltage and transistor P_6 and N_8 turn on. Therefore, POR circuit generates a low-voltage RSTN signal. When the supply voltage reaches the desired value, capacitor C_1 charges with a fixed time constant. As a result, V_A keeps decreasing. As V_A lowers down to a particular value, transistor P_0~P_5 turn on and capacitor C_2 charges. At last, V_A becomes low voltage and V_B becomes high voltage. Transistor N_6 and N_7 turn on and the circuit produces a high-voltage RSTN signal. The shift register then turns into normal working state. During the above powering up process, the $V_{DD}(t)$, $V_A(t)$, $V_B(t)$ and RSTN change as shown in Fig. 3b.

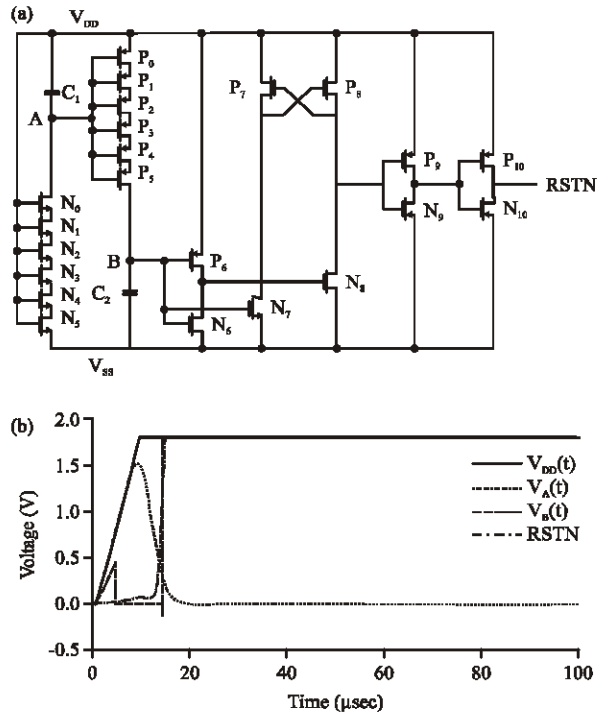

Fig. 3(a-b): (a) SEU hardened bilateral resetting POR circuit structure and (b) Voltages change during powering up process

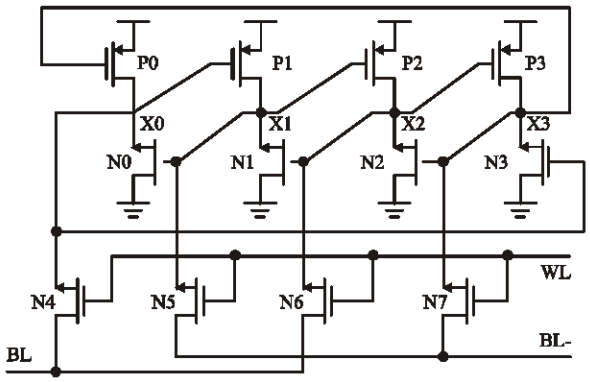

Fig. 4: Schematic of the DICE circuit structure

For traditional POR circuit structure, as shown in Fig. 2a, when node A is bombarded by a high energy particle, the transient current at this node will increase apparently. Therefore, V_A goes high and turns on N_0 which leads to an unexpected resetting signal. For bilateral resetting POR circuit structure, as shown in Fig. 3a, when node A is bombarded by a high energy particle, transistors P_0~P_5 will turn off. Thus, the wrong signal won't transfer to the output. While, if node B is bombarded by a high energy particle, the output logic reverses and the circuit generates a wrong resetting signal. Comparing node A in traditional POR circuit with node B in our bilateral resetting POR circuit, due to the fact that C_1 in Fig. 2 is generally 10 times larger than C_2 in Fig. 3 which indicates that the radiation-sensitive layout area of node A is 10 times larger than that of node B, the probability of being bombarded of node B is 1-order less than that of node A. As a result, the proposed bilateral resetting POR circuit structure is more radiation tolerant than the conventional counterparts under cosmos environment.

SEU hardened DICE circuit design: The mechanism of traditional DICE circuits is to store and backup data within four redundant sub-circuits. The schematic of the DICE circuit structure is shown in Fig. 4. When the information stored in one single node is upset by a bombarding particle, the back-up data stored in the other three nodes will restore the incorrect information through feedback. As shown in Fig. 4, the four transistors, (N_0, P_1), (N_2, P_3), (N_1, P_2) and (N_3, P_0), form two pairs of cross-coupled reverse-phase latches. The input data (logic "1" or logic "0") will be transferred to two complementary data (1010 or 0101) which are stored in node X_0~X_3, respectively. Each of the four nodes is controlled by its two adjacent nodes and there is no dependency between the two adjacent nodes. When the input is logical "0" (X_0~X_3 = 0101), inverter (N_0, P_1) and (N_2, P_3) form a loop to latch steadily. Same data is stored in node X_0, X_1 and node X_2, X_3, respectively. While the other two inverters, (N_1, P_2) and (N_3, P_0), turn off and segregate the above two latches. Similar for the case the input is logical "1" (X_0~X_3 = 1010), the inverter (N_1, P_2) and (N_3, P_0) turn on and the other two turn off.

Under the radiation circumstance, assuming one node of the DICE circuit, X_i which stored logical "0", is bombarded by a particle, a positive current pulse will be generated in this node. This current pulse will generate a negative disturbing pulse in node X_{i-1} through transistor N_{i-1}. However, the positive upsetting signal in node X_i is blocked by transistor P_{i+1} and will not affect node X_{i+1}. Meanwhile, the negative upsetting signal in node X_{i-1} will not transfer through transistor N_{i+2} thus will not affect node X_{i+2}, Therefore, node X_{i+1} and X_{i+2} are protected from the particle bombardment. When the bombardment passes over, the unaffected nodes of X_{i+1} and X_{i+2} will force node X_i and X_{i-1} going back to normal through the feedback of N_i and P_{i-1}. Therefore, the bombardment will only cause a temporary disturbance which will vanish through self-feedback. As for a negative disturbing pulse, it can be analyzed in the same way.

However, although the radiation-induced disturbance of the DICE output is limited in a short time period, when the output terminal is connected to a combinatory logical circuit, the disturbance may lead to wrong logical result. Besides, in traditional DICE layout designs, the input nodes with the same logical state are commonly linked together in order to save the layout area. In this case, if one of the input nodes is disturbed by particle bombardment, the two nodes connected with this node will also turn upset, thus cannot be restored through feedback. In order to solve above problems, in this study, the DICE circuit of the proposed register is hardened at both system and circuit level, shown in Fig. 5. Bit-line segregation and tri-mode redundancy techniques are applied at the input and output of the circuit, respectively. Furthermore, clock redundancy is added.

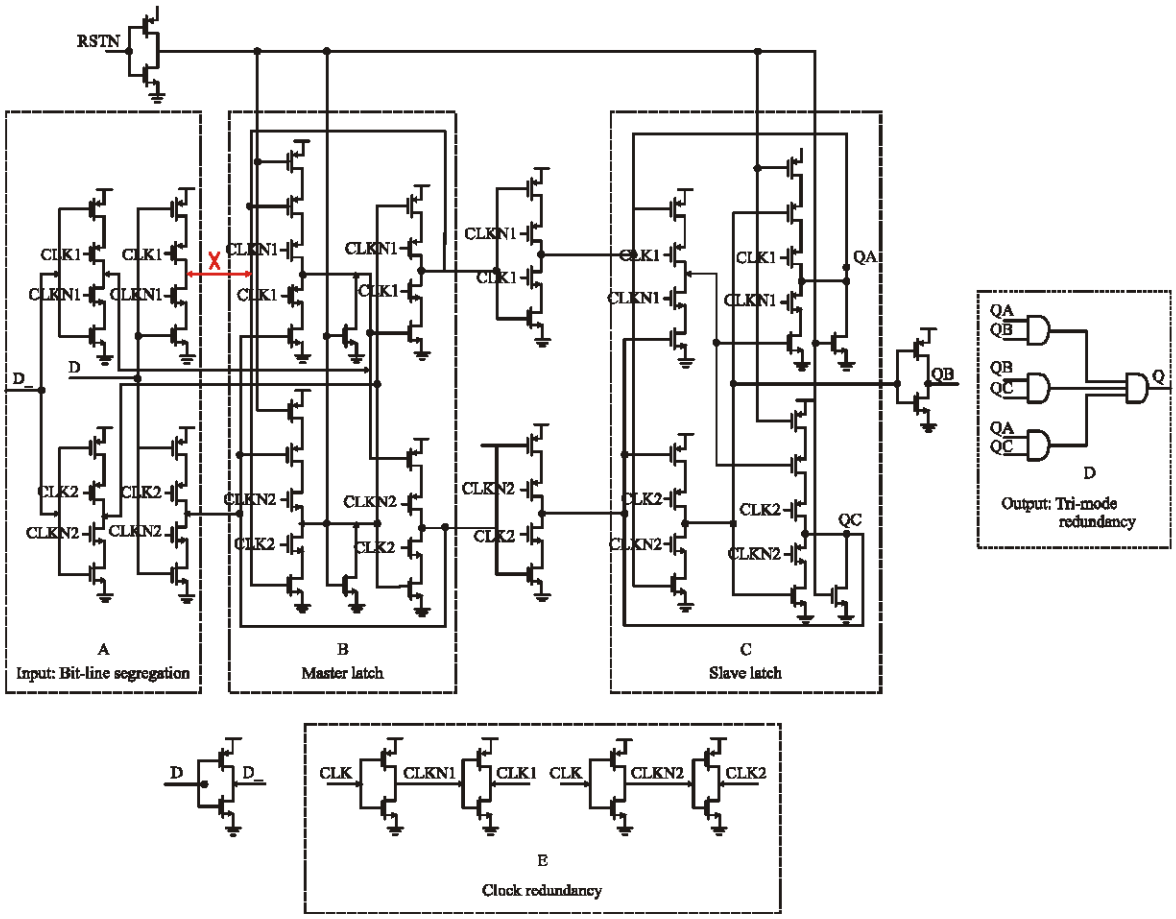

Fig. 5: Schematic of SEU hardened DICE circuit

As shown in part A of Fig. 5, bit-line segregation technology is applied to isolate the 4 input signal wires. In part D, tri-mode redundancy technique is applied by picking three output nodes from the slave latch. If one of the output data turns to a wrong logical state, this structure ensures the final output remaining correct. Only in the case when two of the output data turns to wrong state, the final output of the register will upset. Considering that the probability to have two nodes being bombarded simultaneously is quite low, no further discussion about this case is introduced in this study.

The circuit of clock redundancy is realized as shown in part E of Fig. 5. The clock signal is generated by two identical invertors which are independent from each other. When one of the inverters turns upset due to the particle bombardment, the other inverter can still work as normal which guarantees the validity of the generated clock signal.

Compared with the traditional DICE structure, the circuit proposed in this study introduces the SEU hardened circuit structures in three parts-clock generation circuit, input circuit and output circuit. The entire performance is apparently improved.

RESULTS

Based on TSMC 0.18 μm process, the SEU hardening performance of the proposed POR circuit and the entire shift register were simulated using Cadence Spectre. Current pulse was injected in the radiation-sensitive nodes to emulate the particle bombardment effect.

Supposed the depth of the injected particle into the circuit board is 1 μm and assumed that the incident particle vertically impacts the circuit board. The bi-exponential current source model was applied to emulate the bombardment. The damage caused by the particle can be estimated by Linear Energy Transfer (LET). The expression of the current source was shown in Eq. 3:

$$I(t) = f(LET)(e^{-1/t\alpha} - e^{-1/t\beta}) \quad (3)$$

where, f(LET) is a linear function of LET, $t_{\hat{a}}$ denotes the time constant of charge collection, $t_{\hat{a}}$ denotes the time constant of settling the trace of the charge. We assumed t_{α} = 200 ps and t_{β} = 50 ps. Considering the extremely low probability of encountering a particle with LET larger than 100 MeV•cm^2/mg

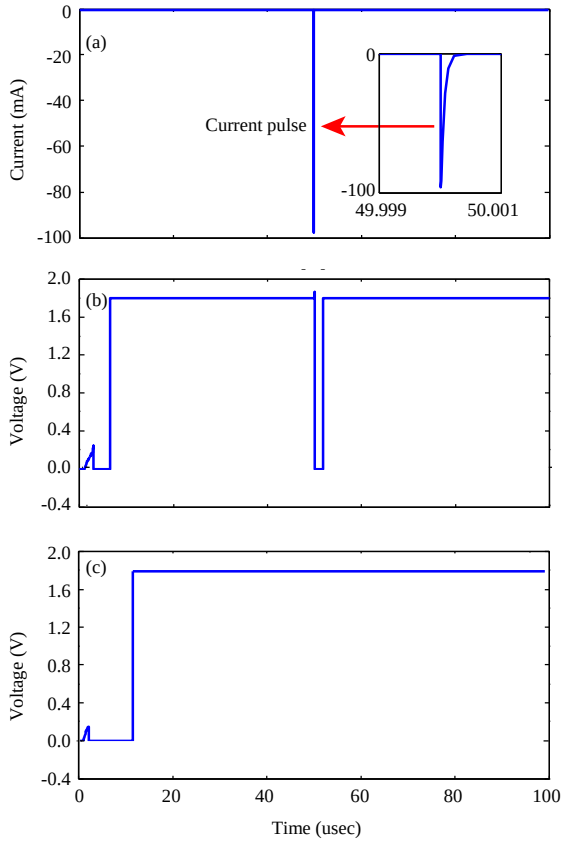

Fig. 6(a-c): Performance of POR circuit, when LET = 100 MeV•cm^2/mg, (a) Current pulse used to emulate the particle bombardment, (b) Output RSTN signal of traditional POR circuits and (c) Output RSTN signal of the proposed bilateral resetting POR circuit

in the environment with space radiation, it w as convincible to conclude that the device, whose upsetting threshold is larger than 100 MeV•cm^2/mg, has excellent SEU hardening performance.

When there was no current pulse injecting, simulation results of the traditional and bilateral POR circuits were shown in Fig. 2b and 3b. After the supply voltage was settled, a current pulse which emulates a 100 MeV•cm^2/mg single particle bombardment, was injected in a sensitive node A (Fig. 2a and 3a), shown in Fig. 6a. The simulation result was shown in Fig. 6. Same as we discussed above, under this condition, the traditional POR was upset and generated a low resetting signal which further reset the entire shift register incorrectly. The simulation result was shown in Fig. 6b. While, the proposed bilateral resetting POR circuit was immune to this disturbance. The output maintained logical "1" during the particle bombardment which showed better SEU-hardening performance. The simulation result was shown in Fig. 6c.

As an example, the layout of the proposed bilateral resetting POR circuit was designed based on TSMC 0.18 μm CMOS process, as shown in Fig. 7. The area inside the white dashed line was the SEU sensitive area of the SEU-hardened POR circuit. Compared with the traditional one, the sensitive area was 10 times smaller.

In order to verify the SEU hardening performance of the designed DICE circuit, a current pulse which represents a 100 MeV•cm^2/mg particle bombardment was injected in node X (Fig. 5), when the master latch (Fig. 5, part B) was in hold state and the slave latch (Fig. 5, part C) was in sampling state. The clock signal and the input signal were shown in Fig. 8a and b. Same as the above analysis, we saw that the traditional DICE circuit can restore to the correct state through self-feedback, there always existed a time delay during the restoration. Thus, the output state experienced a transient upset during the bombardment. The simulation result was shown in

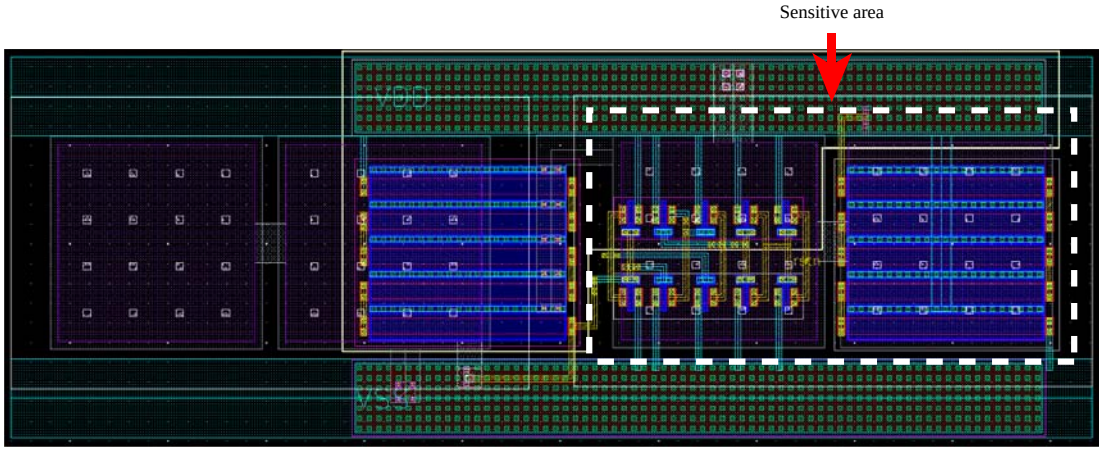

Fig. 7: Layout of the bilateral resetting POR circuit

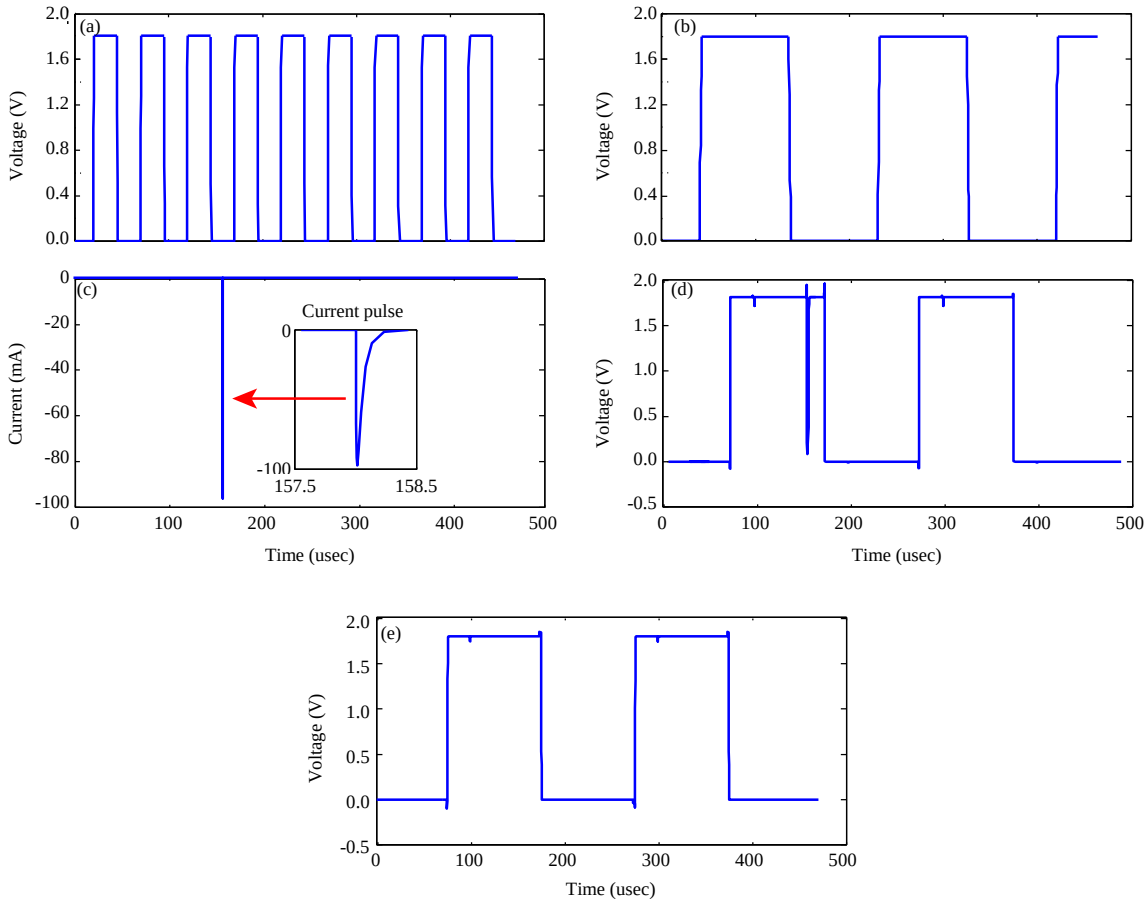

Fig. 8(a-e): Performance of SEU hardened DICE circuit, when LET = 100MeV•cm^2/mg, (a) Clock signal, (b) Input signal, (c) Current pulse used to emulate SEU effect, (d) Output of traditional DICE circuit and (e) Output of SEU hardened DICE circuit

Fig. 8d. This kind of transient upset will lead to wrong logical result when applied in combinational circuits. While, the proposed shift register circuit was immune to this kind of upset which showed great SEU hardening performance and the result was shown in Fig. 8e. Due to the low probability of bombarding during the rising edge of the clock signal and simultaneously bombarding two or more sensitive nodes, no further discussion about these cases was introduced in this study.

Also, as an example, the layout of the proposed DICE circuit was designed based on TSMC 0.18 μm process, shown in Fig. 9 illustrated the corresponding layouts of the schematic parts. Also, more SEU-hardening measures were introduced during the layout design to further reinforce the performance. Firstly, metallic crossings were reduced to prevent mutual disturbing. Secondly, groups of nodes which store the same information were cross arranged to prevent charge sharing. Thirdly, the distance of P type and N type transistors was increased. Fourthly, contacts were added next to the active region.

DISCUSSION

Based on the above method analyses and simulations, we compare the SEU hardening performance of three types of registers, including the one with SEU hardened POR, the one with SEU hardened DICE and the one with both. The results are shown in Table 1.

If the POR circuit is not SEU hardened, the output state of the shift register can be easily upset by particle bombardment due to the incorrect resetting signal. Therefore, this type of register has poor SEU hardening performance. As the performance of the SEU hardened DICE is better than traditional DICE, the proposed shift register based on bilateral resetting POR and SEU hardened DICE circuit shows great SEU hardening performance.

Compared with previously published studies about shift registers, in this study, based on traditional structures of shift registers, as well as combining the theory of transient circuit analysis, the performance of the SEU-hardened shift register is elaborated from aspects of both schematic and layout. As

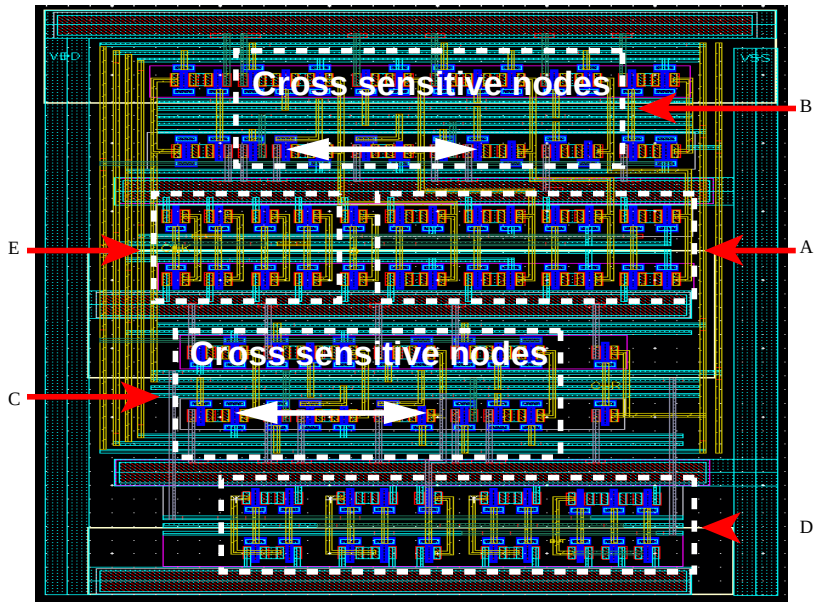

Fig. 9: Layout of the rad-hardened DICE circuit

Table 1: SEU hardening performance comparison of shift registers

	DICE	
SEU hardening performance	Traditional	SEU hardened
POR		
Traditional	Poor	Poor
SEU hardened	Moderate	Fine

shown in the above simulation results, we can see that bilateral resetting POR and SEU hardened DICE (combined bit-line segregation, clock redundancy and tri-mode redundancy) is more tolerant to radiation than traditional ones (Calin *et al*., 1996).

CONCLUSION

In this study, a high-performance SEU hardened shift register is proposed utilizing bilateral resetting POR, bit-line segregation and tri-mode redundancy technologies. The upsetting probabilities of POR and DICE circuits in our designed register are greatly reduced. The present shift register is designed on TSMC 0.18 μm process and simulated with Cadence Spectre. The bi-exponential current source model is applied to emulate the particle bombardment in the simulation. The results of transient analysis show great SEU hardening performance of the proposed shift register. Compared with traditional designs, the proposed shift register has better reliability and is more tolerant to radiation. The application of this design can be widely extended in astronautic field.

ACKNOWLEDGMENT

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