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Power-gating Schemes of MOS Current Mode Logic Circuits for Power-down Applications

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Abstract: With the increasing demand for battery-operated mobile platforms, energy-efficient designs have become more and more important for nanometer CMOS circuits. Compared Conventional Cmos Voltage-mode Logic (CMOSVML), MOS Current-Mode Logic (MCML) can operate at a high frequency. However, the MCML circuits have larger static power consumptions than CMOSVML ones due to their constant operation currents. In this paper, various power-gating schemes for MCML circuits are addressed to reduce their static power dissipations in sleep mode. The power-gating switches of the four power-gating schemes are realized by the PMOS transistors for linear load resistors of MCML circuits, the additional high-threshold PMOS transistor, the bias NMOS transistor for MCML circuits and the additional high-threshold NMOS transistor, respectively. The structure and operation of the proposed power-gating schemes are presented. In order to verify the correctness of the proposed power-gating schemes, a mode-10 counter based on MCML circuits are realized. All the circuits are simulated with HSPICE at SMIC 130 nm CMOS technology. The simulation results show that the power dissipations of the MCML circuits can be greatly reduced by shutting down their idle logic blocks. The proposed power-gating MCML circuits can be used for low-power high-speed applications.

Key words: MOS current-mode computing, low-power electronics, high-speed application, power-gating technique

INTRODUCTION

The output voltage swing ΔV in MOS Current-Mode Logic (MCML) circuits is taken as several hundred millivolts (Alioto and Palumbo, 2003). Obviously, its swing is much little than conventional CMOS voltage-mode logic (CMOSVML) circuits (Hassan *et al*., 2005; Wu and Hu, 2011), so that the circuits designed with the MCML techniques can operate over a higher speed (Yamashina and Yamada, 1992; Hi and Li, 2013). Therefore, MCML circuits are generally suitable for high-speed applications, such as optical transceivers and high-performance processors (Yamashina and Yamada, 1992; Tanabe *et al*., 2001; Musicer and Rabaey, 2000).

Nowadays, energy has become one of the most valuable sources. With the increasing demand for battery-operated mobile platforms like portable computers, laptops, cellular phones, wireless sensors and biomedical applications that require ultra-low energy dissipations, energy-efficient designs have become more and more important for computer hardware (Zhang *et al*., 2011). In CMOSVML circuits, power dissipation consists mostly of dynamic and static components. The total power consumption can be expressed as (Zhang *et al*., 2011).

$$P_{CMOS} = afC_L V_{DD}^2 + V_{DD} I_{leakage} \quad (1)$$

where, CL is load capacitance, VDD is source voltage, f is operation frequency, $I_{leakage}$ is leakage current and a is signal activity, respectively. In Eq. 1, the first and second terms are dynamic and leakage power dissipations, respectively. In early CMOS technology, the leakage power dissipation can be neglected and the dynamic power dissipation caused from charging and discharging loads is major in total power ones (Zhang *et al*., 2011). Continued technology scaling reduces area and delay of the CMOS circuits at the expense of degradation in leakage power dissipation (Hu and Yu, 2012). The power dissipation caused by leakage currents of MOS devices has been an important factor for low-power designs in computer hardware (Hu and Yu, 2012).

In CMOSVML circuits, an effective method for reducing leakage power is MTCMOS (Multi-Threshold CMOS) power-gating techniques (Fallah and Pedram, 2005). Since not every cell works all the time in the circuits, the source voltage can be cut down when they are in sleep mode to reduce their power losses by using low-leakage sleep transistors with high threshold (Kao and Chandrakasan, 2001). The MTCMOS

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technology is difficultly applied to flip-flops directly, because the data stored in traditional CMOSVML ones will be lost when the power supply is shut down. Therefore, the extra circuits for storing data during sleep mode should be added in CMOSVML flip-flops.

The power consumption of the MCML circuits with given voltage and current is a constant (Hu *et al*., 2012). The static power dissipation of MCML circuits is much large than the traditional CMOSVML, because of their constant currents in all operation time (Hu *et al*., 2012). Similar to CMOSVML, power-gating techniques can be introduced into MCML circuits to reduce static dissipations. However, the structure and operation are different from CMOSVML. In this study, various power-gating schemes for MCML circuits are addressed to reduce their static power dissipations in sleep mode. In order to verify the correctness of the proposed power-gating schemes, a mode-10 counter based on MCML circuits are realized. The power dissipations of mode-10 counters based on the conventional MCML without power-gating and the proposed power-gating MCML are compared by using HSPICE simulations.

REVIEW OF MCML CIRCUITS

The inverter/buffer can be realized based on MCML, as shown in Fig. 1 (Musicer and Rabaey, 2000; Hu *et al*., 2012). The NMOS Ns acts as the current source that is used for the differential input pair, which is mirrored from the current source in the bias circuit. The transistors P1 and P2 operating at linear region are used for the loads of the differential input pair. The control voltage V_{rfp} is from the bias circuit. The output logic swing is controlled by the bias circuit. The logic functions of the MCML circuits are realized with the pull-down network (NMOS transistors N1 and N2).

In the MCML circuits, the high and low levels of the output voltages are $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - I_B R_D$, respectively, where R_D is linear resistance of the PMOS transistors and I_B is the circuit of the NMOS Ns. The logic swing ΔV can be written as $I_B R_D$.

MCML is a type of differential logic with differential input logic tree. A logic gate can be realized by using the corresponding differential pull down network. The MCML basic gates such as AND2/NAND2, OR2/NOR2, XOR2/XNOR2 are shown in Fig. 2.

The power consumption of MCML can be expressed as:

$$P = V_{DD} I_B \quad (2)$$

From Eq. 2, there is static power dissipation in MCML circuits in all operation time because of their constant currents. This means that the static power dissipation of MCML circuits much larger than the traditional CMOSVML. However, not every cell works all the time. This behavior leads to needless waste of power.

POWER-GATING SCHEMES FOR MCML CIRCUITS

Power-gating is an effective way to reduce the power dissipation. Since the structure, operation and signal waveforms of the MCML circuits are different from the conventional CMOSVML ones, the power-gating schemes and switches of the MCML circuits should be also different.

In this section, four power-gating schemes for MCML circuits are addressed to reduce their static power dissipations in sleep mode. Their power-gating switches are realized by the PMOS transistors for linear load resistors of MCML circuits, the additional high-threshold

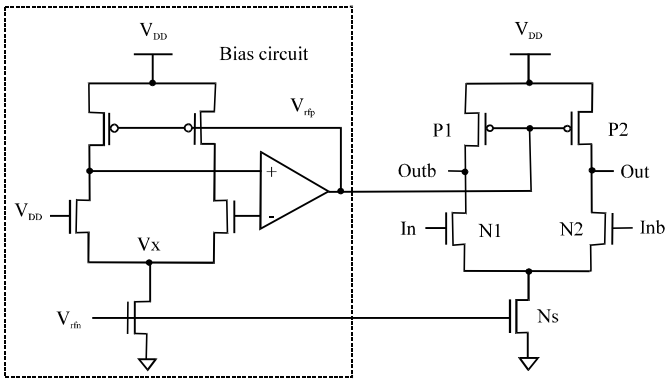

Fig. 1: MCML inverter/buffer and its bias circuit

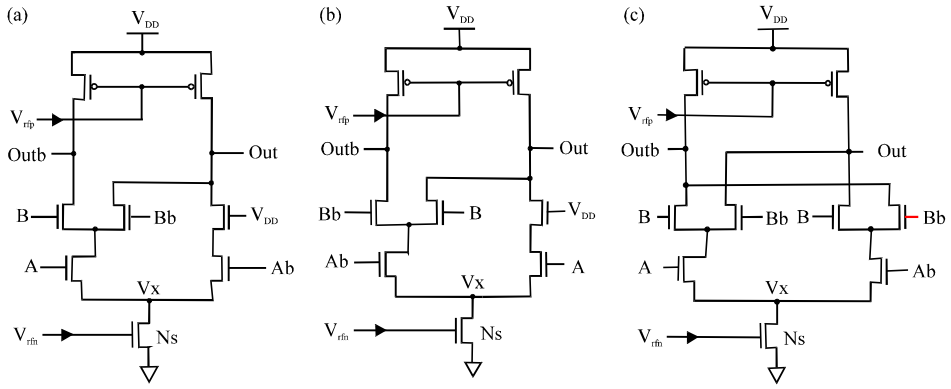

Fig. 2(a-c): Basic gates based on MCML, (a) AND2/NAND2, (b) OR2/NOR2 and (c) XOR2/XNOR2

PMOS transistor, the bias NMOS transistor for MCML circuits and the additional high-threshold NMOS transistor, respectively, as shown in Fig. 3.

In the power-gating MCML circuit shown in Fig. 3a (PMOS_ linear transistors), an extra input signal sleepb (active control signal) is added to control V_{rfp}. The high-threshold PMOS transistors (P1 and P2) used for linear load resistors of MCML circuits are used for power-gating switches. A power-gating control circuit consisting of NMOS transistor (G2) and PMOS transistor (G1) is added for switching power-gating switches under the control of the signal sleepb. The power-gated MCML circuits works in two modes under the control of sleepb (active control signal). When sleepb are high, the circuit works in active mode. The PMOS transistor G1 is off and the NMOS transistor G2 is turn on and thus $V_p = V_{rfp}$, so that the power-gating switches (P1 and P2) act as normal linear load transistors. Therefore, the MCML circuits operate in active mode.

In the power-gating MCML circuit shown in Fig. 3b (PMOS_ additional transistor), an extra input signal sleep (sleep control signal) is added to shut down the power source V_{DD}. The additional high-threshold PMOS transistor is used for power-gating switches. The power-gated MCML circuits works in two modes under the control of sleep. When sleep is low, the PMOS transistor G1 is turn on, so that the virtual power source follows the V_{DD}. In this mode, the MCML circuits act as usual and thus the circuit works in active mode. When sleep is high, the PMOS transistor G1 is turn off, the virtual power source is shut down and thus MCML circuits operate in sleep mode.

In the power-gating MCML circuit shown in Fig. 3c (NMOS_ bias transistor), an extra input signal sleep (sleep control signal) is added to control V_{rfn}. The high-threshold transistor (Ns) used for the bias current of MCML circuits is used for power-gating switch. A power-gating control circuit consisting of NMOS transistor (G2) and PMOS transistor (G1) is added for switching power-gating switches under the control of the signal sleep. The power-gated MCML circuits works in two modes under the control of sleep. When sleep are low, the PMOS transistor G1 is turn on and the NMOS transistor G2 is off and thus $V_N = V_{rfn}$, so that the bias transistor (Ns) act as normal bias current source. Therefore, the MCML circuits operate in active mode. When sleep are high, the PMOS transistor G1 is off and the NMOS transistor G2 is turn on, so that V_n is set as GND and thus the bias current source is shut down. Therefore, the circuit works in sleep mode.

In the power-gating MCML circuit shown in Fig. 3d (NMOS_ additional transistor), an extra input signal sleepb (active control signal) is added to shut down the bias current source. The additional high-threshold PMOS transistor is used for power-gating switches. The power-gated MCML circuits works in two modes under the control of sleepb. When sleepb is high, the NMOS transistor G1 is turn on, so that the current source acts as usual and thus the MSML circuit works in active mode. When sleepb is low, the NMOS transistor G1 is turn off, so that the bias current source is shut down and thus MCML circuits operate in sleep mode.

The sub-threshold current of MOS transistors I_{sub} occurs due to minority carrier move by diffusion along the surface below the channel, when the gate voltage is below the threshold voltage. It is the dominant contributor to the total leakage current at nanometer CMOS process. I_{sub} can be expressed as:

$$I_{sub} = \frac{W}{L}\mu V_T^2 C_{sth} \exp\left(\frac{V_{GS} - V_{th} + \eta V_{DS}}{nV_T}\right) \times \left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (3)$$

where, W and L denote transistor width and length, μ denotes carrier mobility, $V_T = kT/q$ (≈26 mV) is thermal

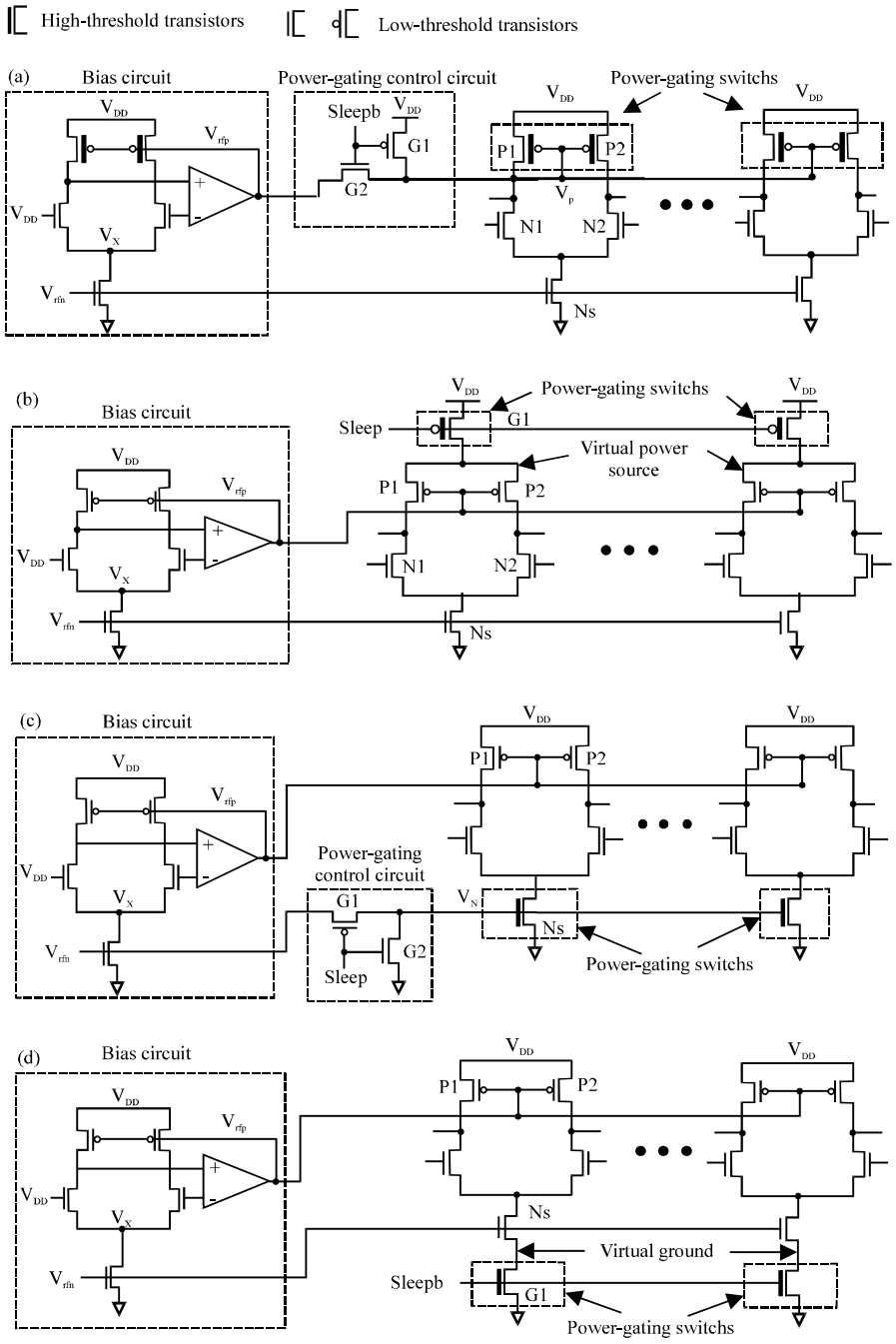

Fig. 3(a-d): Four power-gating schemes in which the power-gating switches are realized with, (a) The PMOS transistors for linear load transistors (PMOS_ linear transistors), (b) The additional high-threshold PMOS transistor (PMOS_ additional transistor), (c) The bias NMOS transistor (NMOS_ bias transistor)] and (d) The additional high-threshold NMOS transistor (NMOS_ additional transistor)

voltage at temperature T, $C_{sth} = C_{dep}+C_{it}$ denotes the summation of depletion region capacitance and interface trap capacitance both per unit area of the MOS gate, V_{GS} and V_{DS} are gate-source voltage and drain-source voltage, V_{th} is threshold voltage, η is drain-induced barrier lowering (DIBL) coefficient and $n = 1+C_{sth}/C_{ox}$ is slope shape factor, where C_{ox} is gate input capacitance per unit area of the MOS gate.

From Eq. 3, the sub-threshold leakage current increases exponentially with threshold voltage (V_{th}). For a typical technology with a sub-threshold slope of 100 mV decade^{-1}, each 100 mv reduction in V_{th} will cause an order of magnitude increase in leakage currents. Therefore, increasing the threshold voltage can reduce leakage dissipations. In the proposed four power-gating schemes, the all power-gating switches are realized with high-threshold transistors to reduce their leakage power in sleep mode.

SIMULATIONS OF POWER-GATING MCML CIRCUITS

To certify the correctness of these power-gating schemes, the four power-gating MCML circuits are simulated using HSPICE with SMIC 130 nm technology. A mode-10 MCML counter is used for the power-gated circuits. The four power-gating schemes are applied to this counter.

The structure of the MCML D flip-flop is shown in the Fig. 4. The most common approach for constructing D flip-flop is to use a master-slave configuration. The MCML D flip-flop is realized by cascading a negative latch (master stage) with a positive one (slave stage), as shown in Fig. 4a and b. The current switching between the pairs takes place by the complementary signals of the clock. The sample pair works as a buffer. When it is activated by the clock signal, it keeps track of the input data and transforms it to the outputs. This is known as the sampling mode of the latch. When the clock polarity changes, the hold pair becomes active, the cross-coupled transistors in hold pair from a regenerative positive feedback structure keep the output data in the same previous state. This is known as the hold mode because the output is isolated from any changes in the input data, as no current should be flowing through the sampling pair.

The structure of the decimal counter based on MCML is shown in Fig. 5. The decimal counter consists of NAND2, NAND3 and D flip-flop. The MCML decimal counter is stimulated by using HSPICE at the 130 nm CMOS process.

The simulation waveforms of the power-gating MCML mode-10 counters are shown in Fig. 6. Its operating frequency is 200 MHZ. Because the waveforms of these four power-gating schemes are similar, only one of the waveforms of these four power-gating circuits is listed.

As is shown in Fig. 6, the power-gated MCML circuits have proper logic functions when sleepb is high. On the other hand, the outputs Q0-Q3 are all set to low level when sleepb is 0, since the power-gated MCML blocks are shut down by using the power-gating.

The power dissipations of the MCML mode-10 counters with the power-gating schemes and without power-gating have been compared in Fig. 7a in various operating frequencies. In these simulations, the active ratio α ($\alpha = T_{active}/(T_{active}+T_{sleep})$ is taken as 0.8. From Fig. 7a, all the four power-gating schemes have an advantage over power dissipation compared with the normal MCML circuit without power-gating over a wide range of operating frequencies for α = 0.8. Moreover, the power dissipation savings of the four power-gating schemes are almost the same.

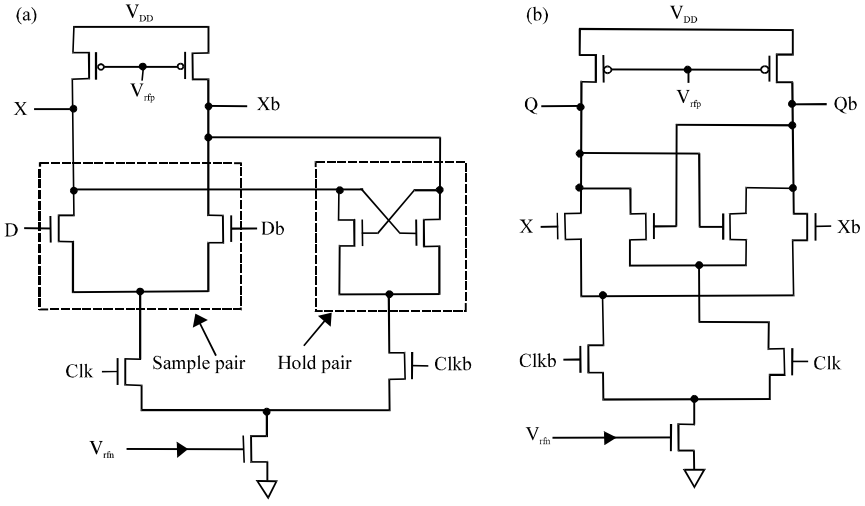

Fig. 4(a-b): MCML D flip-flop with master-slave configuration, (a) Negative latch (master stage) and (b) Positive latch (slave stage)

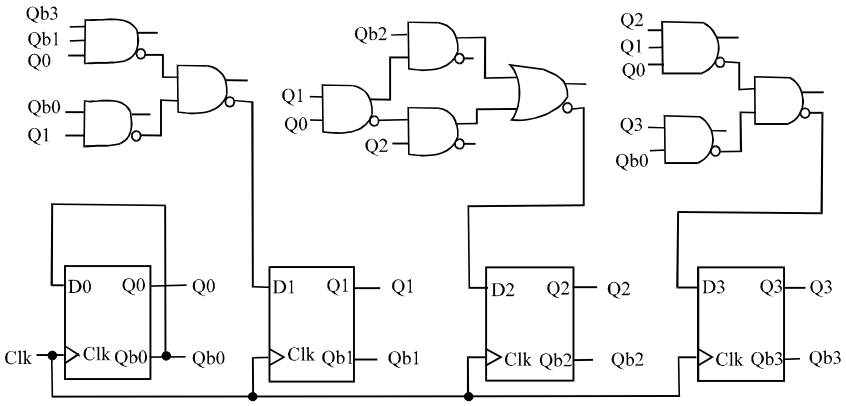

Fig. 5: Mode-10 counter consisting of the two-input and three-input MCML NAND gates and MCML D flip-flops

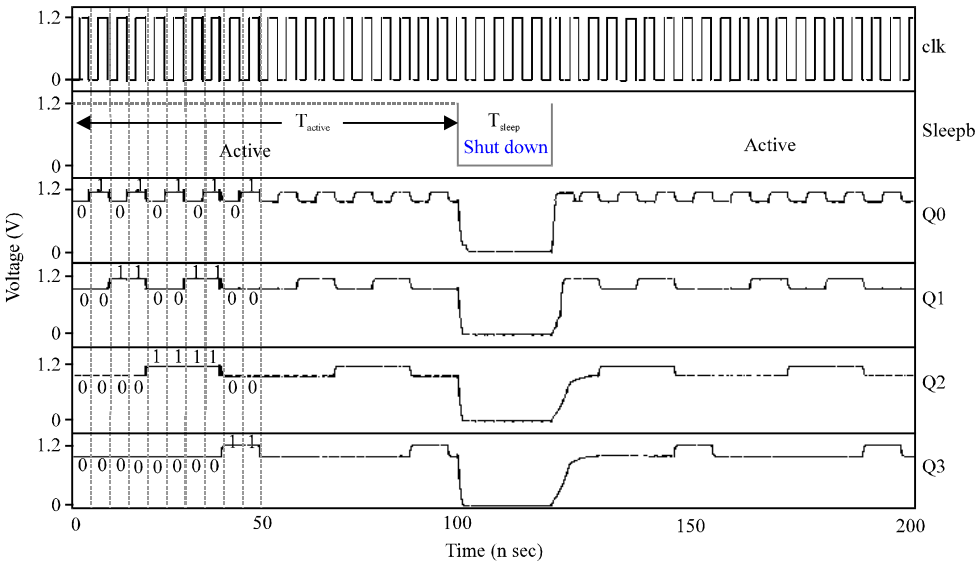

Fig. 6: Simulated waveforms of the power-gating MCML mode-10 counter

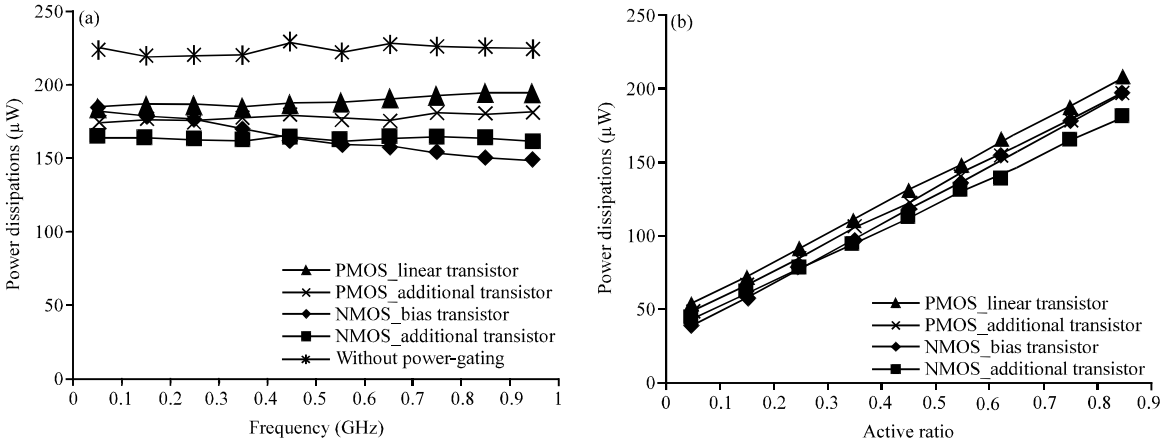

Fig. 7(a-b): Power dissipation comparisons of MCML mode-10 counters with power-gating and without power-gating in, (a) Various frequencies and (b) Various active ratios

The active ratio affects strongly the energy dissipation of the power-gating MCML circuits. The energy dissipations of the power-gating MCML mode-10 counters are shown in Fig. 7b for different active ratios. In these simulations, the operating frequency is 250 MHZ. The power-gating MCML circuits can attain large energy savings for a small active ratio.

CONCLUSION

Compared conventional CMOS Voltage-Mode Logic (CMOSVML), MOS Current-Mode Logic (MCML) can operate at a high frequency. However, the MCML circuits have larger static power consumptions than CMOSVML due to their constant operation currents. In this study, various power-gating schemes for MCML circuits have been addressed to reduce their static power dissipations in sleep mode. In order to verify the correctness of the proposed power-gating schemes, a mode-10 counter based on MCML circuits have been realized. All the circuits are simulated with HSPICE at SMIC 130 nm technology. The simulation results certified the correctness of these power-gating schemes. The power dissipations of the MCML circuits can be greatly reduced by shutting down their idle logic blocks. Besides, the active ratio has a great influence on energy dissipation. The power-gating MCML circuits can attain large energy savings for a small active ratio.

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