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A Real-time and Cost-Effective Image Processing System for Quality Assurance of Sheet Materials

[1,2]Qiwu Luo, [2,1]Yigang He, [1]Wenxin Yu and [1]Jian Zheng
[1]College of Electrical and Information Engineering,
Hunan University, Changsha, 410082, Hunan, China
[2]School of Electrical and Automation Engineering,
Hefei University of Technology, Hefei, 230009, Anhui, China

Abstract: Real-time surface defect inspection of sheet materials is increasing challenge due to the fast production rhythm and high requirement of quality. Choosing Xilinx Virtex-6 FPGA XC6VLX240T, this study presents an embedded hardware scheme for online image acquisition and parallel data processing, then realized it on a 12-layer Print Circuit Board (PCB) with a high performance of signal integrity. The equipped PCI express (PCIe) interface supports expansion with host PC smoothly which had achieved an actual peak transfer rate high up to 1.788 Gbps. At the end of this study, the designed FPGA platform was used as a sub-system to steel surface inspection equipment applying in a hot-rolled workshop. The application effects showed that this system was qualified for the real-time computational task when the maximum rolling speed is as high as 18 m sec^{-1}. Due to the advantages of source-open, customization and cost-effectiveness, the embedded FPGA platform is standing ready for widespread adoption of quality assurance in the sheet material fields.

Key words: Surface defect inspection, field programmable gate array, digital image processing, machine vision, quality assurance

INTRODUCTION

Quality assurance is a pivotal aspect in continuous sheet material production. As a significant attribute in products, quality itself is a crucial differentiator between their own offerings and those of competitors, so that it is increasingly recognized and emphasized by suppliers. With the high requirement for the quality of the products in the iron and steel industry, the product quality assurance is of great importance and become a hot issue. The intense commercial competition has gradually promoted nearly all the sheet material manufacturers including steel factories to increase its production efficiency insuring high level of quality simultaneously.

In order to meet the pressing demand of online quality detection and controlling, intelligent machine vision technology has been widely applied for building real-time steel surface defect inspection system as a result of its high resolution, non-contacting and smart size (Steger *et al*., 2008). During this process, some companies such as Cognex Corporation (Cognex, 2013), ISRA (ISRA, 2013a) and ISRA Vision (ISRA, 2013b) have done some contributions to develop some surface defect inspection equipments, overcoming some barriers of tough environment, continuous vibration, defect classification as well as defect database management. Most of them consist of high speed cameras, frame grabber cards, Industrial Personal Computers (IPCs) and workstations and the workstations are responsible for running defect detecting algorithms. Supposing that each camera is equipped with an industry control computer for image acquisition and a workstation, plus additional circuits and physical constructions, a commercially available system now costs approximately $ 800,000 to $ 2100,000 which is seemly not affordable for the average steel factory. However, perhaps these enterprises concentrating on the commercial value, economic benefits and intellectual property right, the corresponding technique details are not (or rarely) reported commonly.

In recent literatures, many researches tried to propose some new algorithms or to develop some low cost inspection systems to overcome the barriers mentioned above. Pernkopf and O'Leary (2003) provided contrastive analyses about image acquisition for surface inspection applications which can help us to capture high quality image of metallic surface. A computer vision system for automatic steel surface inspection was developed (Liu *et al*., 2010). Its average detecting time consumption

Corresponding Author: Qiwu Luo, College of Electrical and Information Engineering, Hunan University, Changsha, 410082, Hunan, China

of one image (2048×512 pixels) is 0.2839 sec, with the correct detection rate being more than 85%. At the same time, some embedded image processing based on FPGA emerged for speedy processing (Li *et al*., 2011). However, there are still some obstacles which at least, need further research to overcome. The biggest one is how to achieve the real-time analysis, in other words is, as for PC-based approaches, the speedy computation and transmission of massive data gathered in a very short period is usually infeasible because of its serial execution mechanism of command. Furthermore, the produce rhythm is often seriously fast. Taking hot-rolling mill for an example, the normal rolling speed is high up to 12 m sec^{-1} (the maximum speed is 18 m sec^{-1}), with the width of less than 1.65 m. If the resolution radio of defect inspection system is 0.5×0.5 mm, the peak image data flow can be derive as Eq. 1:

$$Q = (w/r_w)\times(v/r_v) = (2\,m/0.5\,mm)\times (18\,m\,sec^{-1}/0.5\,mm) = 144\ Mpixes\ sec^{-1} \quad (1)$$

where, w is the width of camera FOV (field of view), for retaining some engineering margin, it is set slightly wider than the width of billet. v is the billet rolling speed. r_w and r_v are the lateral resolution and vertical resolution respectively. If the selected camera is gray line-scan type, with each pix discretized as one byte, then the peak data flow Q is high up to 1.152 Gbps which is really a heavy analysis task to the image processing equipment. What is more, the gradual image backlog would make the situation by far worse.

This study presents a novel methodology that takes advantage of the speedy and parallel data processing capability of Field Programmable Gate Array (FPGA) and realizes it on a 12-layer Print Circuit Board (PCB) for improving the signal integrity. Image subdividing method (Liu *et al*., 2008) is imported and each image block (32×32 pixel) is stored in block RAM (BRAMs), then denoising algorithms and image feature computations of image blocks are realized parallel on FPGA. According to the multi-threshold approach based on the feature values, the proposed image processing platform can identify whether the raw image blocks are defective or non-defective.

The main contribution of this design is the development of a low-cost, real-time hardware image processing system for online quality assurance of hot-rolled strip. And this system is successfully applied in a hot-rolled workshop in Valin LY Steel which also can be widely promoted to other sheet material industries such as printing, aluminum and glass producing.

PROPOSED HARDWARE ARCHITECTURE

Here, put forward a hardware scheme of surface defect inspection platform based on FPGA, its structure diagram is shown in Fig. 1. As the 'heart' of the board, the main processor is XC6VLX240T which belongs to Xilinx Virtex-6 family. The whole system can be mainly divided into three functional blocks: Image acquisition unit (label 1), image processing unit (label 2) and data transmission unit (label 3). And the corresponding device drivers are packed as Intellectual Property (IP) cores which are organized by an 32-bit embedded software processor MicroBlaze (label 4) via., Processor Local Bus (PLB). The power system (label 5) can not only provide the working voltage of each unit, but also control the time sequence of each supply voltage monitored by a power-on and reset generator with adjustable delay time from 1.25 m sec to 10 sec. At the same time, in order to enhance the maintainability of the system, a flexible Universal Asynchronous Receiver/Transmitter (UART) interface (label 6) is equipped for program debugging.

The image acquisition unit (label 1) supports two kinds of camera interfaces, one is cameral link interface proposed by NI (NIC, 2000) and its detailed design had been illustrated in the previous studies (Luo *et al*., 2013). Here, it was integrated into the whole system for better signal integrity through Cameral Link Driver and UART controller1. NI LVDS-CMOS Data Conversion Chip Array consists of electric level conversion chips: DS90CR288A, DS90LV047 and DS90LV019. The other is Gigabit Ethernet which is managed by the media access control (MAC) IP core. The module No. of physical layer (PHY) chip is 88E1111 manufactured by Marvell. Consequently, this system is compatible with various high-speed cameras because neally all of which are equipped with these two interfaces.

As for the image processing unit (label 2), the computing center is constituted by Digital Signal Processing (DSP) cores, with abundant cache such as Block Random Access Memory (BRAM) and Double Data Rate 3 (DDR3) SDRAM around them. The DSP cores are basically composed of advanced DSP48E slices, Look-Up Tables (LUTs), true dual-port RAM blocks and First Input First Output (FIFOs) (Xilinx, 2012). They are developed obeying black box which can be smoothly described in VHDL or M language, any other engineers can embed related algorithms for their specific purpose.

When it comes to the data transmission unit (label 3), it is worth concern that four 128-MB DDR3 SDRAM chips were employed, providing massive data-storage capacity which is propitious to both data transmission and image

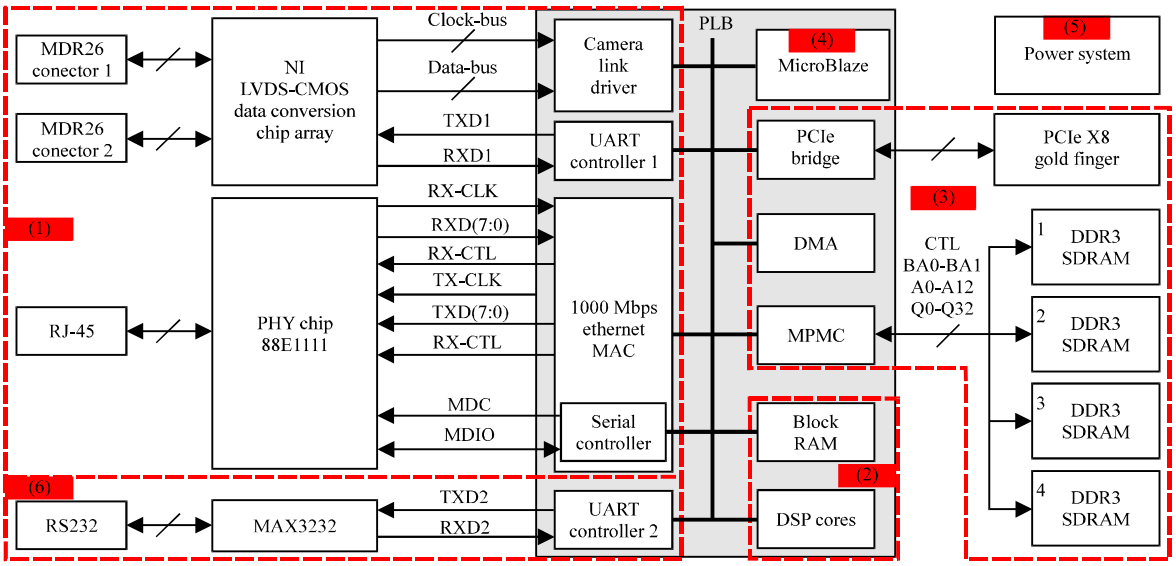

Fig. 1: Hardware structure and signal topology. This diagram is organized according to the direction of signal flow and all the modules in the grey box are realized in FPGA chip. Label 1 is the image acquisition unit, supporting cameras with Gigabit Ethernet and Camera Link interfaces and the camera can be configured through UART Controller 1 by the software processor-MicroBlaze. Label 2 is the image processing unit, massive dataflow is computed parallel by the DSP Cores, around of them is speedy Block RAM. The data transmission unit (label 3) is a PCIe X8 type with DMA engine, so that, Gigabit data can be transparently transported between the local DDR3 SDRAM on FPGA and that of remote IPC

processing units. PCIe Bridge is in charge of the one-to-one address mapping between the embedded FPGA system and IPC. On the FPGA side, the PLB address of DDR3 SDRAM is monitored by Multi-Port Memory Controller (MPMC) while on the remote IPC side, its physical RAM address is mapped into PLB domain through PCIe Bridge. And with the help of the Direct Memory Access (DMA) controller, block-data can be moved freely among the BRAM, DDR3 SDRAM and the remote RAM without supervision of MicroBlaze on FPGA or CPU on IPC.

HARDWARE CIRCUIT IMPLEMENTATION

The proposed hardware architecture includes a large quantity of high-speed traces between chips as follows:

- The frequency of data, address and control bus between FPGA and DDR3 chip is high up to 200 MHz (1/4 multiply by the operating frequency of DDR3)
- The camera LVDS bus frequency is high up to 560 MHz when the pix clock frequency is 80 MHz
- The theoretical transfer rate of PCIe (configured as generation 2) is high up to 2.5 Gbps (Xilinx, 2010)

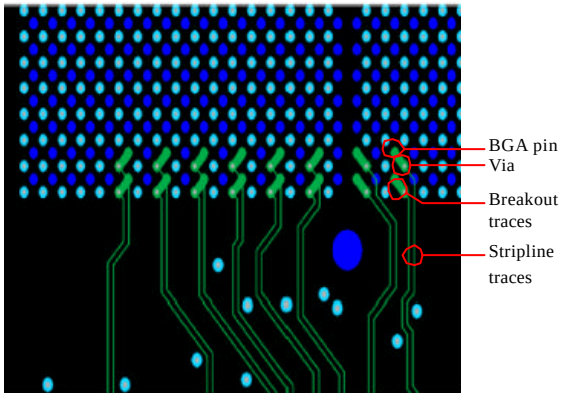

Fig. 2: Layout of stripline traces for PCIe interface

According to the transmission line theory, the impedance of LVDS line must be controlled at 50 ohms (±5%) for reducing the signal interference, the length tolerance of high-speed differential pairs is seriously critical. Taking PCIe part for an example, the layout of the differential stripline traces is demonstrated in Fig. 2, the fan-out direction of Ball Grid Array (BGA) package and trace gap are significant for the signal integrity. In

Table 1: Layer stack up and parameters of the 12-layer board

Layer stack up	No.	Thickness (mil)	Net
	1	1.8(0.5 oz•plating)	Sig-h1
	A1	3.9	
	2	1.2(1.0 oz)	Ground
	B1	5.12	
	3	1.2(1.0 oz)	Sig-v1
	A2	7.3	
	4	1.2(1.0 oz)	Ground
	B2	5.12	
	5	1.2(1.0 oz)	Sig-h2
	A3	7.3	
	6	1.2(1.0 oz)	Sig-v2
	B3	5.12	
	7	1.2(1.0 oz)	Ground
	A4	7.3	
	8	1.2(1.0 oz)	Sig-h3
	B4	5.12	
	9	1.2(1.0 oz)	POWER
	A5	7.3	
	10	1.2(1.0 oz)	Sig-v3
	B5	5.12	
	11	1.2(1.0 oz)	Ground
	A6	3.9	
	12	1.8(0.5 oz• plating)	Sig-h4

No.1-12 layers are the conductive layers while the No. A1-A6, No. B1-B5 are the inter-layers. The 3rd and 4th column give the corresponding parameters about each layer

order to minimize the signal 1st-reflection, impedance termination is necessary and important near the receivers (Johnson and Graham, 2010). It can be clearly seen from Fig. 2 that any FPGA signal is transmitted obeying following path: BGA pin, breakout traces, via., stripline traces and PCIe gold finger, where the BGA pin and PCIe gold finger make up the signal transmitter-receiver pair. The trace width and trace gap of the differential traces are 6 and 8 mils respectively in this study.

The PCB layer stack up and the related parameters are presented in Table 1. There are 12 conductive layers and 11 interlayers between them and the total thickness of PCB is around 2.0 mm. The No. 3 (Sig-v1), No. 6 (Sig-v2), No. 10 (Sig-v3) are vertical wiring signal layers while No. 1 (Sig-h1), No. 5 (Sig-h2), No. 8 (Sig-h3), No. 12 (Sig-h4) are horizontal wiring signal layers, the other conductive ones including No. 2, 4, 7, 11 and 9 are copper layers, with the first four layers being ground layers while the last one being power layer. The cuprum thickness of each signal layer and the dielectric constant of each interlayer are given in the third column of Table 1. A simple way to understand the meaning of 1.0 oz foot^{-2}

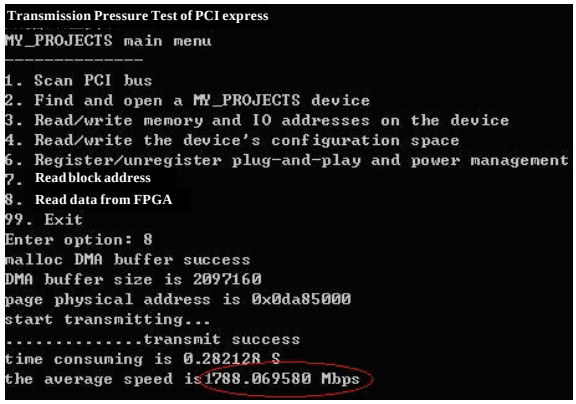

Fig. 3: PCIe transmission rate recorded on the IPC interface

is that it equals to some 1.2 mils thickness derived together with the density of copper. After tin plating, the top layer (No. 1) and bottom layer (No. 12) are thicken to 1.8 mils.

The online defect inspection system for surface quality study covers Gbps-grade massive image acquisition, computation and transmission and therefore the testing for its real-time performance is extremely significant and worth considering. From repeatedly transmission ability testing aiming at PCIe interface, its testing conditions are as follows. 241 packets were prepared to be sent continuously from FPGA to IPC and each packet contained 2097160 bits data, the matched DAM buffer size was defined as the same as packet size. Then data transmission was started, the total time consumption recorded by testing interface running on IPC is 0.282128 sec. The experimental results presented in Fig. 3 showed that its peak transfer rate in a single-direction (from FPGA to PC) had achieved 1.788 Gbps.

The experimental figure is a screenshot from the interface software on IPC, there are 8 options presented respectively in it. After scanning PCI bus, the designed FPGA card can be found in the bus tree, the testing results were not generated until the option 8 (read data from FPGA) was selected.

APPLICATION CASE

In the hot strip factory, there are plenty of defects such as foreign matters, roller traces, scarring errors, scratches and spots on the slab surface caused by various reasons which means massive loss of finance and reputation to the steel manufacturers. From the corresponding literatures, despite the real-time

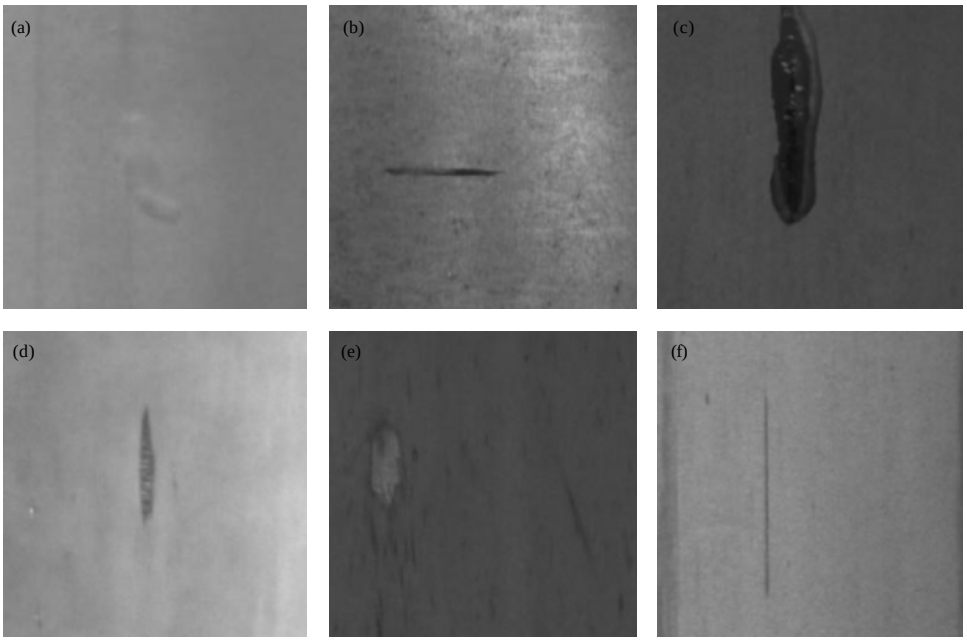

Fig. 4(a-f): Defective samples identified by the proposed system. These 6 types of defects cover approximately above 98% of all the occurred ones, the category names are as follows (a) Roll marks, (b) Horizontal scratches, (c) Entrapped slag, (d) Oxide scales, (e) Convex hull and (f) Longitudinal cracks

performance of the automatic defect detection system on hot-rolled flat steel products proposed by Ghorai *et al.* (2013) have realized the real-time computation when the rolling speed is under 5 m sec^{-1}, rare commercial or research products can achieve the actual online defect inspection when the rolling speed is as high as 18 m sec^{-1}.

The proposed FPGA-based image processing board was used as a sub-system to an online steel surface inspection equipment which has been applied in a hot-rolling mill in Valin LY Steel in southern China. Some efficient algorithms based on Defect Characteristics Fusion (DFF) with Pre-Denoising Function (PDF) are realized parallel on the FPGA chip, thus the embedded platform can determine preliminarily whether the raw images are defective or non-defective. Then keep the defective ones and send them to the IPC for following stage to make an accurate defect assessment. Some universal defects occurred in the mentioned hot-rolling mill identified by the proposed system is shown in Fig. 4 which are roll marks (label a), horizontal scratches (label b), entrapped slag (label c), oxide scales (label d), convex hull (label e) and longitudinal cracks (label f) respectively.

Where, the roll marks (label a) are periodical defects usually resulting from damaged rollers, the horizontal scratches (label b) and longitudinal cracks (label f) are random defects always caused by erroneous machineries and the rest of defects often arise as a result of systematic problems mainly in the upstream casting process. These metallurgical defects can be broadly categorized into two groups: Textural defects and geometric defects. Roll marks (label a), entrapped slag (label c) and oxide scales (label d) belong to textural defects which can be detected by the methods based on textural analysis while horizontal scratches (label b), convex hull (label e) and longitudinal cracks (label f) are inside the range of geometric defects, can be indentified by algorithms based on morphological filtering. And the average detection accuracy about these kinds of defects has achieved 95.3% reported from the quality department of Valin LY Steel until August, 2013.

A photo of the proposed image processing system and its distribution of each module are given in Fig. 5. It is this electronic equipment achieved a scientific computational balance between the embedded sub-system and its host PC. Contrasting with Fig. 1, each functional module can be found in Fig. 5. The chip in central of the platform is FPGA (label a), image data from cameras can be captured though MDR26 connector1 (label b1) and MDR26 connector 2 (label b2), with connector1 for base mode and both for medium/full mode. The RJ45 jack (label c) of Gigabit Ethernet interface could

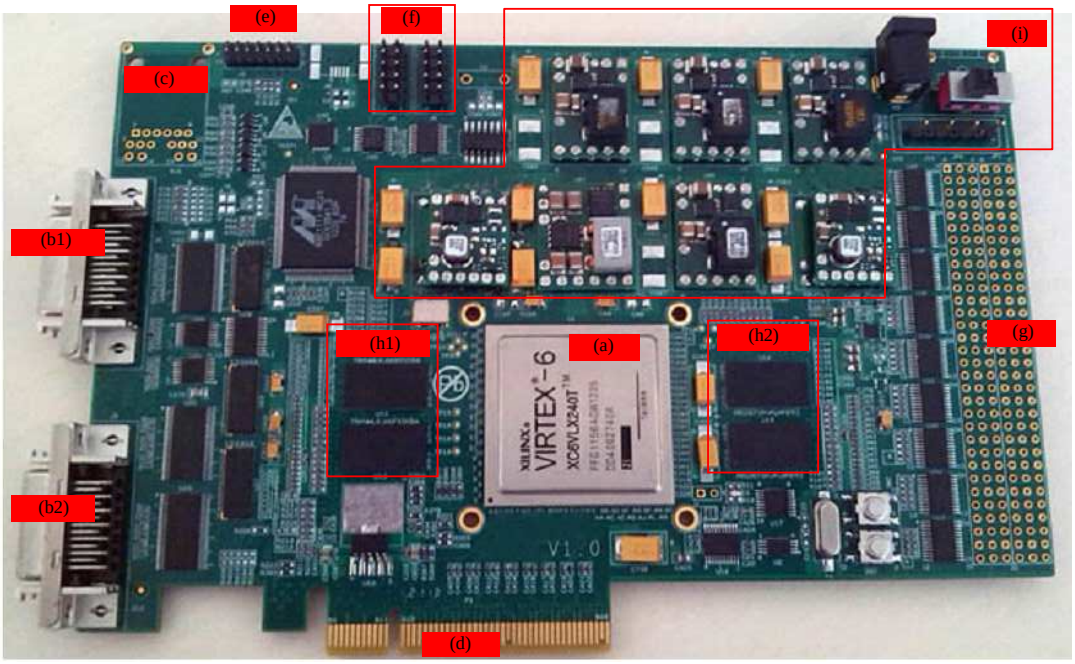

Fig. 5: Functional module distribution in the realized board (a) Virtex-6 FPGA chip. (b1) and (b2) MDR26 connectors for cameras equipped with cameral link interface, (c) RJ45 jack for Gigabit Ethernet, (d) PCI express X8 Gold Finger, (e) JTAG interface, (f) UART interfaces, (g) Extended interfaces, (h1) and (h2) DDR3 chips, (i) Power systems

be welded if necessary. The remaining labels d, e and f and are PCIe, JTAG and UART interfaces communicated with host IPC. Program bit stream can be downloaded into FPGA obeying boundary-scan protocol. It also provides an extended interface namely label g. The four DDR3 SDRAM chips (label h 1 and 2) are placed around the FPGA nearly as possible for ensuring the reliability of data. The devices (label i) supply the multi-voltage power for whole system. The limitation of this equipment is that if the rolling speed is greater than 18 m sec^{-1}, having satisfied the average requirements of recent hot-rolling mill. Above this speed limitation, the operating frequency of MicroBlaze, the capacity of BRAM and the complexity of recognition algorithms become the bottlenecks. In addition, it is worth mentioning that this prototyped surface inspection equipment based on the proposed image processing system has a price tag of about 1/6 of its commercial counterpart, needing not ultra high performance server array.

CONCLUSION

A real-time and cost-effective image acquisition system has been realized on the Xilinx Virtex-6 FPGA. The customized hardware architectural and the individualized PCB layer stack up is more flexible and reliable than the development based on existing evaluation board (Xiang *et al*., 2013) which is beneficial to its promotion and commoditization. When the designed system is applied to the automatic surface defect inspection equipment, the total cost is only about 1/6 of that of a commercially available system while the computation ability is improved to some extent which is qualified for the 18 m sec^{-1} maximum rolling speed. However, improving the efficiency of algorithms embedded on FPGA plays a crucial part in the real-time defect inspection which needs further research.

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