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Design of a New Structure of SAR ADC

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Abstract: This study introduces a novel design of 1MHz 8-bits Successive Approximation Analog-to-Digital Conversion (SAR ADC) circuit for the application of AGC (Auto-Gain Control) module within a RF (Radio Frequency) receiver channel by using 0.25 μm SOI CMOS (Silicon On Insulation, Complementary Metal Oxide Semiconductor) process. The schematic design of the proposed circuit is based on the R-2R resistor matching network, current mirror structure and high precision comparator. Such arrangement improves the overall precision of the proposed SAR ADC. An inside start-pulse generator is employed at the same time to achieve a compact time sequence and further improve the utilization of the overall system clock frequency. The testing results show that the DNL for the proposed SAR ADC is less than 0.5 LSB and its INL is less than 1 LSB.

Key words: Successive approximation analog-to-digital conversion, auto-gain control, R-2R resistor matching network, current mirror structure, start-pulse generator, SOI CMOS

INTRODUCTION

In satellite communication system, the received signal from the antenna can be varied in a wide range from less than -100 dBm to greater than -20 dBm. In order to cope with such wide power level spectrums from the antenna, the receiver module must be able to control its gain with respect to different receiving signal level. The present trend for dealing with such problem is to employ an AGC (Auto-Gain Control) module circuit. It has the ability of reducing the channel gain when the received signal level is high and increasing the channel gain when the received signal level is lower. One of the most important parts for a typical AGC is the Successive Approximation Analog-to-Digital Conversion (SAR ADC) circuit. Its duty is to convert the sampled input signal into digital form for the use of producing a feedback control to the auto-gain amplifier. Its performance highly affects the overall module characteristics of AGC in the way of accuracy, reaction speed and power assumption. Furthermore, the present trend of chip design requires that the SAR ADC has to have a smaller size and lighter. In the literature, the SAR ADC has been widely study by many researchers, such as by Sugiyama *et al*. (2010), the authors have introduced a 2 bit/step conversion SAR ADC by using split capacitor array and dual-sampling technique which has the advantages of less power consumption; however the complex design structure demands a bigger size of chip and advanced fabrication process, it is therefore increasing the overall design difficulty and cost. A similar of 2 bit/step conversion SAR ADC has been proposed by Wei *et al*. (2011). The proposed SAR ADC is based on multi-stage of Kelvin divider and larger number of resistor and control switches, in which lead to a much higher power consumption and larger scale as well. It further leads to complex of fabrication process and higher cost. Hesener *et al*. (2007), the authors have employed a non-binary search algorithm within a designed SAR ADC to increase the conversion rate and reduce the power consumption. However, such design needs complex digital controller and thermometer capacitor array (Chen *et al*., 2009), in which has the same problems with the designs by Sugiyama *et al*. (2010). Therefore, in order to fit the present trend in the field of high demanding communication system such as satellite communications, the power consumption, accuracy, size and cost have to be considered during the design of SAR ADC circuit. Due to the application of the SAR ADC circuit designed in this article, the AGC loop in the receiver's chip worked well and the setting time is less than 1ms which is suitable for the target.

OVERALL SAR ADC SYSTEM DESIGN

The overall system of the proposed SAR ADC consists of a Sample/Hold block, a Comparator circuit, a SAR Control Logic (with some registers) and a ADC circuit. The block diagram of the proposed design is illustrated as Fig. 1.

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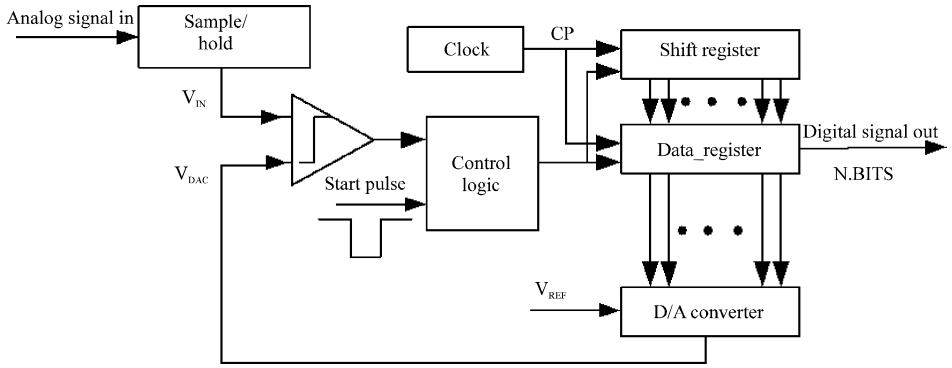

Fig. 1: Block diagram of a typical SAR ADC module

In Fig. 1, the analog signal is sampled by the Sample/Hold circuit; its output is send to an Op-Amp which constructs a comparator with respect to the second input as the ADC output. Then the SAR Control Logic reacts upon the output of the Comparator and sends out the corresponding signal to the related registers. It forms the new input of the ADC. Finally, after N cycles of system clock the conversion is finished and the converted data is exported (Sauerbrey *et al*., 2003). At the beginning of the process, the 8-bits data register is set as 10000000 with MSB equals to 1. The output of the DAC is set as half of the reference voltage V_{REF}. In the following, if the input voltage V_{IN} is smaller than V_{DAC}, then the comparator outputs a logical low voltage, the MSB of the data register is set to 0. Conversely, if V_{IN} is greater than V_{DAC}, then the comparator outputs a logical high voltage, the MSB of the data register is kept as 1. At the end of this process, the control logic of the SAR is moved to the next bit. When the LSB is reached, it indicates that a conversion cycle is finished and then the output is stored into the data register. The detail design of the main sub-systems is stated in the following section.

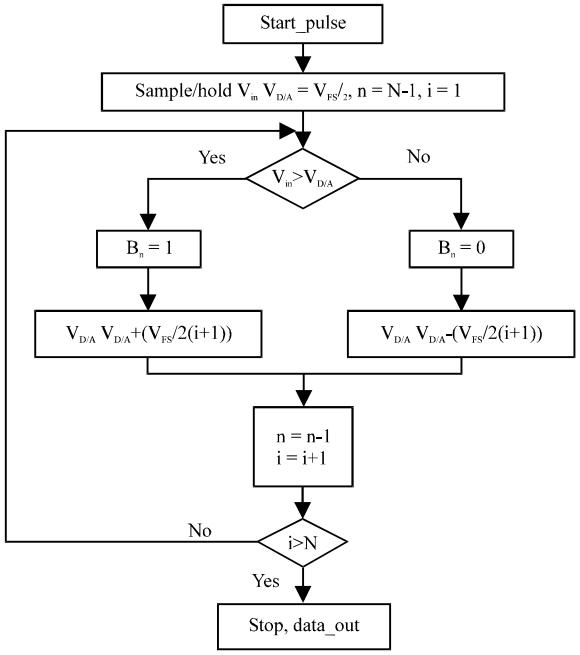

Fig. 2: SAR algorithm proces

SUB-SYSTEM DESIGN

SAR control logic circuit design: The design of the SAR Control Logic circuit is based on the successive approximation algorithm which is programmed by using the Verilog HDL language. Finally the gate-level netlist, timing constrains file and standard delay file is obtained by using a synthesis tool, Synopsys DC. The simulation is performed with the gate-level delay file. At the first, the follow chat of the successive approximation algorithm is detailed in Fig. 2 (Azin *et al*., 2011).

In Fig. 2, the start pulse sending a control signal to the Control Logic, this initiates the Control Logic to handle the compared result which is sent by the Comparator. If the sampled voltage V_{in} is greater than the V_{DAC}, then the results of the comparator Bn is set to 1, the new value of V_{DAC} (new)is produced by:

$$V_{DAC}(new) = V_{DAC} + \frac{V}{2} \quad (1)$$

Otherwise, the new value of V_{DAC} (new) is calculated as:

$$V_{DAC}(new) = V_{DAC} - \frac{V}{2} \quad (2)$$

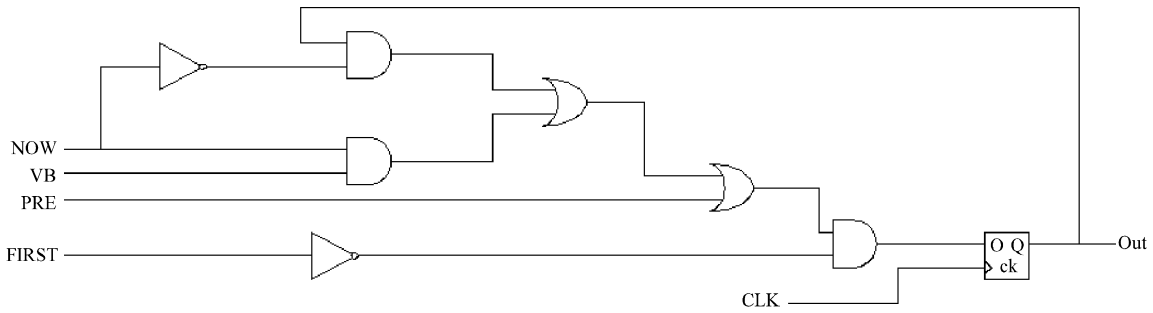

Fig. 3: A unit circuit of SAR logic

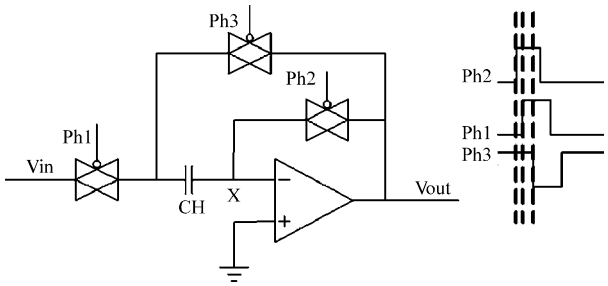

Fig. 4: Schematic design of the sample/hold circuit with its clock phase

where, V_{FS} is $(1-1/2^N)V_{REF}$. After that, the calculation is moved to the next bit until the LSB is confirmed and the whole conversion is finished (Zhu *et al*., 2010). The gate-level circuit of such algorithm is produced by using a synthesis tool based on the stated algorithm. A unit circuit of the SAR Logic circuit is demonstrated as Fig. 3.

In Fig. 3, when the transition begins, the value of the pin "FIRST" is initialized as "1", the output pin "OUT" is cleared to "0". "PRE" is set as "1". At the time when the n^{th} bit is converting, "PRE" pin is set to "1" and "OUT" is preset to "1". At the following clock circle, "PRE" changes to "0", "NOW" is set to "1" and the output is changed with respect to the value of "VB". At one clock circle after, "NOW" pin is changed to "0" and the output is kept as unchanged (Katyal *et al*., 2006).

Sample/hold circuit design: As introduced early that the Sample/Hold circuit is to sample the input signal. The schematic design of the proposed Sample/Hold circuit is illustrated as Fig. 4.

As illustrated in Fig. 4, the proposed Sample/Hold circuit is based on a capacitive feedback structure with three switches to control the sampling and amplifying status. As shown in the right hand side of Error! Reference source not found., within in a sampling period, the first and second switches, Ph1 and Ph2 are switched on while the third switch, Ph3 is set off. The potential at point "X" is approximately set as 0 at this time instance and the potential at the left hand side of the capacitor is same as V_{in}. When the third switch is on, the first and second switches are set off, the circuit becomes a capacitive feedback circuit with the potential of V_{out} is same as V_{in} and this potential is hold until the end of the this sampling period. In order to reduce the influence of charge injection when the switch is closed, there are slit delays between first and second switch when they are switched on and third switch when it is switched off.

Comparator circuit design: Figure 5 shows the proposed design of the Comparator circuit which is similar as an operational amplifier. The input stage of the comparator uses a folding cascode structure and the output stage employs a common-source PMOS transistor. The open-loop structure simplifies the comparator circuit design and reduces the size of the overall system without reduce its performance. Furthermore, it does not need to compensate the comparator with such open-loop design, this leads to a wider bandwidth and faster reaction time.

DAC circuit design: Figure 6 shows the implementation of the N-bit DAC circuit used in the proposed SAR ADC circuit with N = 8. The right hand side of the diagram is a matched R-2R resistor network combined with a current mirror structure. The left hand side is a voltage-to-current converter; it has a negative feedback operation amplifier with a PMOS transistor to stabilize the current of the current mirror. This eliminates current variation caused by the fabrication process error and temperature deviation. It also reduces the level of consistency for the resistors used by the R-2R matched network. This means that the distortion level of the resistor can be lifted as soon as the distortion is in a linear faction which is true factor for the present fabrication process technology used in the industry.

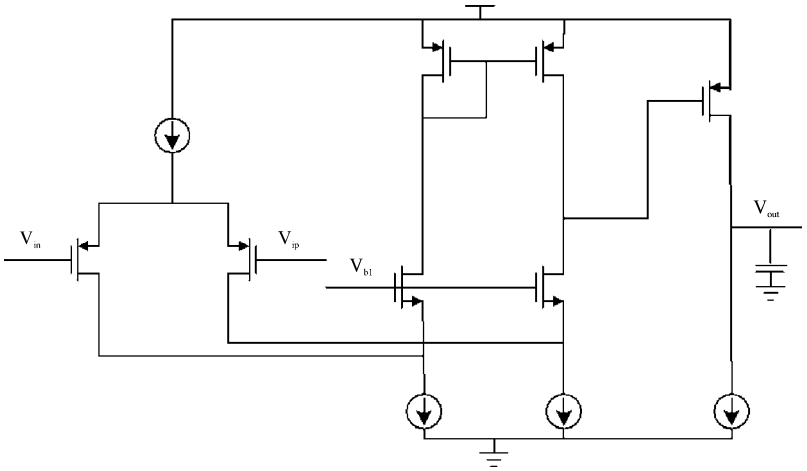

Fig. 5: Comparator circuit design

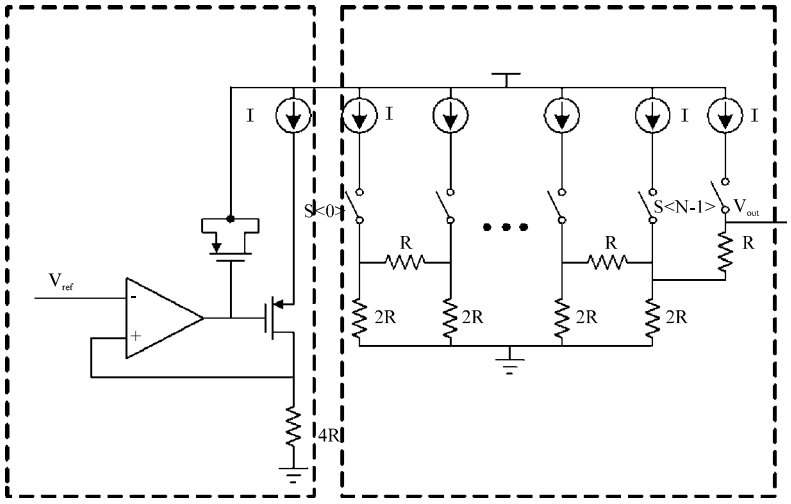

Fig. 6: Circuit design for a N-bit DAC (N = 8 in this article)

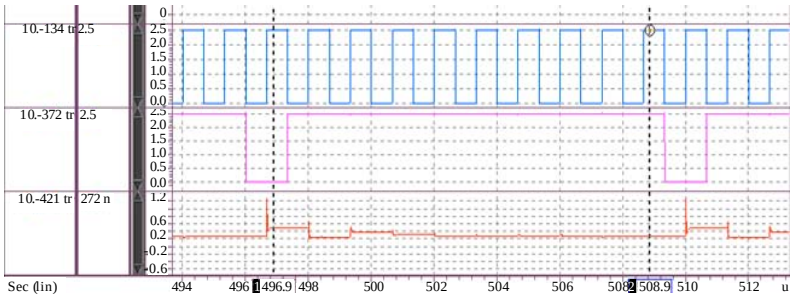

Fig. 7: Conversion process for input voltage at 273 mV

SIMULATION AND TEST RESULTS

With the designs introduced in the previous sections, the simulation of the proposed design is performed by using the EDA tool of cadence spectre. The simulation results are illustrated at Fig. 7.

Figure 7 illustrates the conversion process at an input voltage is set as 273 mV. The first plot indicates the

system clock. The second plot shows the starts control signal for the conversion, the conversion time finishes at the changing of the LSB finishes. The third plot represents the conversion process. It starts at a voltage level which is half of the reference level V_{REF}. The conversion period equals ten times of the system clock cycle with a 90% of pulse width. This arrangement effectively reduces the AD conversion time. The spike at each of the beginning conversion point is caused by circuit's setting up time. It settles in a time period of less than 0.05 us and does not affect overall performance of the conversion.

Figure 8 shows the simulation results from the Sample/Hold circuit. The first plot indicates the input

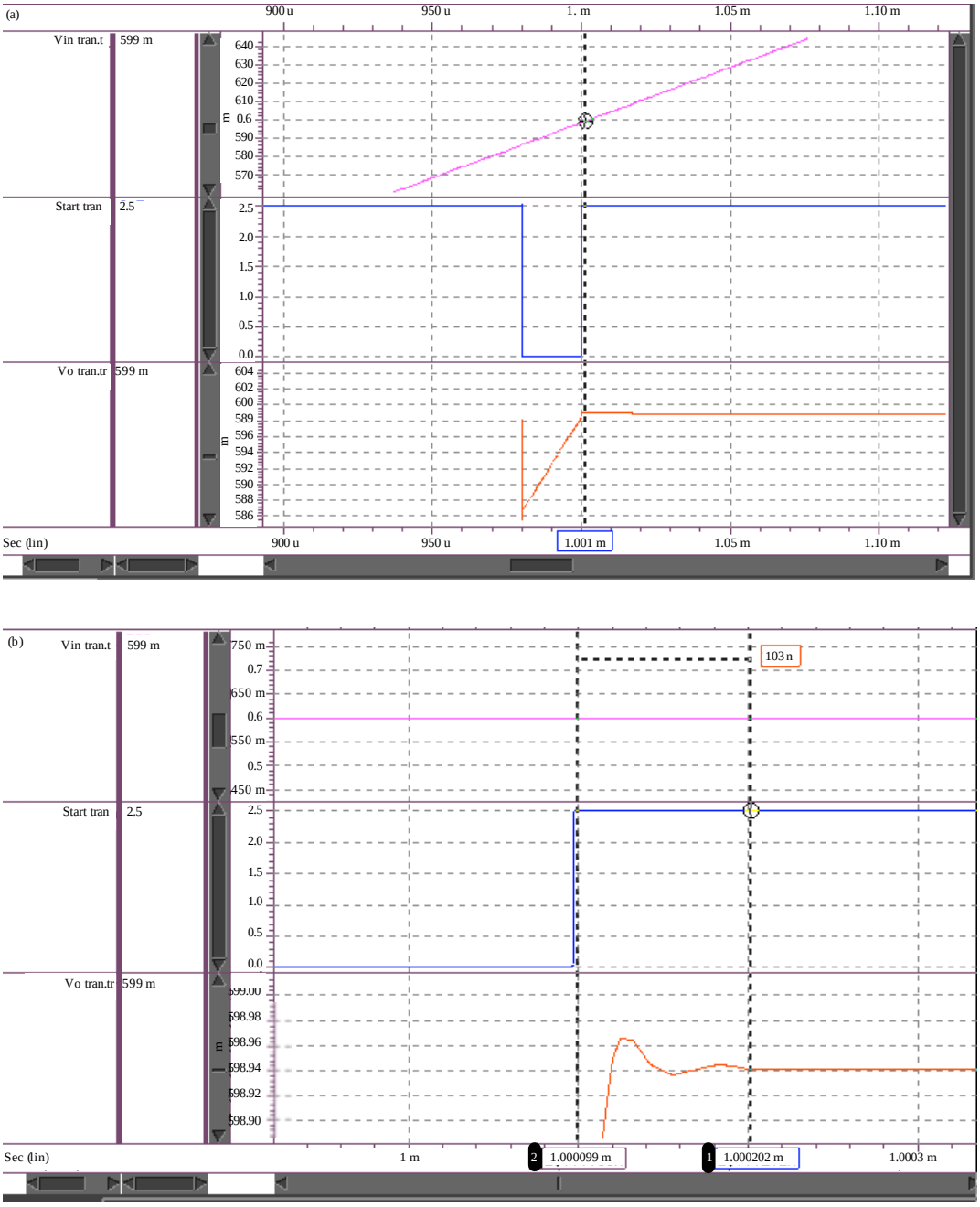

Fig. 8(a-b): Simulation results for the sample/hold circuit

voltage and the third line is the output voltage plot. The second plot at the middle of the figure is the system clock. The input voltage is 599 mV at the time of the sampling is finished. At the hold period, the output voltage remains 599 mV without any change. It clearly illustrates that the output is continuously following the input voltage during the sample/hold period with a settling time for the output is around 100 n sec which is an important factor that limits the system clock frequency. However, the designed system period in this study is 1 μ sec; it is therefore the comparison can be done after the output voltage has been settled. The tested results for the proposed design are demonstrated in the following by using a NI PXI testing system (Fig. 9-10).

In Fig. 11 and 12, the DNL and INL of the proposed SAR ADC module are illustrated. The maximum DNL error

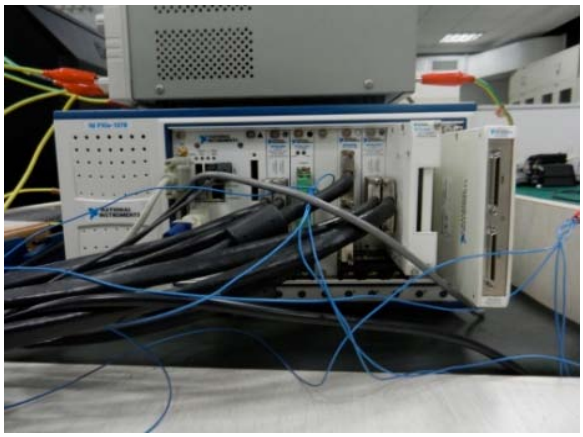

Fig. 9: PXI testing system

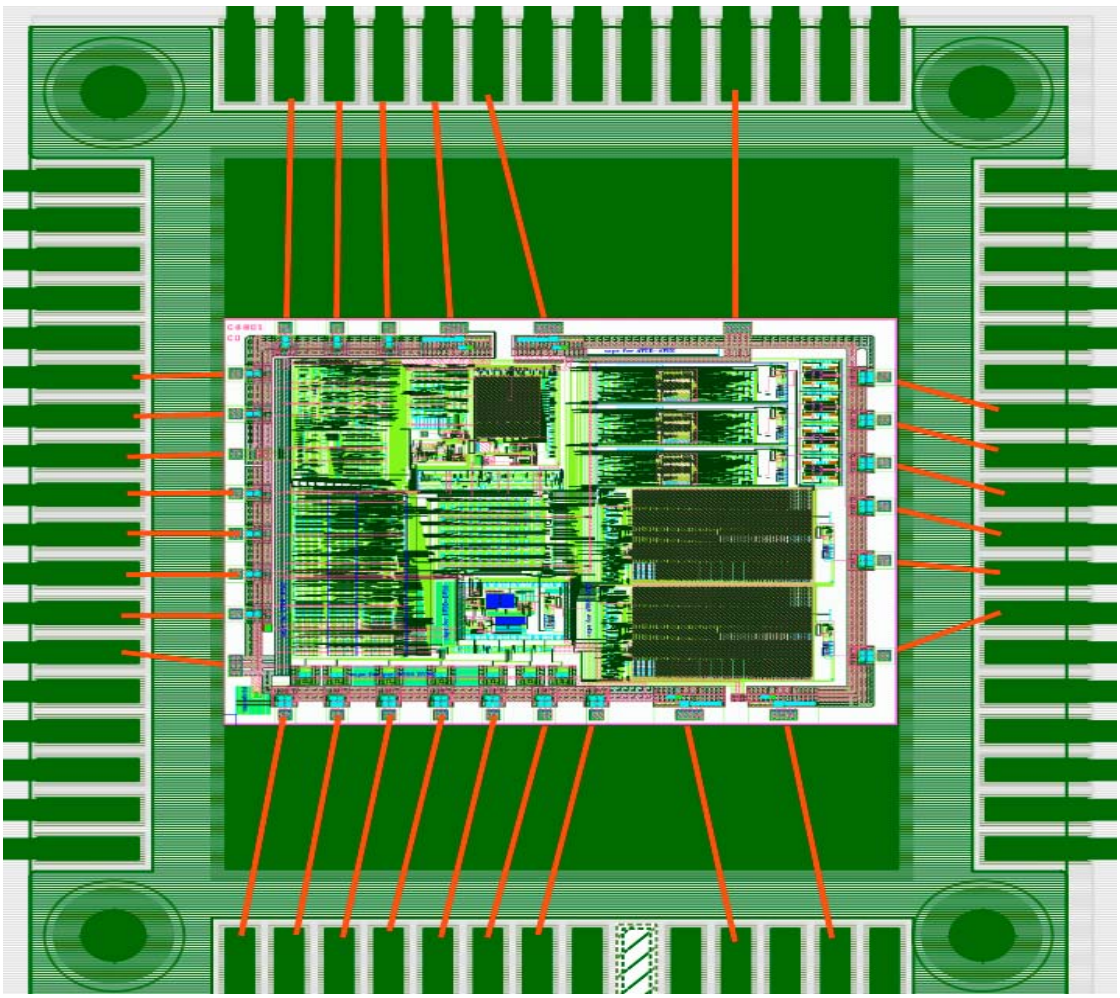

Fig. 10: Circuit board of testing system

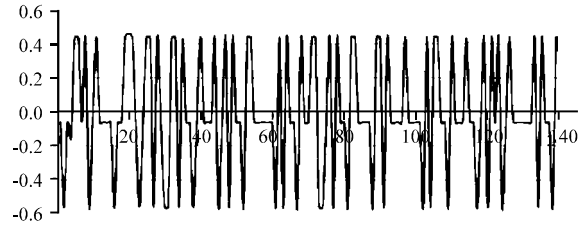

Fig. 11: Tested DNL result for the proposed SAR ADC module

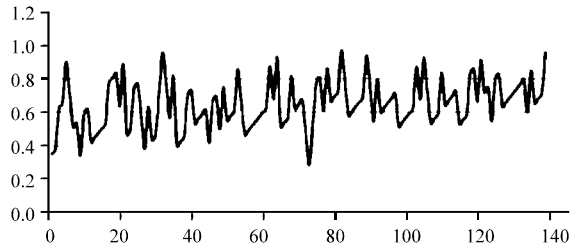

Fig. 12: Tested INL result for the proposed SAR ADC module

is around 0.5 LSB which is evenly distributed around the horizontal axis. It indicates that the output variation of the ADC is around its mean value. Its INL error is less than 1 LSB.

CONCLUSION

In conclusion, a novel AGC structure and SAR ADC module are introduced for the application of a satellite communication receiver channel. The AGC structure has the advantages of linear step. In order to improve the system clock frequency, the accuracy of the DAC conversion results and reduce the overall size of the AGC circuit, a novel SAR ADC is detailed. The simulation results demonstrate that the proposed SAR ADC circuit is able to achieve a high precision performance. The tested results echoes the simulation with a DNL error around 0.5 LSB and INL error less than 1LSB.

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