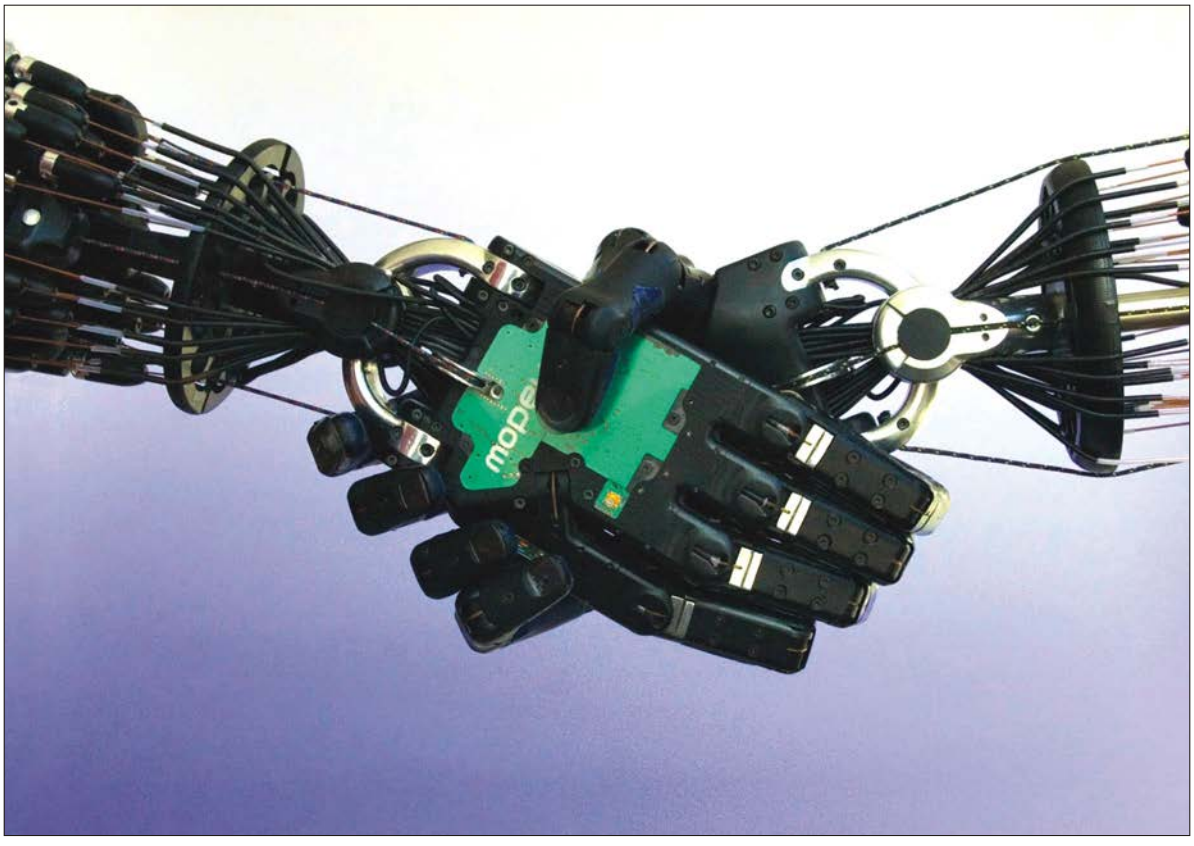

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Achieving Low Power Test Pattern By Efficient Compaction Method For SoC Design

[1]S. Saravanan and [2]Har Narayan Upadhyay
[1]School of Computing, [2]School of Electrical and Electronics Engineering, SASTRA University, Thanjavur-613401, India

Corresponding Author: S. Saravanan, School of Computing (SOC), SASTRA University, Thanjavur-613401, India Tel: +00919842569532

ABSTRACT

Present System-on-Chip (SoC) contains various design models and all the design components are integrated into single Integrated Chip (IC). Thus total volume of SoC test pattern is also growing in complex manner. This huge test pattern also invokes various challenges in switching power, memory space and accessing time. The problem on huge test pattern involved for scan based testing is focused in this research. Coloring algorithm is proposed to compact test pattern. Utilization of unspecified test pattern promises more compaction in coloring algorithm. This proposed method never contains any extra silicon area overhead. Due to this advantage, proposed technique is more suitable for reduction of test pattern. An experimental result produces significant reduction in above said problems and tested with ISCAS89 benchmark circuits.

Key words: Test pattern, compaction, coloring algorithm, scan based design

INTRODUCTION

System on Chip (SoC) is continuously growing in its feature size to follow Moore's law. This rule states that every one and half year, the total size of the chip gets doubled. This rule directly increases huge test pattern, memory space, accessing time and cost. The cost of the manufactured chip testing in the semiconductor industry is totally depends on huge test pattern. Thus all above said challenges can limit the design reliability. So it is necessary to reduce test pattern. Scan based testing of sequential circuits is also major challenges for SoC testing.

All primary input contains the combination of '0', '1' (specified) and 'X' (unspecified) bit. This makes the test pattern to identify whether the given test pattern is in specified bit or unspecified bit. Specified bits are defined by '0' and '1' combination and in unspecified bits, only 'X' is identified. These unspecified bits are more in test patterns compared with specified bits. This will approximately close to 99% of unspecified test pattern bits. Every unspecified bit is considered to be specified by assigning random values of '0' and '1', leading to uncompacted test pattern in scan based design. Obtaining the minimal number of test set is the ideal goal of test compaction. All stuck at faults in the design are detected by these feasible compacted test patterns. Higher compacted test sets are very economical even with the extra test set. Test pattern size is directly involved to the cost, storage and test accessing time and hence, this testing problem is activated more in the scan designed circuits (Wunderlich and Zorian, 1997).

Two types of test compaction techniques are classified broadly. They are static and dynamic compaction. In compaction of static test, the number of test patterns was minimized after they are minimized during the process of ATPG in dynamic test compaction.

The problem of reducing test pattern for SoC has been attended from several recent literatures. Many techniques for reducing test patterns are summarized by Touba (2006). Most of the work has been focused on compression of test data for general scan testing (Chandra and Chakrabarty, 2001, 2003; El-Maleh and Al-Abaji, 2002; El-Maleh, 2008; Jas *et al*., 2003; Nourani and Tehranipour, 2005; Tehranipour *et al*., 2005). Many of these techniques observed to reduce test pattern to save memory cost and to advance the functionality of Automatic Test Equipment (ATE) transmission. Static test compaction algorithms and its various categories are discussed in El-Maleh and Osais (2003).

Redundant vector elimination and vector test vector reordering with fault simulation is observed in Boateng *et al*. (2001). Merging of compatible test vectors based on test relaxation or raising is shown in Miyase *et al*. (2002). Removing some of the already existing test vectors for compaction is identified in Kajihara *et al*. (1994). Static compaction techniques are preferred more than dynamic compaction for several reasons (El-Maleh and Khursheed, 2007; Lin *et al*., 2001). Circular-scan based architecture (Azimipour and Eshghi, 2008) is used to select several scan chains in parallel approach with help of multiple hot decoders. Scan insertion and scan stitching is performed with Register Transfer Level (RTL) coding style, which is discussed by Reaz *et al*. (2009). In this work scan flops are considered as don't use during synthesis process and results with cost reduction. Traveling Salesman Problem (TSP) with hybrid ant colony algorithm and genetic algorithm is presented by Shang and Zhang (2012) to solve power dissipation in test vector.

This shows reduced test pattern in compaction manner. Huge test pattern is compacted with full fault coverage. Uncompacted test pattern with unspecified test patterns in random value will increase the complexity of test pattern. Thus this shows the proportionality to the storage access time of the scan design.

PROPOSED TECHNIQUES

Graph theory based coloring algorithm can be used to replace the unspecified bit to corresponding specified bit as '0' or '1'. Undirected graph, which is also called as conflict graph G (V, E) is built for test pattern cubes. This test pattern cube is considered as vertices and link between two vertices as edges. In a test cube in G, an edge can connect two vertexes only if two test cubes patterns are conflict to each other (adjacent vertices are not of same color). The value of the conflict graph is 1, then it represents that those two vertices are not compatible patterns of test cubes. Conflict graph can be plotted using conflict table, only if a conflict occurs and an edge can be formed between a pair of vertices. In such cases, the vertices will be differentiated by coloring. Proposed work is based on Welsh and Powell (1967) coloring algorithm as shown in steps given below:

Input: Chosen test vector

Output: Compacted test vector

(1) Sort the vertices in decreasing order of degree and initially have every vertex uncolored

(2) Traverse the vertices in order, giving a vertex color 1 if it is uncolored and it does not yet have a neighbor with color 1

(3) Repeat this process with colors 2, 3, etc. until no vertex is uncolored

Normal test pattern for ISCAS89-S27 design circuit is given in Table 1. It contains 16 Test Patterns (TP) each with 7 bit. Its corresponding final compacted test pattern is shown in Table 2. It shows 7 Compacted Test Patterns (CTP) each with 7 bit.

Table 1: Normal test pattern of S27 circuit

TP							
1	1	X	X	0	X	1	0
2	0	X	X	0	X	1	0
3	X	1	0	X	0	X	X
4	X	0	0	X	1	X	X
5	X	0	0	X	0	X	X
6	X	1	1	X	X	X	X
7	X	X	1	X	X	1	X
8	X	0	X	1	0	0	0
9	X	1	X	1	X	0	0
10	0	X	X	0	X	0	0
11	0	X	X	X	X	1	1
12	X	0	X	0	0	0	0
13	1	X	X	X	X	X	1
14	0	X	X	X	X	X	X
15	0	X	X	X	X	X	1
16	1	0	X	1	0	X	0

Table 2: Compacted test pattern (CTP) of S27 circuit

CTP							
1	0	1	0	X	0	1	1
2	0	1	1	0	X	1	0
3	1	0	0	0	1	1	0
4	1	X	X	X	X	X	1
5	0	0	0	0	0	0	0
6	X	1	X	1	X	0	0
7	1	0	X	1	0	0	0

Due to large amount of don't care values, it is compacted with proper known value. There is no loss in fault coverage due to this proposed compaction method. This is one of the main advantages when using compaction method in given test cubes. One more advantage of compaction technique is reduced area overhead. Proposed technique never increases silicon area. Thus this advantage gives more comfortable in reduction of test pattern. Scan based test pattern is considered for this proposed work.

RESULTS

This section describes the experiment performed to asses the efficiency of achieving low test pattern based on compaction method. The proposed method is implemented using VHDL and tested with full scan design of ISCAS89 circuits. Test patterns used in these experiments are obtained by using Mintest (Hamzaoglu and Patel, 1998) and TetraMax from Synopsys tools. All the provided test patterns target at 100% fault coverage. The Compaction Ratio (CR) is computed by equation:

$$CR = \frac{\text{Total No. of data bits reduced}}{\text{Total No. of original data bits}}$$

Table 3 shows compaction results of various ISCAS89 circuits. Various columns are tabulated having pattern number, pattern length, original test patterns bit, percentage of unspecified bit ratio

Table 3: Proposed test pattern compaction ratio (CR) results

Circuits	Pattern number	Pattern length	Original test patterns bit	Unspecified Bit (%)	CR (%)
S510	132	25	3300	74	47.72
S838	254	66	16764	77	50.78
S1423	514	91	46774	93	86.77
S5378	1291	214	276274	96	89.07
S9234	1621	247	400387	95	89.82
S15850	3634	611	2220374	99	95.30

Table 4: Proposed test pattern results compared with various existing methods in (%)

	Compression ratio (%)								
Circuits	Chandra and Chakrabarty (2001)	Chandra and Chakrabarty (2003)	El-Maleh and Al-Abaji (2002)	El-Maleh and Osais (2003)	Jas *et al.* (2003)	Nourani and Tehranipour (2005)	Tehranipour *et al.* (2005)	Tseng and Lee (2010)	Proposed results
S5378	37.11	50.77	54.98	51.93	55.10	53.75	51.64	54.63	89.07
S9234	45.25	44.96	51.19	45.89	54.20	47.59	50.91	53.20	89.82
S15850	62.82	65.83	69.49	67.99	66.00	67.34	66.38	69.99	95.30
Average	48.39	53.85	58.55	55.27	58.43	56.22	56.31	59.27	91.39

and compacted pattern ratio. The percentage of unspecified bit ratio is found to be increasing form 74 to 99% for various circuits as in column five in the given Table 3 and percentage of compacted pattern ratio (CR) ranges from 47 to 95%. In Table 4 proposed results are tabulated for various ISCAS89 benchmark circuits compared with various existing test pattern compression results. Proposed results vary from 89 to 95% in compression of test patterns. Averages of various existing methods are compared with proposed results and the proposed result show significant values.

CONCLUSION

The present challenge of reducing test pattern is one of the most important tasks for reduction in SoC test pattern. It is very particularly identified in the field of scan based sequential patterns. This paper proposes about compaction technique for minimizing test patterns. This is achieved by coloring algorithm and it reduces scan based test pattern in significant manner. Experimental result shows that average test pattern is reduced significantly up to 91%. This also promises minimized memory storage and accessing time issues, due to direct proposition with compacted test pattern.

REFERENCES

Azimipour, M. and M. Eshghi, 2008. Parallel circular-scan architecture. J. Applied Sci., 8: 2083-2090.

Boateng, K.O., H. Konishi and T. Nakata, 2001. A method of static compaction of test stimuli. Proceedings of the 10th Asian Test Symposium, November 19-21, 2001, Kyoto, Japan, pp: 137-142.

Chandra, A. and K. Chakrabarty, 2001. System-on-a-Chip test data compression and decompression architectures based on Golomb codes. IEEE Trans. CAD of Integr. Circuits Syst., 20: 355-368.

Chandra, A. and K. Chakrabarty, 2003. A unified approach to reduce SOC test data volume, scan power and testing time. IEEE. Trans. Comput. Aided Des. Integrat. Circ. Syst., 22: 352-363.

El-Maleh, A. and S. Khursheed, 2007. Efficient test compaction for combinational circuits based on fault detection count-directed clustering. IET Comput. Digit. Techniques, 1: 364-368.

El-Maleh, A.H. and R.H. Al-Abaji, 2002. Extended frequency-directed run length code with improved application to system-on-a-chip test data compression. Proceedings of the 9th International Conference on Electronics, Circuits and Systems, Volume: 2, September 15-18, 2002, Dubrovnik, Croatia, pp: 449-452.

El-Maleh, A.H., and Y.E. Osais, 2003. Test vector decomposition based static compaction algorithms for combinational circuits. ACM Trans. Design Automat. Electron. Syst., 8: 430-459.

El-Maleh, A.H., 2008. Efficient test compression technique based on block merging. IET Comput. Digital Tech., 2: 327-335.

Hamzaoglu, L. and J.H. Patel, 1998. Test set compaction algorithms for combinational circuits. Proceedings of the International Conference on Computer-Aided Design, November 8-12, 1998, San Jose, CA., USA., pp: 283-289.

Jas, A., J. Ghosh-Dastidar, M.E. Ng and N.A. Touba, 2003. An efficient test vector compression scheme using selective huffman coding. IEEE Trans. Comput. Aided Des. Int. Circuits Syst., 22: 797-806.

Kajihara, S., I. Pomranz, K. Kinoshita and S.M. Reddy, 1994. On compacting test sets by addition and removal of test vectors. Proceedings of the 12th IEEE VLSI Test Symposium, April 25-28, 1994, Cherry Hill, NJ., USA., pp: 202-207.

Lin, X., J. Rajski, I. Pomeranz and S.M. Reddy, 2001. On static test compaction and test pattern ordering for scan designs. Proceedings of the International Test Conference, October 30-November 1, 2001, Baltimore, MD., USA., pp: 1088-1098.

Miyase, K., S. Kajihara and S.M. Reddy, 2002. A method of static test compaction based on don't care identification. Proceedings of the 1st IEEE International Workshop on Electronic Design, Test and Applications, January 29-31, 2002, Christchurch, New Zealand, pp: 392-395.

Nourani, M. and M. Tehranipour, 2005. RL-huffman encoding for test compression and power reduction in scan application. ACM Trans. Design Autom. Electron. Syst., 10: 91-115.

Reaz, M.B.I., W.F. Lee, N.H. Hamid, H.H. Lo and A.Y.M. Shakaff, 2009. High degree of testability using full scan chain and ATPG-An industrial perspective. J. Applied Sci., 9: 2613-2618.

Shang, J. and L. Zhang, 2012. Ant colony algorithm and genetic algorithm optimization for test vector reordering inform. Technol. J., 11: 1786-1789.

Tehranipour, M., M. Nourani and K. Chakrabarty, 2005. Nine-coded compression technique for testing embedded cores in SoCs. IEEE Trans. Very Large Scale Integr. Syst., 13: 719-731.

Touba, N.A., 2006. Survey of test vector compression techniques. Des. Test Comput. IEEE, 23: 294-303.

Tseng, W.D. and L.J. Lee, 2010. Test data compression using multi-dimensional pattern run-length codes. J. Electron. Test, 26: 393-400.

Welsh, D.J.A. and M.B. Powell, 1967. The upper bound for the chromatic number of a graph and its application to timetabling problems. Comp. J., 11: 85-86.

Wunderlich, H.J. and Y. Zorian, 1997. Built-In Self Test (BIST) Synthesis of Self-Testable Systems. Kluwer Academic Publisher, The Netherlands.