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VLSI Based Combined Multiplier Architecture

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ABSTRACT

In this study, an efficient design of multiplier is been designed. Since multipliers are the basic component in most of the electronic devices. A combination of multiplier is proposed based on the certain parameters in which VLSI design should concentrates, such as area, speed and power. This combination of multipliers is composed of two parts one is carry save array multiplier which concentrates in power dissipation by skipping the blocks when it is not needed. The second part is modified Booth Wallace tree multiplier which concentrates in the speed of the multiplier. This combination is found to produce better results in power and speed parameters resulting in an efficient multiplier design.

Key words: Multipliers, carry save array multiplier, modified Booth-Wallace tree multiplier, power, speed

INTRODUCTION

Now a days low power VLSI design is attracting all the electronic devices, since power became a major criterion in designing. Today almost all of the electronic devices are being used in battery backup for portability and comfort. This low power consumption will also helps in reduction of heat dissipation in such electronic devices resulting in wide and long use. Multipliers are used widely in digital signal processing applications. As accuracy is a main advantage of DSP applications, it relies on the power consumption. In power dissipation, dynamic power dissipation occurs mainly due to switching activity of the transistors in the circuit (Weste and Harris, 2005). This dissipation can be reduced to a great extent by avoiding unwanted ON and OFF of the transistors. Researchers are working hardly on reducing the power consumption and dissipation, to improve the efficiency of the circuits. In such way, it is derived that skipping of unwanted blocks or components in the circuits may result in reduction of both power consumption and dissipation. By skipping or bypassing certain blocks while it is not needed (Di and Yuan, 2003). If power dissipation increases, it will increase the heat dissipation which results in the need of proper cooling setup to make the circuit work properly.

This skipping technique can give better results when it is used in array multipliers. As array multipliers will have a regular layout structure and it is easy to implement. The combination of multipliers been specified as Carry save array multiplier and Modified booth Wallace tree multiplier (Marimuthu and Thangaraj, 2008; Lakshmanan *et al.*, 2002; Wallace, 1964). In which transmission gates are used in array multiplier which provides much efficiency and power advantage. Modified booth been chosen because of its great speed advantage and the reduced partial products.

ARRAY MULTIPLIER

In array multipliers, partial products are produced in parallel and they are accumulated using a final adder to produce the final result. It has a regular layout structure and wiring. Therefore, it takes less area to implement. Array multipliers have linear circuit delay (Weste and Harris, 2005). It has a dense layout which is more suitable for fabrication. Here, carry save array multiplier is been used. In carry save array multiplier, the multiplication is done in vector form as shown in Fig. 1.

It consists of a partial product tree which posses the capability of reducing the partial product bits. To sum up all those partial products, a final chain of adder is used. The input is given in the following order as: $(x_{m-1}, \dots, x_2, x_1, x_0)$ and $(y_{n-1}, \dots, y_2, y_1, y_0)$.

Each full adder performs multiplication of a single bit. While taking a brief study of the function of each full adder, all full adders will be in working state even the inputs are '0'. This will increase the power consumption by making use of full adders whose output has no value. These full adders can be skipped passing the previous value to the next level of adders without using full adders as shown in Fig. 2. This technique will reduce the switching activity. This switching activity can be reduced by skipping blocks of logic using transmission gates.

In sequential circuits, large block of the circuit can be isolated using clock gating technique. (Economakos and Anagnostopoulos, 2006) noted that, clock gating in a pipelined array multiplier.

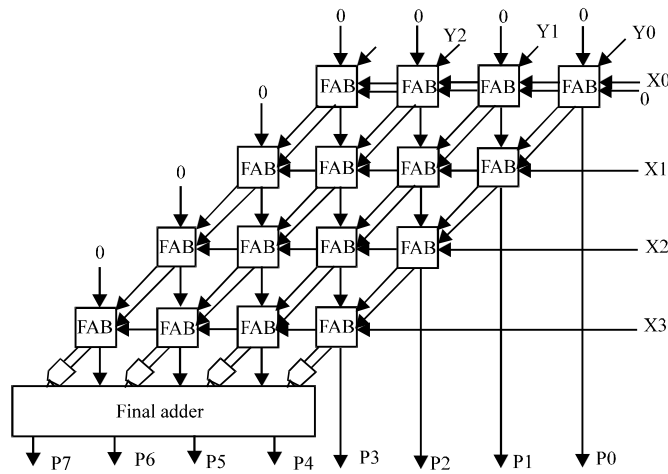


Fig. 1: Carry save array multiplier

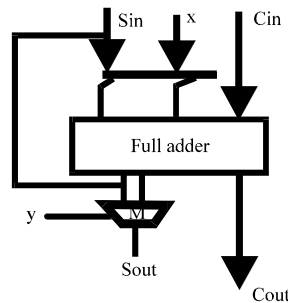


Fig. 2: Bypassing cell (FAB)

In combinational circuits, gating tree should be rearranged in order to provide a more profitable isolation technique. Here transmission gates are used for isolation which appears to consume less power than other gates. Therefore, it can provide low power consumption. Using this transmission gates combined with array multiplier, it will reduce power up to 50%. There are many such bypassing or skipping techniques (Wang and Sung, 2009; Di and Yuan, 2003) have been proposed earlier.

MODIFIED BOOTH-WALLACE TREE MULTIPLIER

The combination of Modified booth encoder (Marimuthu and Thangaraj, 2008) and Wallace tree multiplier (Lakshmanan *et al.*, 2002; Wallace,1964) will reduce overall multiplication time. The Modified Booth-Wallace tree Multiplier block diagram is shown in the Fig. 3.

In modified booth encoder, the multiplier bits are encoded which leads to the reduction of partial products. These are added by the summation part of the Wallace tree multiplier (Karlsson, 2000). By using Modified booth algorithm, area will be reduced and better delay performance can be achieved by the usage of Wallace tree adders.

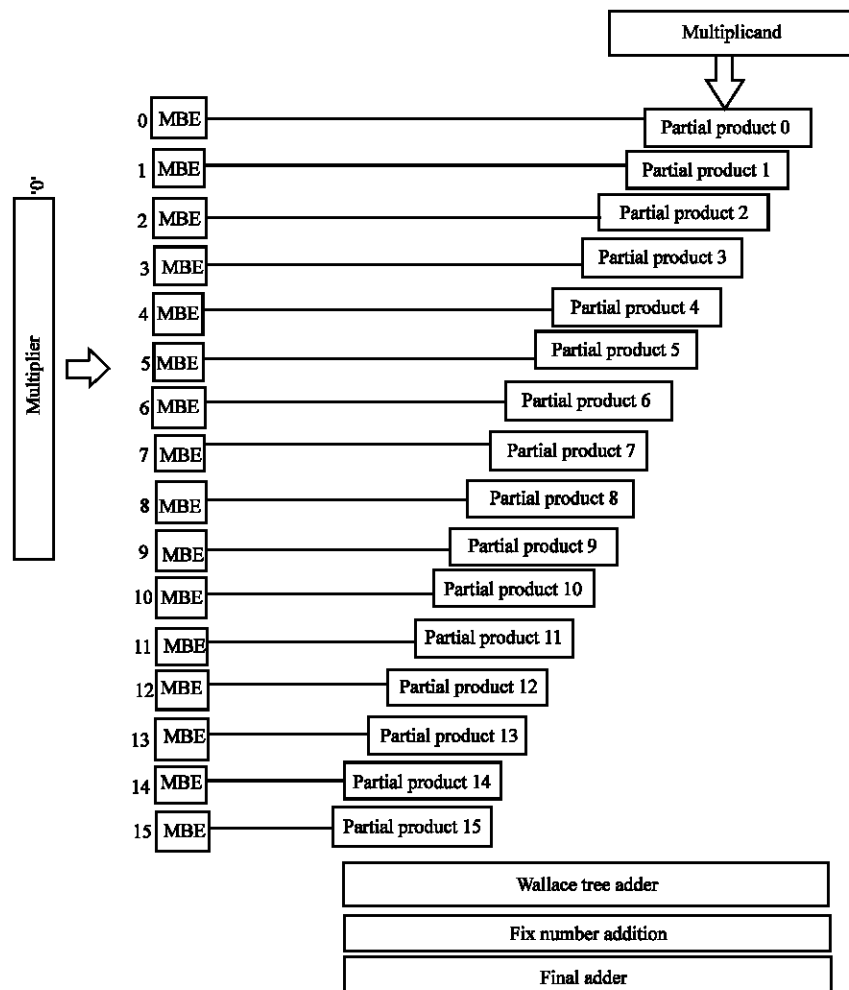


Fig. 3: Modified Booth-Wallace tree multiplier

The two's complement of the binary number can be denoted as:

$$A = (-2^{M-1} a_{M-1} + \sum^{M-2} a_i 2^i)$$

Equivalent base 4 sign digit is represented as:

$$A = \sum^{(M/2)-1} d_i 4^i$$

MacSorley (1961) stated that, "In Modified booth encoding, each three consecutive bits of the multiplier operand are grouped as A_{2n+1} , A_{2n} , A_{2n-1} ($n=0,1,2,\dots,N/2-1$) and recoded using 'd_i' in the booth recoding table shown in Table 1 in order to produce the partial products". Devise summary is presented in Table 2 and multiplier comparison is shown in Table 3.

The multiplier 'A' is appended by '0' at the LSB. Then, these are added using the Wallace tree adders i.e., the addition is taken place in column wise using 3:2 compressors and half adders. All the partial products, P_n 's are added. There will be $N/2$ partial products. The P_{n+1} th partial product will be shifted two bits left from the P_n th. The sign extension sum can be precalculated using the following formula. For this, a fixed number should be added to the result i.e., $(-1) (2n-1)/3$.

$$\begin{aligned} \text{Sign extension} &= \sum^{(M/2)-1} (-1) 2^{2N} 4^i \\ &= 2^N (-1) (2^{M-1})/3 \end{aligned}$$

Delay is less therefore it will be faster in producing the results. The area-delay product and area-delay square product are observed to be better performed in this combination.

Table 1: Modified booth recoding

A _{2n-1}	A _{2n}	A _{2n+1}	d _i
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	2
1	0	0	-2
1	0	1	-1
1	1	0	-1
1	1	1	0

Table 2: Device utilization summary

Logic utilization	Estimated value		
	Used	Available	Utilization(%)
No. of slice registers	179	93120	0
No. of slice LUTs	10319	46560	220
No. of fully used LUT-FF pairs	179	10319	1
No. of bonded IOBs	128	240	53

Table 3: Comparison of multipliers

Multiplier type	Delay (nsec)	Power (μW)	Leakage power (μW)
Carry save array (bypassed)	20.923	155.601	0.10228
Modified booth	15.351	529.641	0.18785
Combined multiplier	14.493	455.054	0.10328

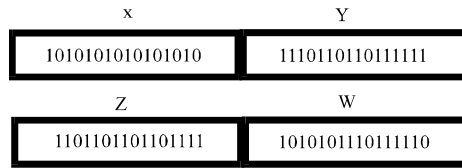


Fig. 4: Splitting of operands

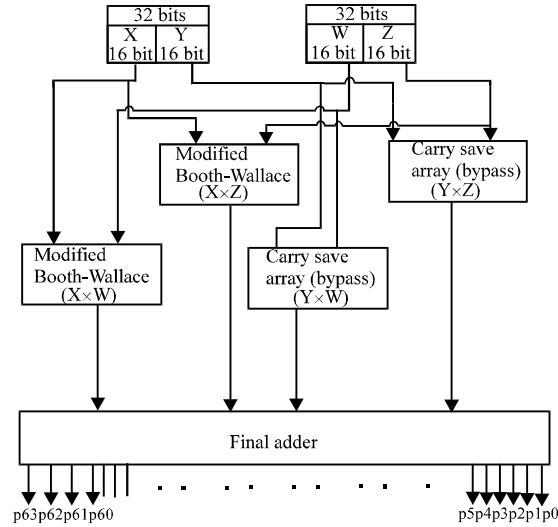


Fig. 5: Combined multiplier architecture

COMBINED MULTIPLIER ARCHITECTURE

The combined architecture of multiplier shown in Fig. 5 consists of Modified Booth Wallace tree multiplier which has its own timing efficiency and Carry save array multiplier with bypassing technique which has its power efficiency (Shah *et al.*, 2000).

The total numbers of operand bits are split into two halves i.e. the multiplier bits are split as X and Y and the multiplicand bits as Z and W as shown in Fig. 4.

These are fed into four multipliers as $X \times Z$, $Y \times Z$, $X \times W$, $Y \times W$ and their results are gained as:

- A = $X \times Z$, Which is gained from first Modified booth Wallace tree multiplier
- B = $Y \times Z$, Which is gained from first Carry Save Array Multiplier
- C = $X \times W$, Which is gained from second Modified booth Wallace tree multiplier
- D = $Y \times W$, Which is gained from second Carry Save Array Multiplier

In these, to gain more power efficiency the part with maximum number of zeros than 1's should be fed through the bypassed Carry save array multiplier i.e., the second part of the multiplicand bits (Y). To get the final result, the product of the each multiplier is obtained and these are shifted according to their positions and added. It is added as:

$$P = C \ll 32 + A \ll 16 + D \ll 16 + B$$

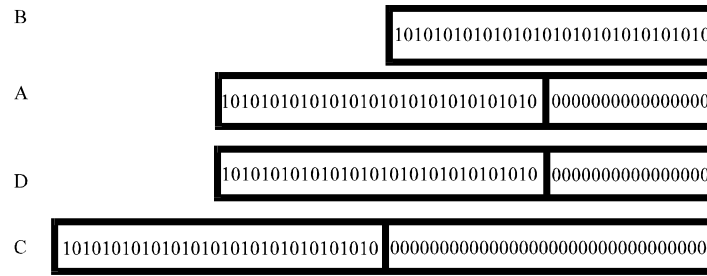


Fig. 6: Shifting and adding

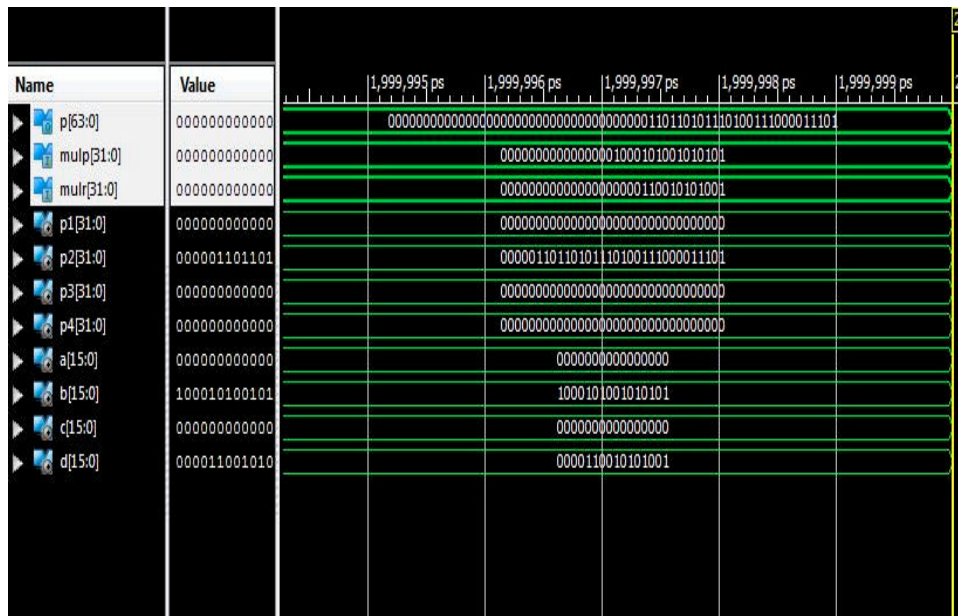


Fig. 7: Combined multiplier simulation

Example of shifting and adding is given in the Fig. 6.

Using the final adder, the shifted bits are being summed up and the final product bits are obtained.

The delay and the power consumed by this architecture is given as follows:

- **Delay timings:** 14.493 nsec
- **Power consumption:** 455.054 μ W

SIMULATION RESULTS

Thus the programs were simulated using tools like Modelsim and Xilinx. The output of the combined multiplier is given as simulation in Fig. 7.

The simulation result of Bypassed carry save array multiplier and modified Booth-Wallace multiplier is given in Fig. 8 and 9, respectively.

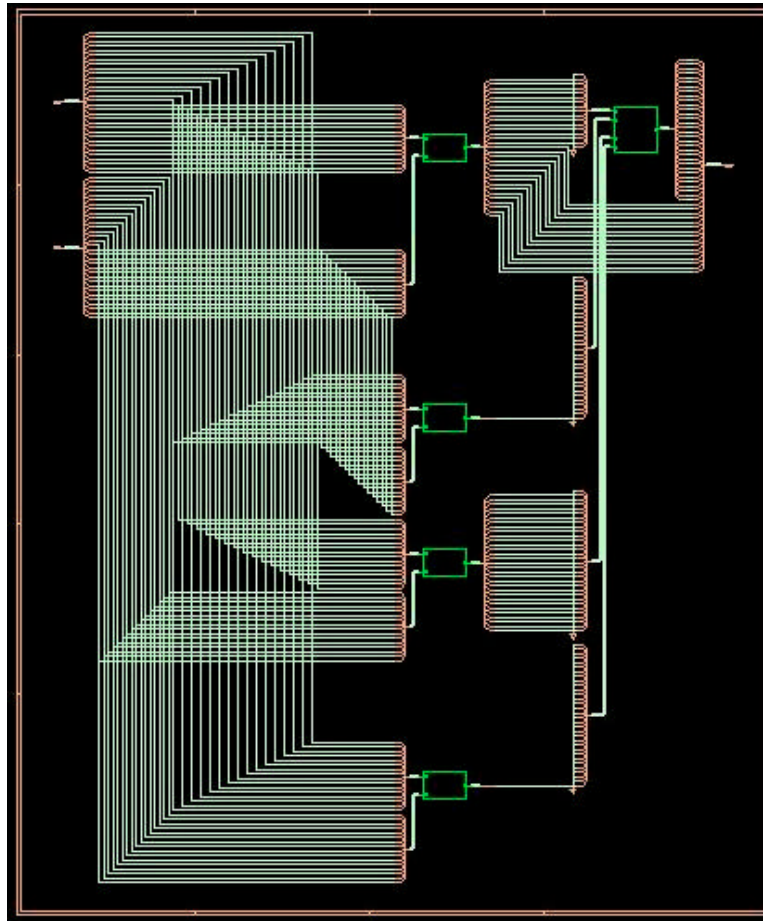


Fig. 10: Synthesis report of combined multiplier architecture

area for fabrication since it has combination of multipliers. The parts of this architecture are selected based on the performance parameters such as, speed, power and area efficiency. Therefore, this multiplier can be considered as efficient and further changes on the combination of multipliers with more advantages and change of technology will result in a better improvement in all parameters.

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