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A High Frequency CCII Based Tunable Floating Inductance and Current-mode Band Pass Filter Application

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Abstract: This study, introduced a new implementation of a CCII based floating inductance operating in class AB. In order to get tuneable characteristics of the proposed design, a translinear CCII configuration is used as a basic block owing to its high level of controllability. A frequency characterization of the translinear CCII is done. In order to optimize its static and dynamic characteristics, an algorithmic driven methodology is developed ending to the optimal transistor geometries. The optimized CCII has a current bandwidth of 1.28 GHz and a voltage bandwidth of 5.48 GHz. It is applied in the simulated inductance design. We first consider the conventional topology of the floating inductance based on the generalized impedance converter principle. Making use of controllable series parasitic resistance at port X in translinear CCII, we design tunable characteristics of the inductance. The effect of current conveyer's nonidealities has been taken into account. A compensation strategy has been proposed. It is based on the insertion of a high active CCII based negative resistance and a very low passive resistance. The proposed compensation strategy does not affect the inductance tuning process. In deed, both processes are controlled separately by means of two different currents. Simulation results show that the proposed inductance can be tuned in the range (0.45 μA-;57.4 μH). The simulated inductance has been applied in a fully integrated tunable high frequency band pass filter to illustrate the versatility of the circuit. The filter is electrically tunable by controlling the conveyer's bias current.

Key words: Active simulated inductance, second generation current conveyors, band pass filter, translinear implementation

INTRODUCTION

In recent years, the tremendous progress in CMOS technology and its increasing interest made it possible to manufacture complex and flexible VLSI chips. This creates a strong motivation to develop analog CMOS circuits performing complex functions. Second Generation Current Conveyers (CCIIs) are useful current-mode building blocks and many authors have demonstrated their versatility in CMOS analog circuit design[1-3]. Generalized impedance converter and inductance simulation are an important domain of application of CCIIs. In modern integrated circuit design, this fabrication is a complex task leading to a large occupation of silicon area. An inductance is usually connected in series, that is why a circuit that acts like a floating inductance instead of a grounded one can be more useful in analog design and doesn't show any particular constraints in general contexts of filter design. Previously reported implementations of active simulated inductance[4-6], have presented a fully integratable design but are either not tunable or limited in frequency domain. In this study, our interest is focused on tunable CCII based floating inductance covering high frequency range of operations.

Owing to the generalized CCII based impedance converter application, a simple capacitor can be converted into an active inductance which value is proportional to the capacitor and the parasitic resistances at port X of the corresponding CCIIs[4]. This principle can be applied in the simulation of either a grounded or a floating inductance. Tunable design can be obtained when we consider controllable CCII implementation. Many recent CCII configurations have been implemented in MOS technology[1,7,8]. Looking for class AB operations, design tunability and high frequency performances, the most suitable CCII configuration is the translinear one. In fact, the parasitic resistance at port X of a transilnear CCII can be tuned by a DC current in a great range of variations. Thus, we consider in this study the conventional translinear topology and optimize its static and dynamic

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performances acting on transistor geometries by applying an algorithmic driven methodology.

The effects of other CCII nonidealities (on port Y and Z) and their inference in the generalized impedance converter design are discussed. To reduce these effects, a compensating strategy is proposed. This solution makes use a low series passive resistance and a high active negative resistance.

DESIGN PRINCIPLE AND CCII NONIDEALITIES EFFECTS

In Fig. 1, a generalized impedance converter which performs a floating inductance simulation circuit is presented[4].

An ideal second generation current conveyor is a three-terminal versatile device (X, Y and Z). CCII Y and Z nodes are characterized by a high (ideally infinite) impedance level, while X node shows a low (ideally zero) impedance. Applying these properties on the design of Fig. 1, we get the inductance value between nodes IN and OUT as follows:

$$L_{eq} = R_1 R_2 C \tag{1}$$

An actual second generation current conveyor (CCII)[9] is characterized by the following relation between its port quantities:

$$\begin{pmatrix} I_Y \\ V_X \\ I_Z \end{pmatrix} = \begin{pmatrix} \dfrac{1}{R_Y // C_Y} & 0 & 0 \\ \beta & R_X & 0 \\ 0 & \alpha & \dfrac{1}{R_Z // C_Z} \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix} \tag{2}$$

where, R_Y, C_Y and R_Z, C_Z are parasitic resistances and capacitances, respectively at port Y and Z. R_X is the series parasitic resistance at port X. α and β are current and voltage gains of the CCII. Considering an actual CCII in the floating inductance of Fig.1, the equivalent floating impedance between nodes IN and OUT is given by:

$$Z_{eq} = \frac{(R_1 + R_{X1} + R_{X2})(R_2 + R_{X3} + R_{X4})Y_C}{\alpha_3 \beta_1} \tag{3}$$

with:

$$Y_C = \frac{1}{R_{Y4}} + \frac{1}{R_{Z1}} + (C_{Y4} + C_{Z1} + C)s \tag{4}$$

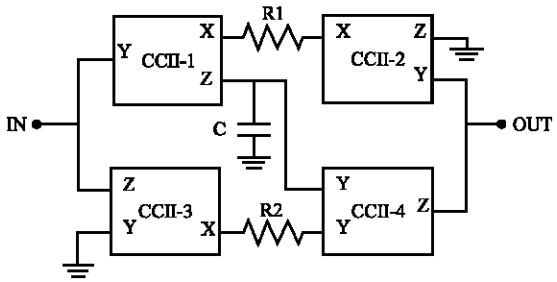

Fig. 1: Floating inductance simulation

According to this relation, the proposed floating inductance frequency behavior can be tuned by varying the parasitic impedance at port X. With a CCII translinear configuration, the parasitic impedance at port X can be controlled by a DC control current. However, the proposed inductance is slightly affected by parasitic resistances at port Y and Z. The finite parasitic resistance at port Y of CCII-4 and the finite parasitic resistance at port Z of CCII-1 introduce a low frequency zero. The inductance is thus equivalent to a small active resistance at low frequency. Moreover, the presence of a pole either in the current transfer gain $\alpha 3$ or in the voltage transfer gain β_1 introduces a high frequency zero in the equivalent floating inductance. For reduced effect of parasitic elements, we should underline that those effects are greatly related to the electronic implementation of the CCII.

OPTIMIZATION APPROACH OF THE TRANSLINEAR CCII

The conventional translinear configuration is a very attractive, turnable and simple implementation of CCII, that has been used in many RF circuit designs and demonstrated good performances at high frequencies[10]. Owing to the translinear loop carried in this configuration, nearly ideal CCII behaviour can be observed at its three terminals. Parasitic effects in this configuration are directly related to a control current and it is also known as CCCCII (current controlled CCII). Most reported realizations of translinear CCII has been implemented using either bipolar transistors or MOS transistors. Both have cases, a simple and flexible design is curried showing the best performances. Let's consider the MOS CCII translinear implementation in Fig. 2.

The considered circuit achieves the function of voltage follower between ports Y and X by means of one mixed translinear loop (M_1-M_4). The transistors M_9-M_{13} ensure the bias of the mixed loop. Transistors M_1 and M_3

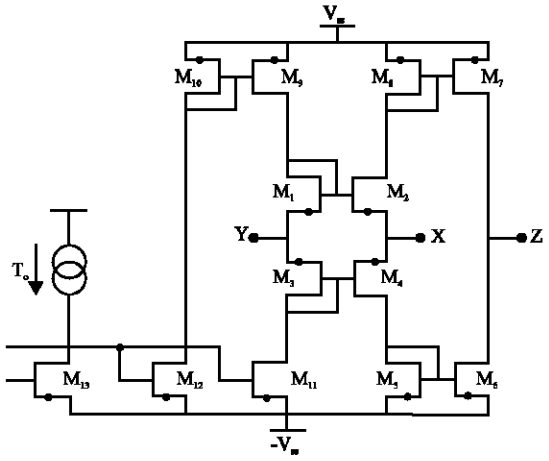

Fig. 2: Translinear loop MOS Based implementation of CCII

are biased to the same current I_o. Assuming the same static gains for the NMOS and PMOS transistors, the parasitic impedance at port X is given by:

$$R_X = \frac{1}{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_N (1+\lambda_N V_{DS}) I_o} + \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_P (1+\lambda_P V_{DS}) I_o}} \quad (5)$$

Where: λ_N and λ_P are channel length modulation coefficients of NMOS and PMOS transistors, respectively and μ_n and μ_p are, respectively electrons and holes mobility and C_{ox} is the oxide capacitance. According to this relation, R_X can be tuned by the dc current I_o.

In the same way, small signal analysis of the translinear CCII leads to the theoretical expressions of the parasitic resistances at port Y and Z, given, respectively in the following equations:

$$R_Y = \left(\frac{1}{g_{m1}} + r_{09}\right) // \left(\frac{1}{g_{m3}} + r_{011}\right) \quad (6)$$

$$R_Z = \left[r_{04}\left(1 - \frac{g_{m6}}{4\alpha\sqrt{\beta I_o}}\right)\right] // \left[r_{07}\left(1 - \frac{g_{m7}}{4\alpha\sqrt{\beta I_o}}\right)\right] \quad (7)$$

where, g_{mi} is the transconductance of transistor M_i.

According to these theoretical expressions, second order effects variations of R_Y and R_Z with respect to the control current Io can be observed. In fact, both transconductances g_{m1} and g_{m3} in Eq. 6 are dependent on I_o. All the above expressions of the parasitic impedances are technology dependent. Thus, an optimization of the CCII can not be a technology independent process and given one particular technology, all the performances of a CCII are closely related to the transistors scaling. The question is then how to scale these transistors to get the best performances.

We fixed our choice in this step on the technology 0.35 μm CMOS of AMS. We used in the CCII optimization the following series of criterions:

- The cut off frequency of the voltage follower F_{CV} between terminal Y and X is maximized.
- The cut off frequency of the current follower F_{CI} between terminals X and Z is maximized.
- The parasitic impedance at port X is minimized.
- The parasitic impedances at port Y and Z are maximized.
- The silicon area of the whole CCII is minimized.

The objective function to maximize can thus be formulated as follows:

$$\phi = \theta_1 F_{CV} + \theta_2 F_{CI} + \frac{\theta_3}{R_X} + \theta_4 R_Y + \theta_5 R_Z + \frac{\theta_6}{\left(\sum W_i L_i\right)} \quad (8)$$

Where, $\theta_1,\ldots,\theta_6$ are positive coefficients used for normalization.

The first step in the optimization is the expressions of the different criterions by a technology dependent model. For accurate modelling, a small signal analysis of the CCII is carried to explicit both voltage and current cut-off frequencies with respect to transistor dimensions. We apply then in the optimization process, a Heuristic programmed with C^{++} software, which is an algorithm driven methodology. This approach[11] was followed in many radiofrequency designs and gave promising results[12]. It starts with an initialization of the parameters vector which include the sizing of the different transistors interfering in the above expressions. A random choice of the variables vector is then done followed by a verification of the preliminary conditions. These conditions are imposed to ensure that the different transistors are in the inversion mode of operations. If these conditions are fulfilled, the vector parameters is a candidate for the following steps, otherwise we do another choice. Next, we compute the objective function. If it is decreasing, when compared to the previous iteration, the parameters vector is saved, otherwise, we keep this vector unchanged. After a series of trials with the randomly chosen parameters, the parameters vector corresponding to the minimal objective function is obtained. When the number of trials is important, this solution corresponds to an optimal solution.

This method does not suffer from any divergence problems seen when applying gradient based methods, but its efficiency is closely related to the number of iterations. Indeed, with a high number of trials, we manage to explore in a simple random way all the proposed tuning range of the different parameters and good performances are ensured.

Simulation conditions are the following: the supply voltage is 2.5 V and the control current is 100 μA. We notice that the optimization process can be done in the same way for other simulation conditions.

Table 1 shows the optimal devices scaling that we get after applying the optimization approach. Figure 3 shows the simulated parasiticresistance R_X of the optimized configuration. For these parameters, the parasitic resistance at port X can be tuned on more than a decade over [232 Ω and 3.57 kΩ] by varying I_o in the range [1-400 μA]. Such control is very important since it will be exploited in the inductance tuning. Moreover, the parasitic resistances at port Y and Z, respectively R_Y and R_Z decrease by a factor of two over the same range of control current. Those parasitic should be taken into consideration in our design, since they interfere in the simulated inductance frequency behaviour. We plot their variation versus the control current I_o in Fig. 4. The remaining other static and dynamic characteristics of the implemented CCII are summarized in Table 2.

Table 1: Optimal device sizing

Device name	Aspect ratio W/L (μm)
M_1, M_2	20/0.35
M_3, M_4	54/0.35
M_{xx} (in PMOS current mirrors)	27/0.35
M_{xx} (in NMOS current mirrors)	10/0.35

Table 2: Simulated static and dynamic characteristics of the optimized CCII

α	1.02
β	0.98
C_Y	63 fF
C_Z	23 fF
F_{CI}	1.28 GHz
F_{CV}	5.48 GHz
Offset voltage	20.4 mA
Offset current	-19.33 μA

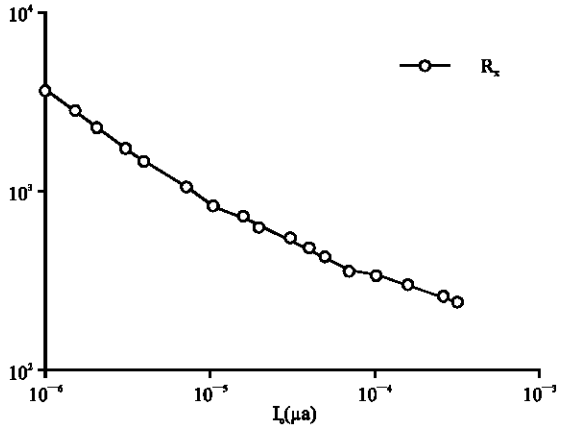

Fig. 3: Parasitic resistance at port X versus the control current I_o for the conventional translinear CCII structure

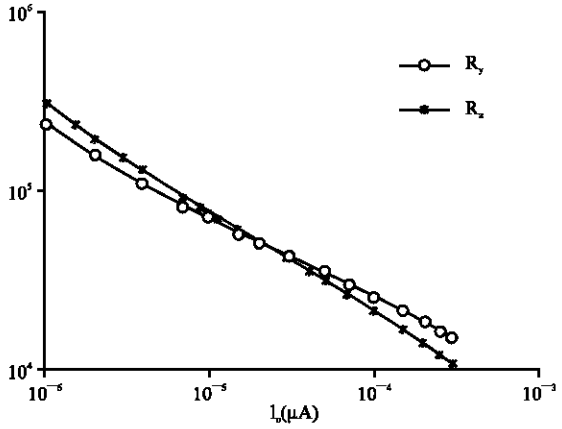

Fig. 4: Parasitic resistance at port Y and Z versus the control current I_o for the optimized CCII

FREQUENCY COMPENSATION STRATEGY AND SIMULATION RESULTS

The circuit of Fig. 1 is simulated using the implemented CCII and taking as null resistances for R_1 and R_2, so that the ideal inductance value is directly related to the series parasitic resistances at ports X. Figure 5, shows that the impedance behavior can be approximated to that of an inductance in a limited frequency range.

As demonstrated above, the lower frequency limitations of the simulated floating inductance is due to the finite parasitic resistances R_{Y1} and R_{Z4}. By varying the control currents of CCII-1 and CCII-4, these parasitic resistances are changing. One way for compensating for these parasitic resistances effects is to connect an active negative resistance in parallel which value is equal to:

$$R_{eq} = -R_{Y1} // R_{Z4} \quad (9)$$

Fot easier comparison both CCII-1 and CCII-4 are made constant. In that case, the simulated floating inductance will be tuned by the control currents of both CCII-2 and CCII-3.

The value of the negative resistance should be very high for low current controls and relatively low for high control currents since R_Y and R_Z are so. Since high values of resistances are required, we should eliminate a passive resistance solution. Actually, this can be done by

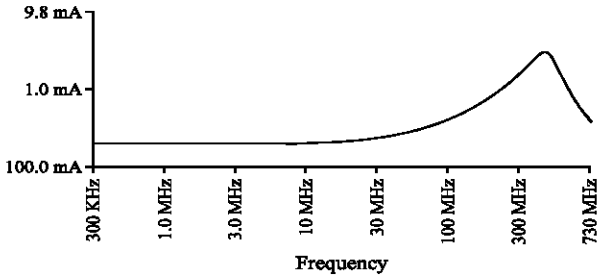

Fig. 5: Floating inductance impedance simulated magnitude results for a control current of I_o=1 μA

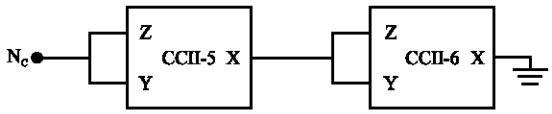

Fig. 6: A negative impedance converter

a controllable resistance so that it can be tuned until satisfying the required equality. Let's consider the negative impedance converter of Fig. 6. Applying the input output relations between the CCII's terminal quantities, we get the following expression for the active negative converted resistance at node N_C:

$$Z_{in} = -\left(R_{Z6} // R_{Y6}\right) \quad (10)$$

By tuning the control current of CCII-6, we can adjust the negative impedance to get the required value for compensation. This impedance converter introduces at node N_C two extra parasitic impedances R_{Y5} and R_{Z5} that should be compensated by the same way. Since the parasitic resistances R_Y and R_Z of the implemented translinear CCII vary in a decade when the control current vary in the range (1 μA; 400 μA), it is always possible to get the compensation. Indeed, we need just to fix the control current of that of CCII-1, CCII-3 and CCII-5 to a low value for example 50 μA and there will exist a control current for the CCII-6 satisfying the compensation condition in Eq. 9. Since the cut off frequency of the used CCII current follower is smaller than that of the voltage follower, the higher frequency limitations of the simulated floating inductance is due to the pole introduced by the current mirrors in the CCII. This pole creates a high frequency zero in the equivalent impedance of the simulated inductance. By connecting a small valued series resistance with the capacitor, we introduce a high frequency pole that can compensate for this zero. The required value of the compensating resistance is low and can therefore be implemented with a passive resistance.

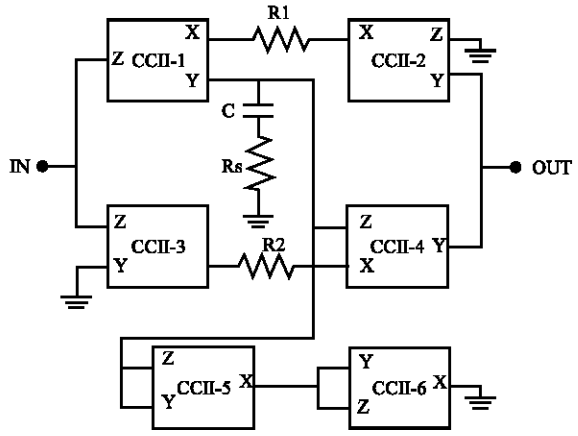

Fig. 7: CCII Based Compensated floating inductance

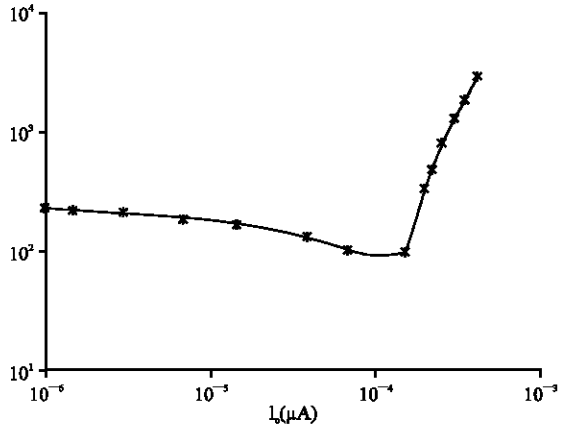

Fig. 8: Series parasitic resistance of the simulated inductance versus the control current of CCII-6

An application of this compensation strategy was implemented as shown in Fig. 7. As a consequence, the lower frequency bound is reduced to 85 MHz. Moreover, a series resistance of 440 Ω leads to an upper bound frequency of 600 MHz for a controlled current of 100 μA.

Simulation results for different control currents of CCII-6, adjusting the inserted negative impedance are shown in Fig. 8. A minimum of the low parasitic resistance of the simulated inductance is obtained for a control current Io6=105 μA when we take for the control currents of the different CCII's $I_o1=I_o4$=159 μA, I_o5= 48 μA, $I_o3= I_o2$=100 μA.

The simulated inductance can be tuned by the control current of both CCII-2 and CCII-3 in more than one decade ranging from 0.45 μA-57.4 μH by varying the control current in the range (0.1 μA; 400 μA).

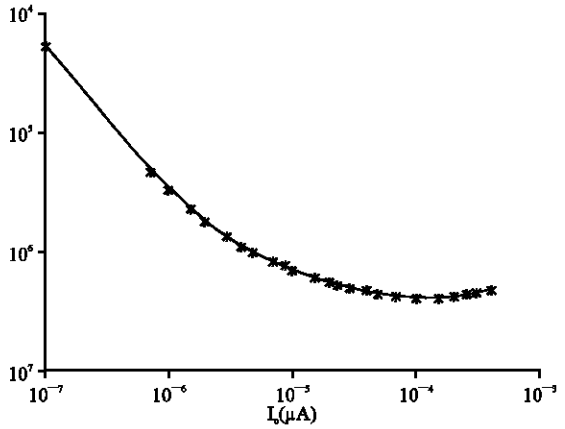

Fig. 9: Simulated inductance value versus the control current

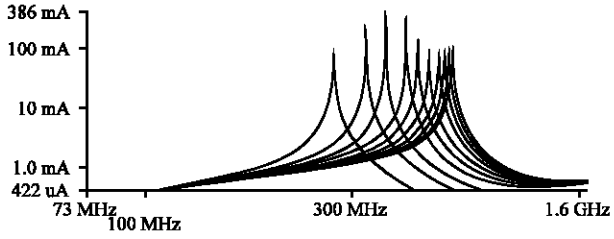

Fig. 10: Frequency resonance of the tunable LC filter design

AN APPLICATION EXAMPLE: CCII BASED BAND PASS FILTER

For proposed simulated inductance, it was applied in the implementation of a fully integratable LC bandpass filter. The resonance frequency of an LC circuit is $F_R = (1/2\pi\sqrt{LC})$, we use the floating inductance simulators and two grounded capacitors. The capacitors are taken equal to C = 0.5 pF. Simulated results of the LC Filter are shown in Fig. 10. It is possible to see that the LC filter response behaves like the one expected in an extended range of frequencies (270 MHz-520 MHz) when the control current is varied in the range (10μA; 400 μA).

CONCLUSION

In this study, we have proposed a class AB CCII based implementation of a tunable simulated floating inductance. In order to improved high frequency characteristics, the proposed design was optimized in a block level starting with the optimization of the translinear current conveyor. The optimized CCII has a current bandwidth of 1.28 GHz and a voltage bandwidth of 5.48 GHz. Then the simulated inductance was considered in a system level for reducing the nonidealities effects of the CCII parasitic impedances. Simulation results show that the simulated inductance can be tuned over more than a decade in the range (0.45-57.4 μH) over a high frequency range of operations. As an example of illustration, we apply the simulated inductance in a high frequency fully integrable band pass filter. The resonance frequency of the designed filter can be tuned in an extended range of frequencies (270-520 MHz) when the control current is varied in the range (10 μA; 400 μA).

REFERENCES

1. Elwan, H. and A. Soliman, 1996. A novel CMOS current conveyor realization with an electronically tunable current-mode filter suitable for VLSI. IEEE Trans. Circuits Syst., 1: 663–670.
2. Surakampontorn, W., V. Riewruja, K. Kumwachara and K. Dejhan, 1991. Accurate CMOS-based current conveyors. IEEE Transactions on Instrumentation and Measurement, 4: 699-702.
3. Masmoudi, D.S. and A. Fakhfakh, 2005. A new low voltage CMOS current controlled oscillator with minimum phase noise. IEEE the 16th International Conference on Microelectronics,Tunisia,
4. Thoumazou, C., F. Lidgey and D. Haigh, 1990. Analog Integrated Circuits Design: The Current Mode Approach. IEE, London, UK.
5. Kiranon W. and P. Pawaranghoon, 1997. Floating inductance simulation based on current conveyors. Electron.Lett, 33: 1748-1749.
6. Ferri, G. and N. Guerrini, 2001. High valued passive element simulation using low-voltage low-power current conveyors for fully integrated applications. IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 48: 405-409.
7. Cheng, M. and C. Thoumazou, 1993. 3V MOS current conveyor cell for VLSI technology. Electron. Lett., 29: 317-318.
8. BenSalem, S., M. Fakhfakh, M. Loulou, D.S. Masmoudi and N. Masmoudi, 2005. An optimized CMOS CCII and High-Q high frequency band-pass active voltage filter. IEEE International Confrence on Signals Systems and Devices, Tunisia.
9. Fabre, A. and M. Alami, 1997. A precise macromodel for second generation current conveyors. IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 44: 639-642.

10. Fabre, A., H. Amrani and O. Saaid, 1996. Current mode band-pass filters with Q magnification. IEEE Transactions on Circuits and Systems-II, 43: 839-842.
11. Fakhfakh, M., M. Loulou and N. Masmoudi, 2004. An improved algorithm-driven methodology to optimize switched current memory cells by transistor sizing. IEEE International Conference on Electrical, Electronic and Computer Engineering (ICEEC'04). Egypt.
12. Ben Salem, S., A. Fakhfakh, M. Loulou, P. Loumeau and N. Masmoudi, 2004. A 2.5 V 0.35 μm CMOS current conveyor and high frequency High-Q band-pass filter. The 16th International Conference Microelectronics ICM 2004, Tunisia.