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Use of a Nonlinear Controller to Improve One-cycle Controller Response

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Abstract: In this study, a new method for improvement of the one-cycle control method in buck type converter is proposed. Better command tracking and better load disturbance rejection ability are its main advantages over the classical one-cycle controller. The main idea is to apply a pseudo reference instead of actual reference to one-cycle controller by an auxiliary controller to improve the response. The magnitude of this pseudo reference is related to the output error value and so the dynamic of filter and load contribute in control process. It is known that this is not the case in one-cycle control method. In addition, as it is shown, in this controller there are three parameters to change the performances of the controller. Therefore, some degrees of freedom have been added to the design parameters in compare to the one-cycle controller. It should be noted that, this method is suitable for the cases which the filter and load have damped behavior.

Key words: One-cycle control, limit cycle, nonlinear control, switching power converter

INTRODUCTION

The progress of control theory in the field of power electronics has resulted in several new methods which are suitable for power converters control. One-cycle control method, which was proposed about one decade ago (Smedley and Cuk, 1991) is one of them. From its invention it has found many applications such as active power filter and power factor correction (Smedley *et al.*, 2001; Qiao and Smedley, 2003) switching amplifiers (Qiao *et al.*, 2000; Lai and Smedley, 1996) etc. The idea of this controller is based on using a resetable integrator to adjust the average value of a chopped signal in each signal.

Its main characteristic is the real time ability to completely reject the variations of input voltage (Smedley and Cuk, 1991). However despite of this great feature its load rejection and command tracking abilities are not satisfactory. Especially at light load, overshoot and lightly damped oscillations may happen in output response (Santi and Cuk, 1992).

In this study a method for compensation some of the deficiencies of one-cycle control method is given. In this method, an auxiliary nonlinear controller is used to select proper reference command for the one-cycle controller due to the value of output error. This method is suitable for the damped or over-damped systems. In addition, the buck type converter has been considered.

However, it is easy to extend the method to the other types of converters.

Overview of one-cycle control method: As shown in Fig. 1, the flip-flop at any clock arrival turn-on the switch until the integral of V_s reaches the reference value divided
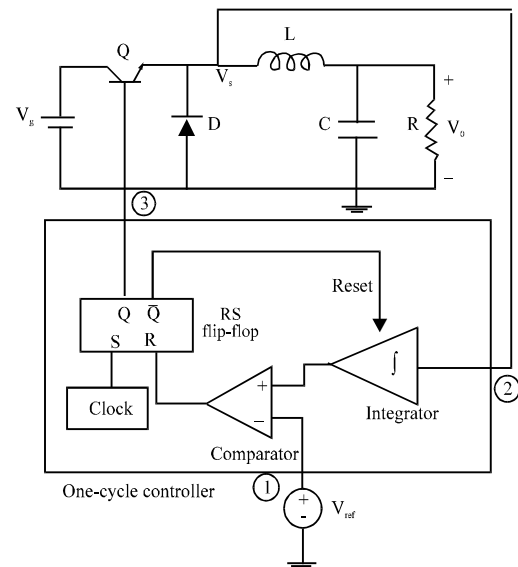

Fig. 1: Basic scheme of one-cycle controlled buck converter

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by switching frequency (gain of integrator). Then the comparator reset the flip-flop and so integrator then turn-off the switch. Therefore, there is a pulse train, of which the mean per cycle is equal to V_{ref}. It is clear that the average or dc value of this train, i.e. the output voltage of the low pass filter, when the filter is lossless, also is equal to V_{ref}. It can be mathematically formulated as follows in which the bar sign represents mean or dc value (Smedley and Cuk, 1991).

$$V_o = \overline{v}_s = \frac{1}{T_s}\int_0^{T_s} v_s \, dt = \frac{1}{T_s}\int_0^{dT_s} v_g \, dt = V_{ref} \qquad (1)$$

Because theoretically low pass LC filters are lossless, the average value of their output signal and input signal are equal. Based on this fact, in one-cycle control method, the output filter is ignored and the feedback signal is taken from the input of the filter (Santi and Cuk, 1992). In the conventional method, a feedback is taken from the output and is compared with the reference value. Therefore the dynamic of the output filter contributes to the control process. Consequently, there is a delay to control the line disturbances.

However, if a high dynamic low pass filter, instead of output filter, is used for measurement of dc value of chopped voltage V_s, it will be possible to control the line disturbance faster. In the one-cycle control method, an integrator is used instead of a high dynamic low pass filter to reduce the response time of measurement and so controller.

Despite of the advantages of one-cycle control method, which have made it suitable for some cases, there are some drawbacks in comparison with the conventional PWM method.

In fact, the main strength of one-cycle control is its ability to reject the input disturbance quickly. However because there is no feedback from actual output, in the case of non-ideality of elements, the output cannot follows the command exactly and therefore in general there is a steady state output voltage error. The non ideality of inductor and non zero value of diode forward voltage are the main causes of output offset in one-cycle controller.

Another problem of the one-cycle control method is its poor dynamic responses to the commands and output disturbance. The rigid structure of the one-cycle controller, which has no any parameters to be adjusted by designer, is the other deficiency of this method. As it is known, in conventional PID (Proportional, Integrator, Derivative) controller, the parameters of controller, i.e. P, I and D, can be adjusted by designer due to the desired response. However this is not the case in one-cycle controller.

Error sensitive one-cycle control method: As mentioned earlier the lack of output feedback is one of the drawbacks of the one-cycle control. It is understood that by adding a feedback from output the performances of the controller can be improved. In Fig. 2, the basic necessary configuration has been shown. By following this approach one can improve the one-cycle control behavior by using another controller. This controller will give another degree of freedom to the overall system. In this study a nonlinear controller has been used as auxiliary controller. It is also possible to use a PID (lead-lag) controller as an auxiliary controller (Ruzbehani *et al.*, 2004).

In Fig. 3, the proposed method, so named Error sensitive one-cycle control method has been shown. This method is a combination of a relay type nonlinear controller and one cycle controller. As it is shown in Fig. 3, the controller chooses the reference value for one-cycle controller according to the output error value.

The operating function of selector block is as shown in Fig. 4. The absolute value of positive and negative
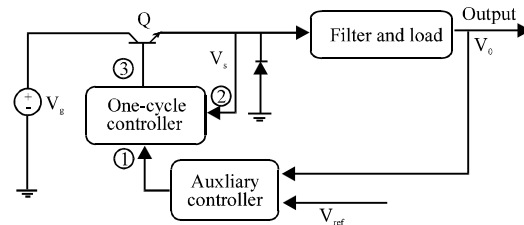
Fig. 2: Schematic diagram of general method for modifying one-cycle controlled buck converter. The numbering of one-cycle controller ports is as Fig. 1
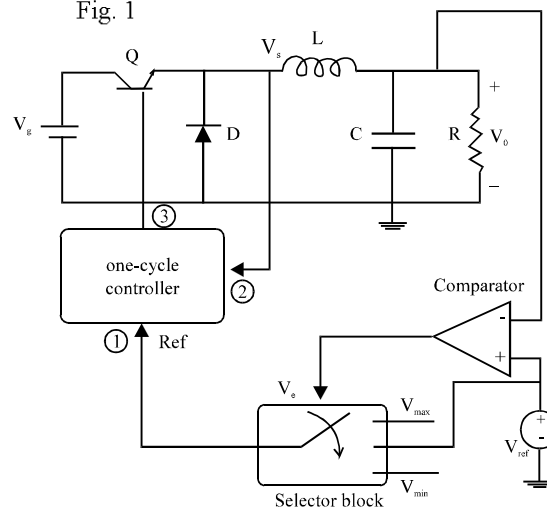
Fig. 3: Schematic diagram of the proposed method, for modifying one-cycle controller performances. The numbering of one-cycle controller ports is as Fig. 1
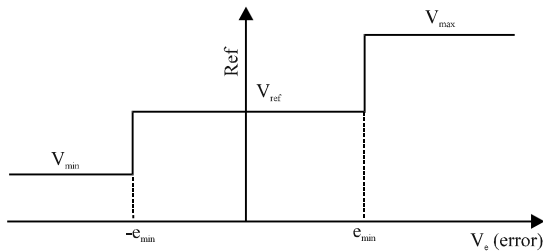
Fig. 4: Mathematical model of selector block function

Fig. 5: Schematic diagram of selector block implementation

switching levels, i.e. e_{min} and $-e_{min}$, can be chosen non equal, but here for simplicity they have been chosen equal.

As Fig. 4 implies: $V_{min} < V_{ref} < V_{max}$. We can see later that this condition must be satisfied for correct operation of the controller. Proper choices for V_{max} and V_{min} are:

$$V_{max} = D_{max} \times V_g$$
$$V_{min} = D_{min} \times V_g$$

In which D_{max} (D_{min}) is the maximum (minimum) allowable value of duty cycle in practical point of view. In practice by choosing proper value for gain of integrator in one-cycle controller, reference voltage can be scaled down to be in the range of comparators working voltage limits.

In Fig. 5 an easy way to implement the selector block has been shown. This configuration also has been used in simulation of controller. The switches states as shown in Fig. 5, are corresponding to the positive control voltage, i.e. V_{c1} and V_{c2} are positive. The operation of circuit is as follows. When $V_e > e_{min}$ (and so $V_e > -e_{min}$), V_{c1} is positive and V_{c2} is negative, so the upper switch states are as shown and those of lower one are opposite. Consequently Ref signal is equal to V_{max}. When $V_e < -e_{min}$ (and so $V_e < e_{min}$), V_{c2} is positive and V_{c1} is negative, so the lower switch states are as shown and those of upper one are opposite. Consequently Ref signal is equal to V_{min}. When $-e_{min} < V_e < e_{min}$, both of V_{c1} and V_{c1} are negative, so the upper and lower switch states are opposite of what is shown in Fig. 5 and consequently the Ref signal is equal to V_{ref}. Capacitor C_1 has been added to filter out the transient effects.

Figure 6 shows the operation of controller. As shown in Fig. 6, at the time t_1 the step function has been applied to the system. In this time, the error is larger than e_{min} and therefore the selector block chooses pseudo reference V_{max} for the controller. Therefore system response is faster than when V_1 is applied as reference, because time constants are the same but references values are different.
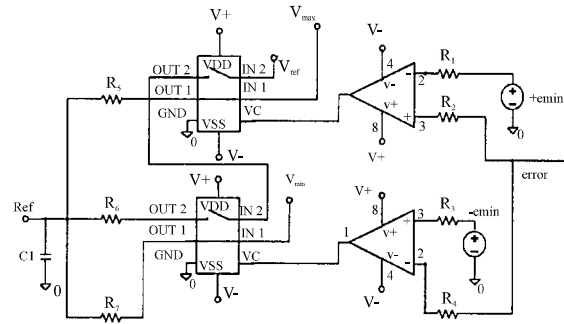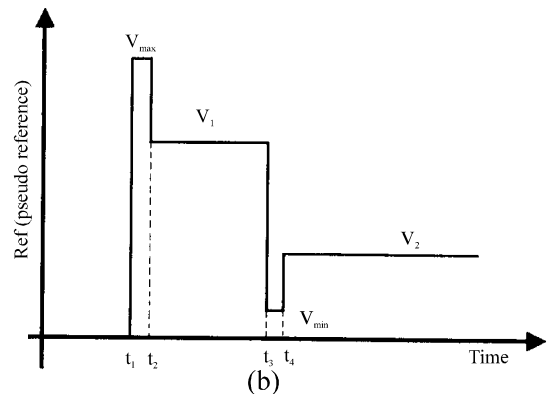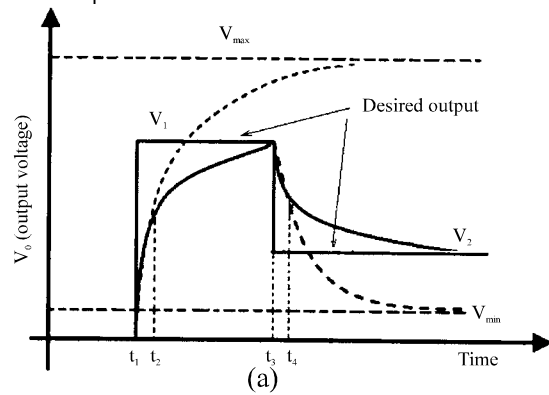

Fig. 6: (a) Output variations due to change of desired output. (b) Pseudo reference generated by proposed controller

At t_2, the error has become equal to e_{min}. Hereafter the selector block chooses V_1, as the reference, which is the actual reference value in this case. For the negative pulses, at the beginning when the magnitude of error is large and therefore the pulse-width should be reduced very fast, the selector block will choose pseudo reference V_{min} until output reaches point t_4. In this point, absolute value of error is less than absolute value of e_{min}. Hereafter the controller acts as a conventional one-cycle controller and chooses V_2 as the reference.
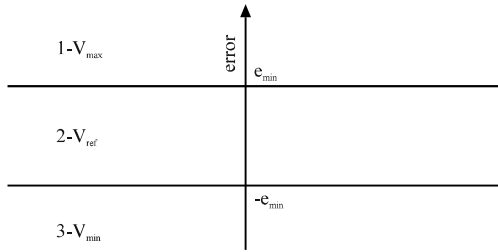
Fig. 7: Scheme of working zones of controller

When there is no need to ac signal (in ordinary buck converter without transformer), it is possible to choose $D_{max} = 1$ and $D_{min} = 0$ ($V_{max} = V_g$ and $V_{min} = 0$). It means that in this condition the switch will held on or off for a while that error is not in the range $\{-e_{min} \ e_{min}\}$ so the response will be faster.

STABILITY OF THE CONTROLLER

In Fig. 7 it is possible to divide the working area of the controller to three zones as follows:
Zone 1:

$$V_e > e_{min} \Rightarrow V_o < V_{ref} - e_{min} \quad \text{and} \quad Ref = V_{max} \quad (2)$$

The nature of zone 1 is to increase the output voltage. This assumption is correct because V_{max} is the maximum accessible output. Therefore, after entering to this zone the output voltage will become so large, which the system will leave this zone and enter zone 2.
Zone 3:

$$V_e < -e_{min} \Rightarrow V_o > V_{ref} + e_{min} \quad \text{and} \quad Ref = V_{min} \quad (3)$$

The nature of zone 3 is to decrease the output voltage. This assumption is correct because V_{min} is the minimum accessible output. Therefore, after entering to this zone the output voltage will become so small, which the system will leave this zone and enter zone 2.
Zone 2:

$$-e_{min} < V_e < e_{min} \Rightarrow V_{ref} - e_{min} < V_o < V_{ref} + e_{min}$$
$$\text{and Ref} = V_{ref} \quad (4)$$

The system will remain in this zone until next command or disturbance (or inertia of system itself) forces the system to leave this zone.

It can be seen that zone 2 acts as an attractive band and because the Ref signal in this zone is located inside the zone, it will satisfy the general stability of the system. However for this matter the condition $V_{min} < V_{ref} < V_{max}$ is
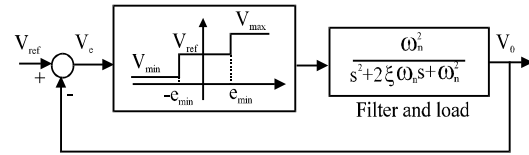

Fig. 8: Simplified Block diagram of the overall system for DF analysis

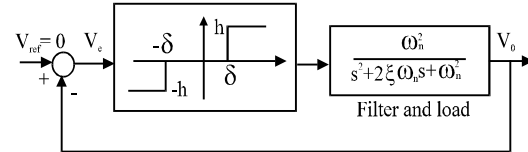Fig. 9: Block diagram of system in symmetric case for the DF analysis

necessary. If this condition is violated, the output will be trapped in one of V_{max} or V_{min}. However, despite of this matter the system in some condition may shows oscillatory behavior.

For more investigation, the model of system for stability purpose will be derived. Because the time constant of the low pass filter, according to the design, is very larger than the switching period, it is possible to model the system as a continuous time dynamic model and ignore the switching phenomenon as it is shown in Fig. 8. This is a well-used approximation in modeling converters (Erickson, 1997). In this model it is supposed that applying a train of pulse with amplitude A and duty cycle D when the frequency is enough high, is same as applying a step with amplitude A × D. Therefore the switching mechanism has been neglected and just its continuous counterpart has been sketched. The nonlinear part of this scheme is a biased asymmetrical nonlinearity.

Among methods, which are applicable for this system, a candidate is describing function or DF (Atherton, 1982). For analysis of this system by use of describing function, it is necessary to use Sinusoid plus Bias Describing Function or SBDF, which in general case is not easy to use. For simplicity in following the problem will be solved for a simplified case.

When the following relation is satisfied.

$$V_{max} - V_{ref} = V_{ref} - V_{min} \quad (5)$$

The resulted nonlinear part will reduce to a relay with dead zone with dc shift of input, as it is shown in Fig. 9, in which

$$h = V_{max} - V_{ref} \quad \text{and} \quad \delta = e_{min} \quad (6)$$

Because the diagram is plotted for limit cycle analysis, it is no need to consider dc values. However for

dc analysis the initial condition of output voltage in Fig. 9 should be considered equal to $-V_{ref}$. The DF of the nonlinear part can be calculated as follows.

$$a > \delta \quad N(a) = \frac{2h}{\pi\delta}\sin(2\cos^{-1}\frac{\delta}{a}) = \frac{4h\sqrt{a^2 - \delta^2}}{a^2\pi}$$
$$a < \delta \quad N(a) = 0 \tag{7}$$

In which a is the amplitude of oscillation. The characteristic equation of the system is as follows.

$$f(s,a) = s^2 + 2\xi\omega_n s + \omega_n^2(1 + N(a)) = 0 \tag{8}$$

Substituting s = jω gives the real and imaginary part of f as follows:

$$R(f(\omega,a)) = -\omega^2 + \omega_n^2(1 + N(a)) = 0$$
$$I(f(\omega,a)) = 2\xi\omega_n\omega = 0 \tag{9}$$

It is clear that the imaginary part of f for non-zero value of ω has no answer and hence sustained oscillation will not happen.

In general the transfer function of filter and load is more complex than above mentioned one, because the resistance of inductor and capacitor also should be taken into account. Hence for more general case, the analytical method is rigorous and stability should be investigated by Nyquist diagram. In this method the intersection of -1/N(a) and G(Jω) give the limit cycle frequency and amplitude (Atherson, 2000). For example if we consider the resistance of inductor (r_L) and ESR (Essential Series Resistance) of capacitor (r_c), the transfer function of filter and load will be as follows.

$$G(s) = \frac{R + Rr_c Cs}{L(R + r_c)Cs^2 + (RCr_c + r_L(R + r_c)C + L)s + R + r_L} \tag{10}$$

In Fig. 10, Nyquist diagram of G(Jω) and -1/N(a) locus diagram, for typical values of parameters have been plotted. As can be seen the resulted locus diagram of -1/N(a) for a>δ, lies on the negative real axis starting at -∞ and returning there after reaching a maximum value of -πδ/2h. From Fig. 10 it can be understood that because the G(Jω) does not intersect -1/N(a), the system in general is stable.

In fact, as much as -1/N(a) loci is far from origin, the possibility of existing limit cycle is less. So to reduce the risk of oscillation, the δ/h or $e_{min}/(V_{max}-V_{ref})$ should be increased. Because V_{max} and V_{ref} are the constraints of design, the only parameter which can be adjusted is e_{min}. Therefore by increasing e_{min} the system will be more stable. On the other hand, as will be shown in simulation,
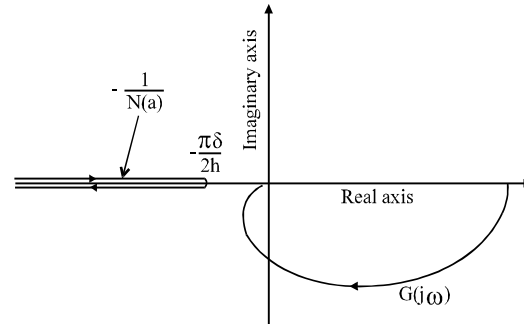

Fig. 10: Nyquist plot of G(Jω) and -1/N(a) loci

by increasing e_{min} the system response will slow down and controller response approaches that of the one-cycle controller. In conclusion selection of e_{min} affects both of stability and speed of system and so should be chosen adequately. For more investigation about the behavior of system in following by use of phase plan portrait, some special cases have been studied.

In Fig. 11, the phase plane portrait for the damped and over damped systems has been given. As shown, in the over damped or near damped cases the system has no oscillation problem and can reach the goal (output =5) at most in some cycles.

Next, two under damped systems have been studied. As shown in Fig. 12, in the case of heavy under damped (damping factor = 0.03) the system oscillates too much before reaching the center. Although the amplitude of oscillation in this case has decreased by time, may be in practice, these cases do not act stable and system experiences long-term decaying oscillation. However, it should be noted that the recommended systems for error sensitive one-cycle control are the over damped or nearly damped systems. In fact, this method is not recommended for under damped system. Because when the system is over damped, by this method the speed of system response increased and therefore rise time will be reduced. However, when the system is under damped, to increase the system speed, means more oscillation, which is not desirable.

Figure 6(b) has demonstrated the behavior of controller by means of the pseudo reference. It can be said that for the under damped systems, this pseudo reference should be changed in opposite manner. That is, for positive step, first step should be smaller than V_1, then V_1 and for negative step first step should be larger than V_2, then V_2. This is an old well known technique that if the step input is applied in two steps to the under damped systems, by proper choosing amplitude and time interval between two steps, it is possible to get the free oscillation output.
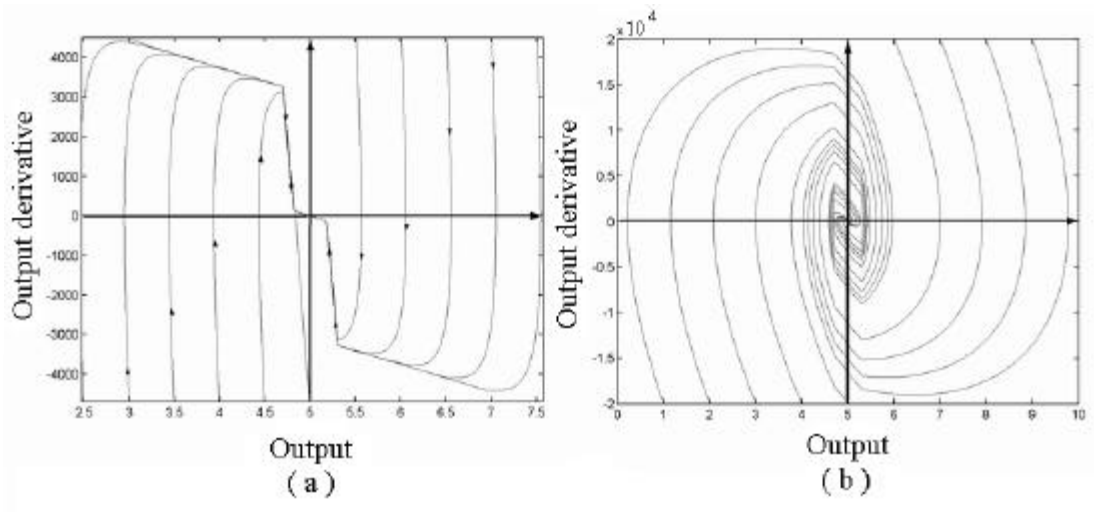
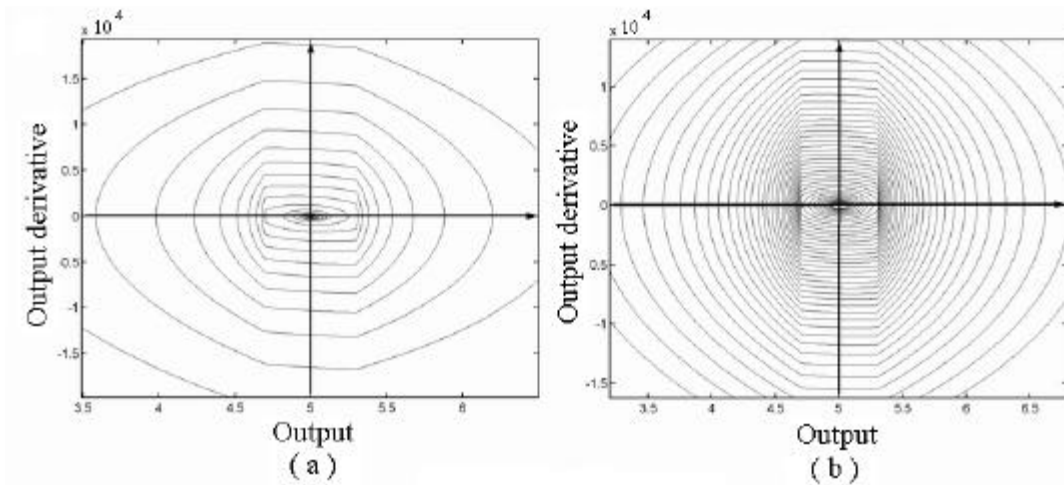Fig. 11: Stable behavior of controller for damped and over damped systems (a) ξ =3.35 (b) ξ =0.7

Fig. 12: Oscillatory behavior of the controller for under damped systems; (a) ξ =0.1 (b) ξ =0.03

SIMULATION RESULTS

For the simulations, the Pspice and Simulink have been used. In the first example, a heavy damped system has been considered. The parameters of system are; L = 1 mH, C = 100 µF, R = 0.4 Ω and the frequency of converter is; f = 20 kHz. As can be seen from Fig. 13, the output reaches the final value sooner than conventional one-cycle control method. In these simulations, it was observed that the output of both controller have an offset error which is related to time delay in switching circuit and integrator, non zero value of diode on-voltage and non ideality of inductance. This is an essential
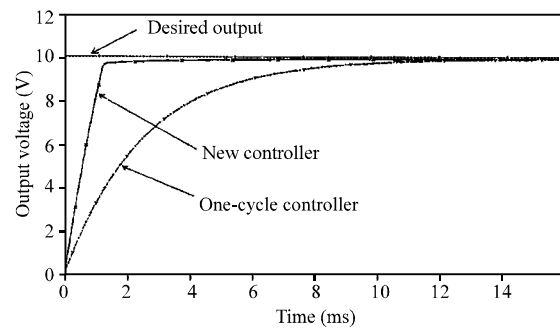

Fig. 13: Comparison of response of the proposed method with one-cycle method for over damped system
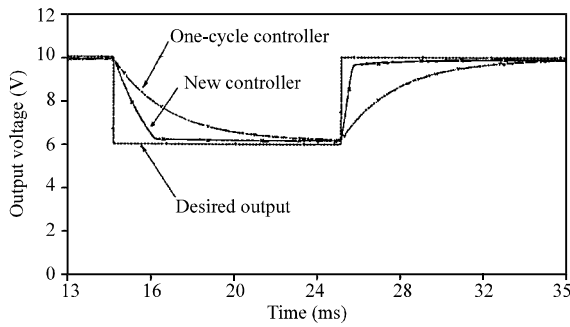
Fig. 14: Comparison between tracking ability of the proposed controller and one-cycle controller
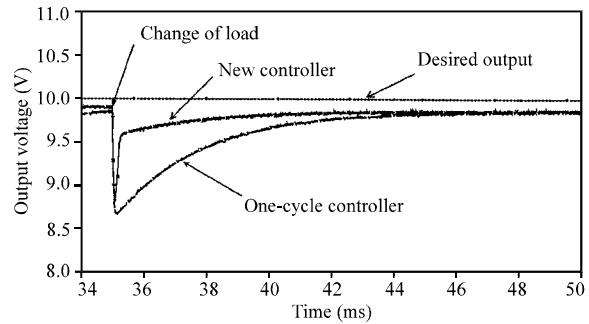

Fig. 15: Effect of e_{min} parameter on the response of system

Fig. 16: The ability of the controller in rejection of disturbance due to load changes in compare to one-cycle controller
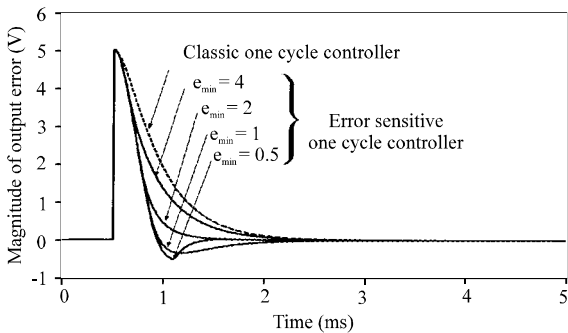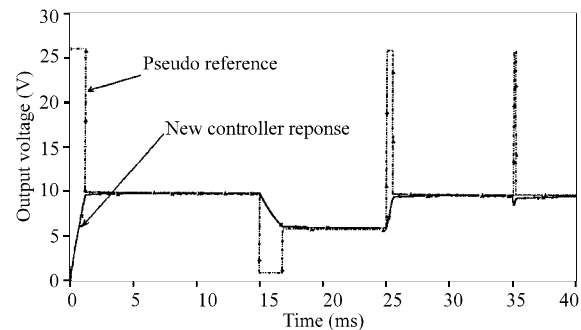

Fig. 17: The change of pseudo reference due to the different cases in the operation of controller

problem of one cycle controller. One of the methods for this problem, which also has been used by the authors in these simulations, is to adjust the time constant of integrator to minimize this offset error.

In the next example, the tracking ability of the controller in compare to the conventional one-cycle controller has been shown. As can be seen from Fig. 14, the proposed controller can follow commands faster than its counterpart. The parameters of system in this simulation are the same as previous example.

In next simulation, the effect of changes of value of e_{min} has been investigated. As shown in Fig. 15, by change of this parameter, the response of system can be changed from having overshot to damped behavior. In fact, by increasing e_{min} the share of real value of reference in the control of system has been increased. Therefore, in this case response of system is approaches to the response of conventional one-cycle controller. It can be seen that by reduction of e_{min} the speed of system increases.

In next example, the ability of the controllers to reject the effect of load changes has been shown. In this example the value of L and C are the same as before and load has been changed from R = 0.4 to R = 0.35Ω. As shown in Fig. 16, the proposed controller has better transient response in rejection of load disturbances

and the speed of controller is more than that of one-cycle controller.

Finally, in Fig. 17, variation of pseudo reference (Fig. 3) due to the above-mentioned conditions has been shown. In fact, the main feature of the proposed method is the use of this pseudo reference instead of actual reference to accelerate the response of system. As shown in Fig. 17, the V_{max} = 26V and V_{min} = 1V.

CONCLUSIONS

A new method to improve the transient response of one-cycle controller by using a nonlinear controller was proposed. The nonlinear controller defines the reference value for one-cycle controller based on the output error. By simulations the performances of the controller were shown. The controller has better step response, command tracking and load change rejection ability, compared to the conventional one-cycle controller.

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