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Analysis Design and Development of Regulated Power Supply-Using Soft Switched Resonant Converters

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Abstract: A high-frequency link series-parallel resonant converter is analyzed using ac complex analysis. Steady-state solutions are derived. A method of optimizing the converter under certain constraints is presented and a simple design procedure is illustrated by a design example. Experimental results are presented to verify the theory.

Key words: Zero current switching, zero voltage switching, dc-dc converter, high frequency, PWM, lagging power factor

INTRODUCTION

Recently, there is an increased interest in the area of resonant converters due to their advantages, i.e., higher frequency of operation, higher efficiency, small size, light weight, reduced EMI, low-component stresses, etc. Recent research has shown that Series-Parallel Resonant Converters (SPRC's) (also called using LCC-type commutation or LCC-type parallel resonant converter) have a number of desirable features compared to series resonant or parallel resonant converters. Operation of such converters above resonance (lagging pf mode) results in a number of advantages: Elimination of di/dt inductors and loss snubbers, use of slow recovery diodes internal to MOSFET', reduced size of magnetic components, etc. An approximate analysis of series-parallel resonant converter operating above resonance using complex circuit analysis has been presented Bhat and Dewan (1987). It is verified using simulation and experimental results.

MATERIALS AND METHODS

Analysis of series parallel resonant converter: The principle of resonant converter can be explained with its operating modes. The resonant converter can operate in five different modes. However the broad classification of modes can be made depending on the duty ratio. n the duty ratio is 1, the resonant converter can operate in two modes via mode 1 and mode 2. The other modes are obtained when duty ratio is less than 1, depending upon the frequency of operation, circuit impedance across terminal AB and duty ratio. When pulse width is maximum (Duty ratio D = 1) the resonant converter can operate in two different modes and under reduced pulse width (D<1), the converter can operate in three different modes. The relative polarity of the parallel capacitor voltage and the voltage across point A and B decides the interval in which the resonant converter can operate (Bhat, 1993).

Mode of operation: Controlling the pulse width of the input voltage to the tank circuit regulates the output voltage of the converter. Here the switching frequency is more than the series resonant frequency and the load is such that equivalent impedance across the terminal AB is inductive, therefore in this mode the converter operates with lagging power factor. The operating waveforms for this mode are shown in Fig. 1. At t = t_0 I(t) is negative therefore D_1 conducts (Fig. 1a, b, c). During the interval t_0-t_1 the current freewheels through S_4, resonant tank, D_1 and back to S_4. This interval is called freewheeling interval (FI). At t = t_1, D_1 and D_2 conduct transferring the energy stored in the inductor back to the source. As a result I(t) reduces to zero and S_1 and S_2 starts conducting. This marks the beginning of power interval. At t = t_3, ib (t) changes from-$I_0 t_0$ +I_0 and converter operation changes. The power interval ends at t = t_4 i.e., (t_0+T/2). It may be noted that in this mode also all switches turned on at zero voltages, facilitating the use of loss less snubber.

Mathematical analysis of converter: Following assumptions are used in the analysis of the series-parallel resonant converter.

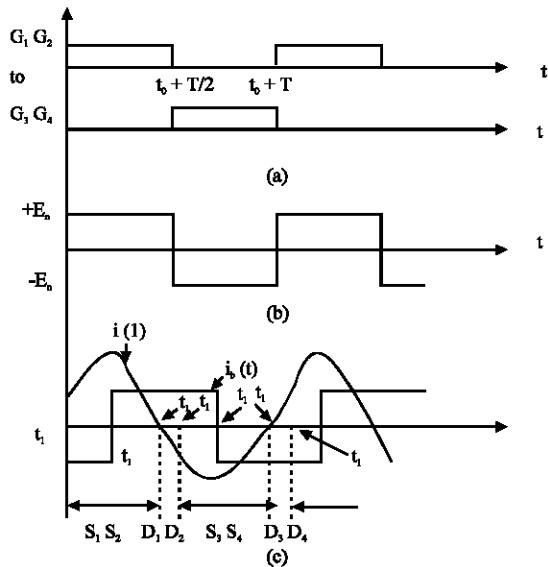- The switches, diodes, inductors, capacitors and snubber components used are ideal.

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Fig. 1: Typical waveform in mode of operation; (a) Gate pulse (b) V_{AB} (t) (c) I (t) and I_b(t)
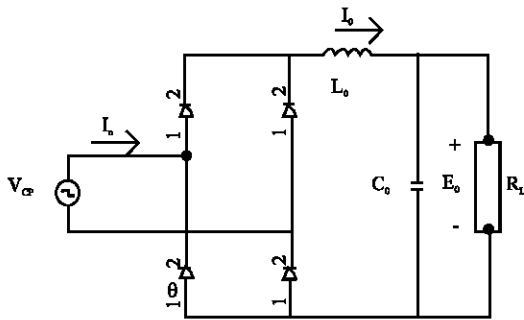

Fig. 2: Output circuit of bridge rectifier and filter component to resonant converter

- The effects of snubber are neglected.
- The inductance I_0 is large enough to keep the load current constant.
- The high frequency transformer is ideal and has unity turns ratio.

From Fig. 2 V_{cp} and I_b represent the rms fundamental component of V_{cp} (t) and I_b (t), respectively. Because of Diode Bridge rectifier and inductive filter present in the output circuit.

The D.C. output Voltage is obtained as the average of A.C. input voltage, Vcp (Rasid, 1998).

$$E_0 = \frac{1}{\pi} \int_0^\pi \sqrt{2\,V_{cp}} \sin \omega t \, d(\omega t)$$

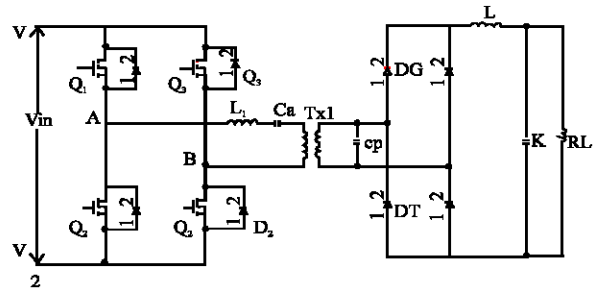$$E_0 = \frac{2\sqrt{2}}{\pi} V_{cp} \tag{1}$$

Fig. 3: PSPICE simulation of series parallel resonant converter

$\omega = 2\pi f$ and f is the switching frequency.

The Fundamental Component of Diode Bridge current is calculated as (using Fourier Analysis).

$$I_b = \frac{1}{\sqrt{2}} \frac{1}{\pi} i_b \text{ (t) Sin } \omega t \, d \, (\omega t) = \frac{2\sqrt{2}}{\pi} I_0 \tag{2}$$

Using Eq. 1 and 2 the equivalent A.C. resistance as seen at the I/P of the Rectifier Bridge is given by:

$$Z_{ac} = V_{cp}/I_b = \pi^2/8 \, Z_L \tag{3}$$

δ and D are related by:

$$\delta = \pi D \tag{4}$$

The RMS fundamental component of inverter output voltage at terminal AB can be found using the waveform shown in (Fig. 3). The duty ratio D is defined as the ratio of the time duration for which the switch S_1 and S_2 or S_3 and S_4 are switched on simultaneously i.e., ton to the half of the switching period (T/2) D = ton/T/2.

The RMS fundamental voltage across AB is given by:

$$V_{AB} = \frac{1}{\sqrt{2}} \frac{1}{\pi} \int_0^{2\pi} V_{AB}(t) \sin \omega t \, d \, (\omega t)$$

$$= \frac{1}{\sqrt{2}} \frac{1}{\pi} \left[\int_{\pi-\delta/2}^{\pi+\delta/2} E_{in} \sin \omega t \, d(\omega t) - \int_{3\pi-\delta/2}^{3\pi+\delta/2} E_{in} \sin \omega t \, d(\omega t) \right] \tag{5}$$

$$= \frac{2\sqrt{2}}{\pi} E_{in} \sin \frac{\delta}{2}$$

Design of series-parallel resonant converter: Following criteria has been taken into account in order to obtain optimum design of series-parallel resonant converters.
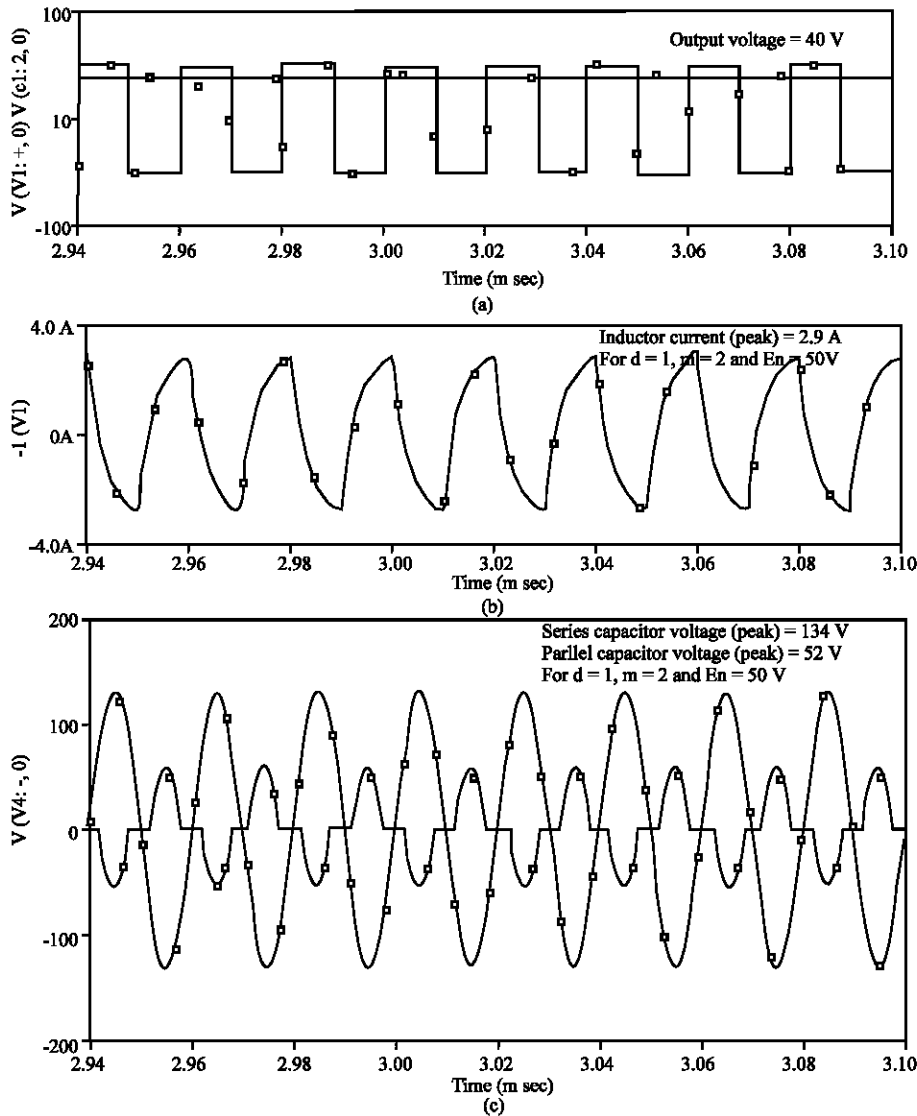
Fig. 4: PSPICE Simulation results for series parallel resonant converter at full load with m = 1 : (a) V_{AB}, V_0 (b) I_{L2} (c) V_{cs}, V_{cp}

• Normalized switching frequency y, such that maintains the lagging power factor conditions.
• Minimum inverter output peak current for small rating and losses.
• Minimum stress in series and parallel capacitor.
• Minimum variation of Duty ratio from full load to no load i.e., good voltage regulation.

Design example:
Minimum input voltage E_{in} = 50 volts.
Output power p = 100 watts.
Switching frequency = 50 kHz.
m = Cs/Cp = 1, Q = 5, y = 8.

The converter gain is given $|E_0/E_1|$ = 0.8 by full load resistance:

$R_L = E_0^2/P = (0.8 * 50)^2/100 = 16\Omega$
$\sqrt{L/C} = Q* R_L = 5* 16 = 80$

Resonant frequency F_o is given by:

$$F_o = F/y = 50,000/.8 = 62.5 \, kHz$$

But $F_o = \dfrac{1}{2\sqrt{LC}}$

$$\frac{1}{\sqrt{LC}} = 2\pi* 62.5* 10^3$$

The values of L and C from (Fig. 3 and 4) are
L = 204 µH

C   = 0.0318 μ F
Since Cs = Cp has been chosen
Cs   = Cp = 2C = 0.0636 μF

RESULTS AND DISCUSSION

Simulation of series-parallel resonant converter: The proposed resonant DC-to-DC converter is simulated using PSPICE software package. It is a general-purpose circuit simulation program, which can be used to obtain the waveforms of different circuit variables both in transient and steady state. However in present study, the simulation is aimed to determine the various voltages and current waveform in steady state (Fig. 3).

Simulation with variation load: Figure 4 and 5 present some of the simulated waveforms obtained for variation of load from full load to 25% of rated load. These waveforms were obtained after a number of simulation runs by varying δ to obtain the approximately the rated load voltage, when load was changed.

Block diagram for series parallel resonant converter with dsp control: The DC input is given to high frequency bridge inverter circuit in series with a resonant circuit, which produces alternating voltage. The switchers are turned on at zero voltage. This circuit is in series with a high frequency transformer. The output of the transformer is rectified using bridge diode rectifier and then filtered.
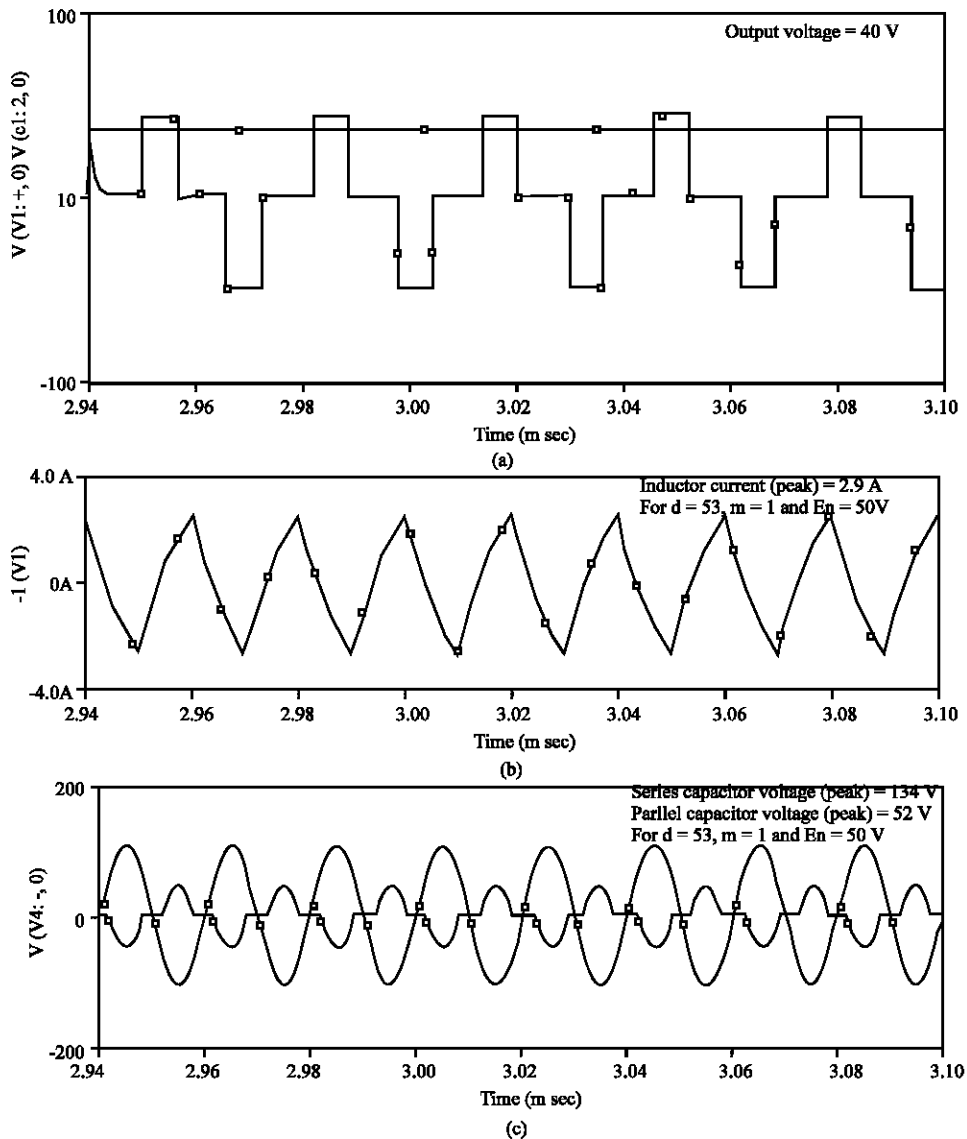

Fig. 5: PSPICE Simulation results for series parallel resonant converter at 25% load with m = 1: (a) V_{AB}, V_0 (b) I_{L2} (c) V_{cs}, V_{cp}
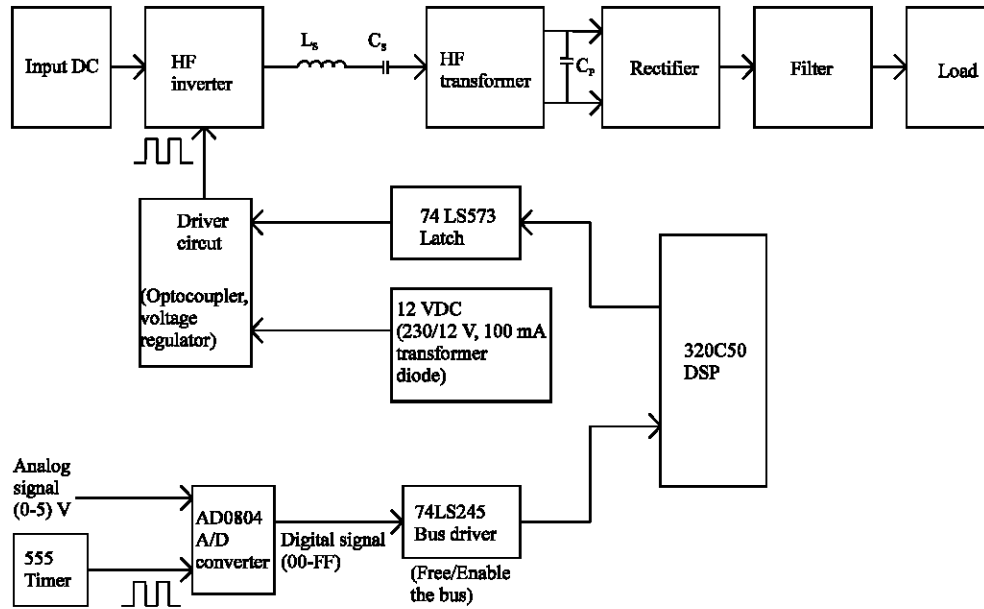
Fig. 6: Block diagram

The filtered output is given as input to the load. Depending on the pulse given by the MOSFET firing circuit controlled by DSP controller, the output voltage is varied (Fig. 6).

Algorithm:
• START
• Disable all interrupts.
• Clear all interrupt flags.
• Stop Timer flag.
• Initialize memory to zero.
• Read memory fro angle between 1 and 4 and 2 and 3.
• Angle in the form of time.
• Make output 0001.
• Run timer for time in the memory
• Make output 1001.
• After time out, make output 0100
• Read the time for angle
• Run timer.
• Make out put 0101 (ABCD)
• Jump to step 6.

Experimental results: Some testing results are presented here to verify the theoretical predictions. An experimental prototype has been implemented for a resistive load of 100W and 16Ω. The resonant inductor is 0.261 mH and the series resonant capacitor is 0.047 μF. The switching frequency is 50 KHz (Fig. 7-8 and Table 1).
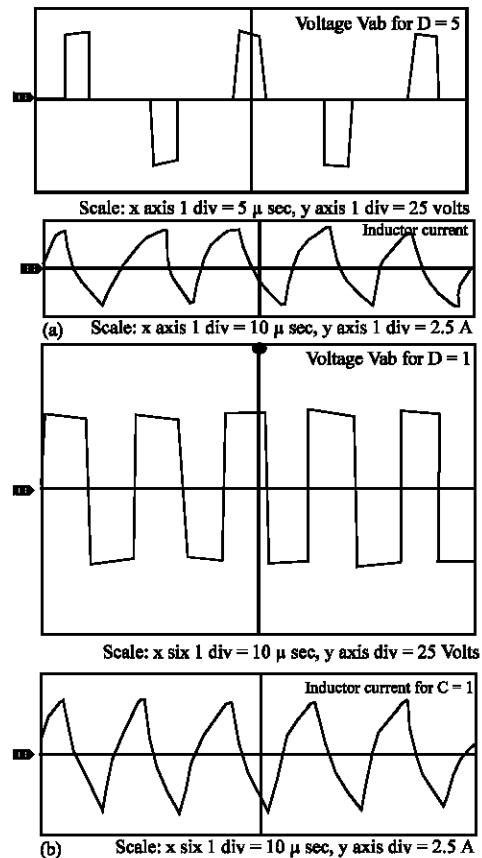
Fig. 7: Experimental results of series parallel resonant converter across V_{AB} and series inductor current at(a) 25% of load and (b)100% of load

Table 1: Comparison of results between simulated calculated and experimental series parallel resonant converter for I/PD-C supply voltage = 50 V and switching frequency = 50 kHz

Load (%)	Inductor current (peak) simulated	Inductor current (peak) experimental	Inductor current (peak) calculated	Series capacitor voltage (peak) simulated	Series capacitor voltage (peak) experimental	Series capacitor voltage (peak) calculated	Parallel capacitor voltage (peak) calculated	Parallel capacitor voltage (peak) experimental	Parallel capacitor voltage (peak) simulated	Output voltage
100	2.90	3.2	2.86	134.60	140.5	131.36	51.39	46.9	52.26	40
75	2.76	2.9	2.69	124.40	126.8	116.80	49.17	44.7	49.37	40
50	2.61	2.4	2.57	112.36	114.7	104.87	43.45	39.4	45.44	40
25	2.45	2.6	2.39	110.93	103.4	99.76	40.76	36.2	41.15	40
10	2.28	2.4	2.28	102.10	99.80	96.02	34.10	30.6	35.40	40
5	2.15	2.3	1.95	96.78	95.60	93.26	30.60	27.4	31.40	40
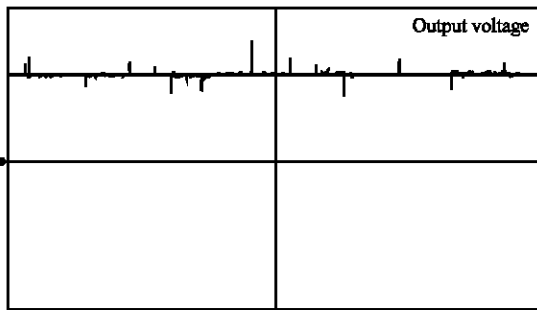
Scale: x axis 1 div = 10 µ sec, y axis = 1 div = 25 volts

Fig. 8: Output across the load at 25% load

CONCLUSIONS

In this dissertation series-parallel resonant DC-to-DC converter has been proposed. This study has led to identification of mode of operation of the converter. For the mode of operation type of switches, diodes and snubber needed have been discussed thoroughly. Converter is analyzed using complex ac circuit analysis method. The analysis presented was used to obtain the design curves. A simple design procedure has been illustrated using a design example of 100 W resistive load. Detailed PS-PICE simulation results have been presented to evaluate the performance the converter. Experimental output is taken. The calculated values, simulated values and the experimental values show very less deviation. So series parallel resonant converter can be used for very large load variation to maintain constant DC output voltage with less loss.

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