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# High-performance Optical Receivers Using Conventional Sub-micron CMOS Technology for Optical Communication Applications

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**Abstract:** A novel sub-micron total-CMOS common-gate Transimpedance Amplifier (TIA) has been designed for high-speed optical communication applications. This total-CMOS approach has given a tremendous flexibility in optimizing the circuit for high performance. The new design shows superior performance compared to recent common-gate and common-base TIAs. Using conventional 0.8 μm CMOS process parameters, simulations showed a transimpedance gain of 69.0 dB over a 3.5 GHz bandwidth, approaching the technology $f_T$ of 10 GHz. The mean input referred noise current density was calculated to be 21.2 pA/Hz$^{0.5}$ at 3.5 GHz, giving an input optical sensitivity of -20.4 dBm for a BER of $10^{-9}$. This allows a data transmission easily at 2.5 Gbps for a NRZ synchronous link. The power consumption is only 44 mW when AC coupled to a 50 Ω load. In addition, the TIA was designed to tolerate a relatively wide variation in bias conditions while preserving stability. Moreover, simulations using a 0.6 μm CMOS process showed even lower noise and wider bandwidth now at 6.0 GHz. The new design approaches similar IC designs in Si-bipolar or GaAs technologies. The design is the first reported TIA, which combines such features and using conventional 0.8 μm CMOS transistors with $f_T$ = 10 GHz.

**Key words:** Optical receiver, CMOS technology, transimpedance gain, low noise, low power

## INTRODUCTION

The rapid increase of data traffic, as a result of the growth of internet and intranet, has demanded huge capacity of optical communication systems. For such demands, GHz systems are actively investigated. Of prime interest is the preamplifier circuit in the receiver front-end of an optical link since it determines the overall performance of the system. Recently, such circuits have been implemented using various technologies such as GaAs, Si-bipolar and CMOS (Ciofi, 2006; Halkias *et al*., 2000; Liu *et al*., 2000). The CMOS technology has the advantages of low-power dissipation, high integration, low cost and easy to access and integrate with other application circuits (e.g., automatic gain control amplifier, digital data recovery, demultiplexer, etc.). CMOS optical receivers have been realized in sub-micron technologies, but still lag behind in performance as compared to their GaAs or Si-bipolar counterparts. Design of low-power wide-band CMOS transimpedance amplifiers is thus an important issue in wire-line broad-band communication circuit techniques. In addition to the wide bandwidth, the transimpedance amplifier requires high transimpedance gain in conjunction with low input referred noise for reliable operation at low photodiode input currents (Hasan, 2005).

This study presents a high-performance 3.5 GHz TIA based on a novel total-CMOS configuration for high-speed optical communication applications. The new configuration is optimized for implementation within the well-established 0.8 μm CMOS technology.

## CIRCUIT DESIGN AND SIMULATION RESULTS

A simple design topology has been adopted for the TIA as shown in Fig. 1. It consists of an input common-gate stage ($M_1$), followed by a common-source voltage gain stage ($M_2$) with a common-source active-load configuration acting as a current mirror ($M_5$) and an output buffer stage ($M_6$) in a source-follower configuration to drive the 50 Ω load. A pin photodiode is used as an input device.

What is novel about this design compared with previous common-gate schemes is that it is a total-FET based approach. That is, solely FETs are used to bias, load and buffer stages. Also, the feedback resistor is connected from the output to the drain of $M_1$ and not to the source of $M_1$, as would be the conventional case.

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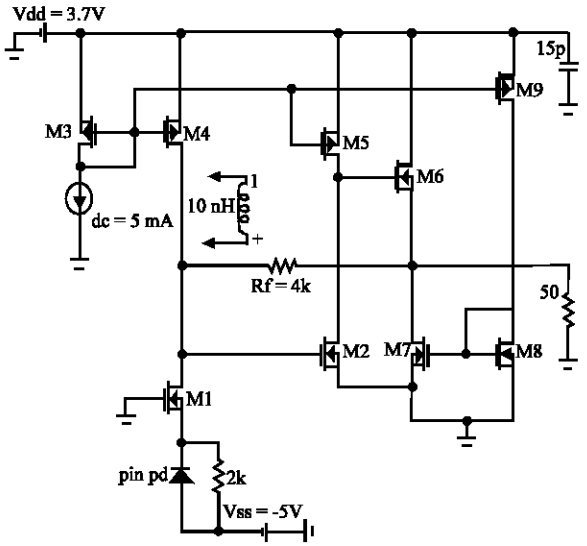


Fig. 1: Common-gate CMOS optical receiver

The simultaneous use of FETs for biasing and stage isolation results in a lower DC power dissipation and allows to optimize the size of transistors for high gain, wide bandwidth, low noise, wide dynamic range and a good bias tolerance while maintaining device processing yield high. For example, the size of $M_1$ and $M_4$ can be optimized to minimize their noise contribution and maximize the amplifier bandwidth. Also, the size of $M_5$ can be optimized to maximize the voltage gain of $M_2$ and hence that of the TIA, while maintaining power dissipation low. In addition, the size of $M_6$ can be optimized for a wider output swing. Also, FETs provide better isolation between stages.

The feedback scheme adopted makes the-3dB bandwidth of the amplifier totally independent of the photodiode input capacitance, which determines only a non-dominant pole since the input resistance of $M_1$ is small (Toumazu and Park, 1996). The-3dB bandwidth of the amplifier is given by Laker and Sansen, (1994).

$$f_{-3dB} \cong \frac{(1+A_{v2})}{2\pi C_T R_f} \quad (1)$$

with

$$C_T = C_{gd1} + C_{gs2} + (1+A_{v2})C_{gd2} \quad (2)$$

where $A_{v2}$ is the voltage gain of $M_2$, $C_{gs2}$ is the gate-to-source capacitance of $M_2$ and $C_{gd1}$ and $C_{gd2}$ are the gate-to-drain capacitances of $M_1$ and $M_2$, respectively. The dominant pole of the amplifier depends mainly on the

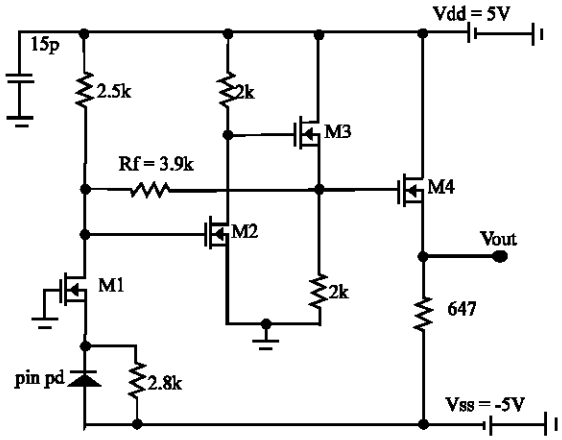


Fig. 2: Common-gate CMOS TIA

input capacitance of $M_2$ with Miller's effect, the drain capacitance of $M_1$ and the feedback resistor $R_f$ as shown in Eq. (1). Therefore, $M_1$ can be made wider to reduce its input resistance and optimize its noise contribution. Since $M_2$ is a much smaller device, its net input capacitance is small and hence $R_f$ can be made larger for the same equivalent bandwidth, which would consequently result in a lower overall noise.

The accurate prediction of the DC operating point of such a circuit is of critical importance because the various stages are bias interdependent. Extensive DC analysis and optimization of the circuit was performed. The goal to accommodate a low DC power consumption, a large bandwidth, a relatively wide variation in bias conditions, to preserve stability and to insure bias insensitivity within a relatively large range of supply voltages has been successively met. The optimum size, for a channel length of L = 0.8 μm, was found to be W = 400 μm and W = 25 μm for $M_1$ and $M_2$, respectively.

The positive and negative supply voltages $V_{dd}$ and $V_{ss}$ can be varied within the range from +3.3 to 6.0 V and from -5.4 to -4.4 V, respectively, without performance degradation. The DC power consumption is as low as 44 mW being ac coupled to the load and 100 mW when it is DC connected to the load. The bias circuitry consumes an additional 30 mW.

Simulations were conducted to compare the new design with published CMOS common-gate (Toumazu and Park, 1996) and BiCMOS common-base (Vansiri and Toumazou, 1995) designs (Fig. 2 and 3, respectively).

The 10 GHz $f_T$ silicon CMOS parts of the conventional 0.8 μm CMOS technology have been used. All designs presented here were optimized to have a bandwidth of 3.5 GHz.

Figure 4 shows the simulated transimpedance gain versus frequency for the three designs. It was assumed

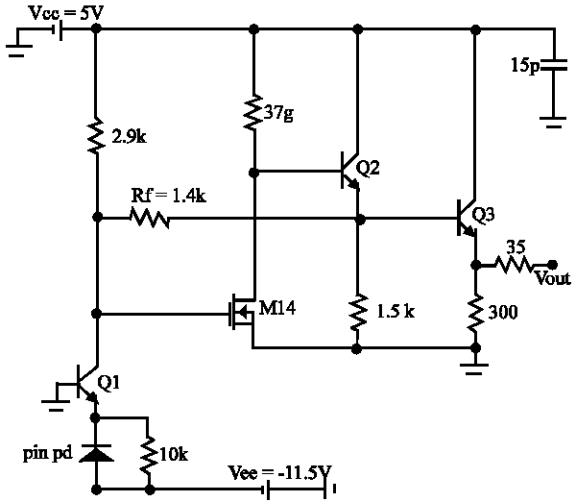


Fig. 3: Common-base CMOS TIA

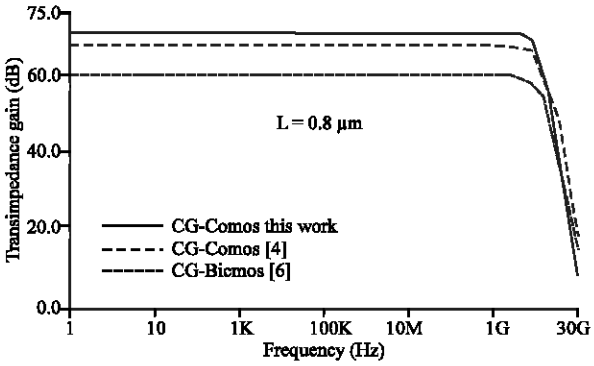


Fig. 4: Transimpedance gain vs frequency for L = 0.8 µm and 30 GHz bandwidth

that the amplifier is driving a load of 50 Ω, the input is driven by an AC current source and a 0.32pF pin photodiode is connected at the input.

For a 3.5 GHz bandwidth, the transimpedance gain of the new TIA is as large as 69.0 dB, at least 2.6 dB higher than in (Toumazu and Park, 1996) and (Vanisri and Toumazu, 1995). This confirms that TIA design based on a total-CMOS approach, allows better optimization that would not have been so, otherwise (Ikeda *et al*., 2001). This is quite important since this approach only uses MOS devices. The 3.5 GHz bandwidth was achieved without capacitive or inductive peaking. Inductive peaking increased the bandwidth to 4.0 GHz by canceling the pole present at about 3.3 GHz, but degraded the amplifier stability.

Figure 5 shows the transient response of the three TIAs when driven by a 2.5 Gbps input current pulse train. The response of the new design clearly reaches 300 mV

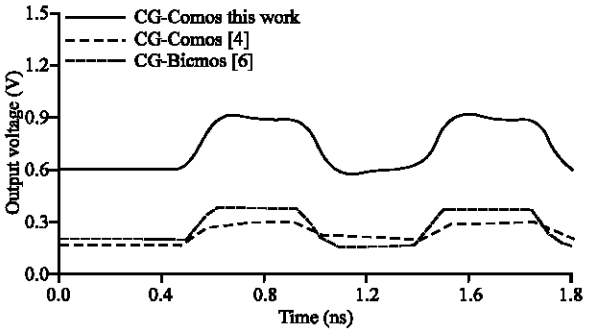


Fig. 5: Transient response of the TIA at 2.5 Gbps for 100 µA pulse input current signal

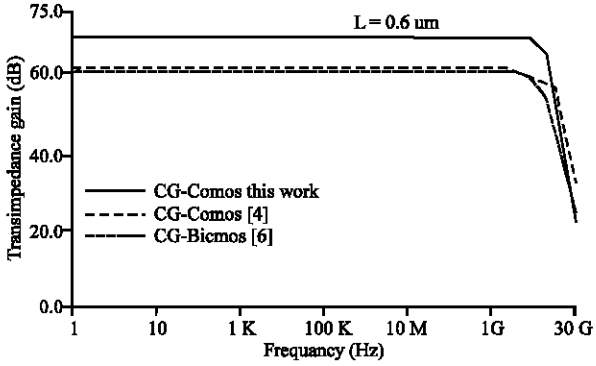


Fig. 6: Transimpedance gain vs frequency for L = 0.6 µm and 30 GHz bandwidth

output swing for 100 µA input current. Toumazu and Park, (1996) and Vanisri and Toumazu,( 1995). According to the above results, one can expect a sufficiently open eye diagram at 2.5 Gbps for NRZ synchronous links.

Further simulations, shown in Fig. 6, have been carried out for the previous circuits using 0.6 µm pure CMOS process parameters. Results are showing bandwidth higher than 6.0 GHz for all circuits. The same feedback resistor achieves this performance for the present work.

## NOISE ANALYSIS

A critical aspect of the design phase was the optimization of the feedback resistor $R_f$ as well as the width of the input and amplifier transistors in a tradeoff between gain, bandwidth, noise and DC power consumption. The noise model, used to calculate the noise components, combines the conventional FET rms noise theory with the optical preamplifier (OEIC) noise theory (Smith and Personick, 1980; Minasian, 1987). The input-referred equivalent noise current spectral density is approximately given by:

$$S_{eq}(f) = \frac{4kT}{R_f} + \frac{4kT}{R_s} + 2qI_{g1} + 2qI_{g2} + \frac{4kT\Gamma}{g_{m1}}\left[\frac{1}{R_s^2} + (2\pi f)^2\left(C_d + C_{gs1}\right)^2\right] + \frac{4kT\Gamma}{g_{m2}}\left[\frac{1}{R_f^2} + (2\pi f)^2\left(C_{gd1} + C_{gd2} + C_{gs2}\right)^2\right] \quad (3)$$

In Eq. (3), k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, $I_{g1}$ and $I_{g2}$ are the gate leakage currents of $M_1$ and $M_2$, respectively, Ã is the excess noise factor equal to 1.7 to account for the short-channel effects, $g_{m1}$ and $g_{m2}$ are the transconductances of $M_1$ and $M_2$, respectively, $C_d$ is the capacitance of the pin photodiode and $C_{gs1}$ is the gate-to-source capacitance of $M_1$.

Two assumptions are made in Eq. (3). First, the total $S_{eq}(f)$ is the result of the input stage and the second stage (Toumazu and Park, 1996; Vanisri and Toumazu, 1995) because current gain in the first stage is unity. Second, the noise contribution of the FET loads $M_4$ and $M_5$ is negligible (Abidi, 1988; Haralabidis *et al*., 2000).

The first two terms in Eq. (3) represent thermal noise contributions by $R_f$ and $R_s$. The next two terms are noise contributions by gate leakage currents, which can be neglected (Toumazu and Park, 1996). The last two terms represent the channel thermal noises of $M_1$ and $M_2$.

In this design, a judicious choice (Abidi, 1988) through successive cycles of DC and RF simulations, has concluded that the optimum value of $R_f$= 4 kΩ allows the desired transimpedance gain and the minimum input noise current density over the bandwidth of DC-3.5 GHz to be achieved. Load FETs $M_4$ and $M_5$ are designed so that their noise contribution becomes negligible (Abidi, 1988).

The conventional total noise spectral density as calculated using Eq. (3) over a 4 GHz bandwidth is shown in Fig. 7. The results from Toumazu and Park, (1996) and Vanisri and Toumazu, (1995) are also shown. All designs show similar noise spectral densities up to around 1.0 GHz. However, above 1.0 GHz the common-base design gives lower noise spectral densities.

The components due to the thermal noise of the resistors in all designs were found to dominate the total noise below 1 GHz. The higher noise densities of the two common-gate designs may be accounted for by the increased channel thermal noise of their FETs in the high frequency range. This noise component was found to become dominant at high frequencies. Also, the higher transconductance of the BJTs in the common-base configuration favors the lower noise densities observed at high frequencies. The mean equivalent input noise

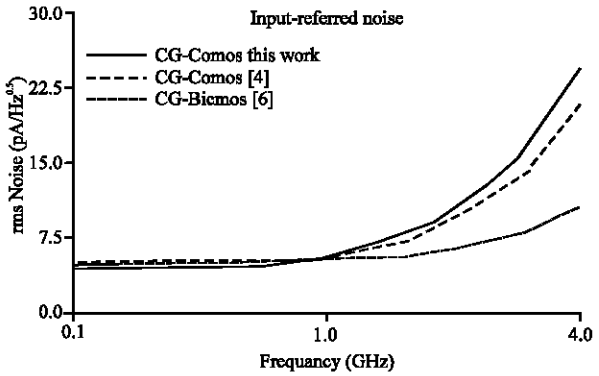


Fig. 7: Total mean input-referred current noise for L = 0.8 μm and 4.0 GHz bandwidth

current density of the new common-gate design was 21.2 pA/Hz$^{0.5}$ at 3.5 GHz. In fact, this was achieved through a careful optimization process since at this frequency the size of FETs determine the overall noise density which trades off with other performance characteristics, as mentioned before. The FET size of the input stage has big effect on the total noise at frequencies greater than 1.0 GHz. However, below 1.0 GHz, little improvement was found from the optimization of the size of the transistors since the thermal noise of the resistors dominates in this frequency region. This indicates that the total-CMOS approach adopted here is important in optimizing noise in the high frequency region.

Using the previous value of the equivalent input-referred noise current density, one calculates (Smith and Personick, 1980) that the input optical sensitivity for a BER of $10^{-9}$ is as low as -20.4 dBm. The corresponding dynamic range is calculated to be 25.5 dB for 500 mV peak output voltage swing. If a wider dynamic range is desired, an automatic gain-control circuit must be added. The above results were obtained assuming a pin PD with 75% quantum efficiency in 0.850 nm wavelength.

Noise simulations, shown in Fig. 8, have also been conducted using a 0.6 μm CMOS process. Results show that the total rms noise current densities are at least, in electrical terms, 1 dB lower in the frequency range above 4.0 GHz. This result, combined with the higher bandwidth result obtained previously for the same process, indicates that the new approach is valid for shorter channel CMOS processes.

Noise reduction using inductive effects (Abidi, 1988), are being studied. Preliminary results show that a 10-15 nH inductor (realizable monolithically) added in series with $M_4$, as shown in Fig. 1, reduces significantly the total rms noise current density above 1.0 GHz. A

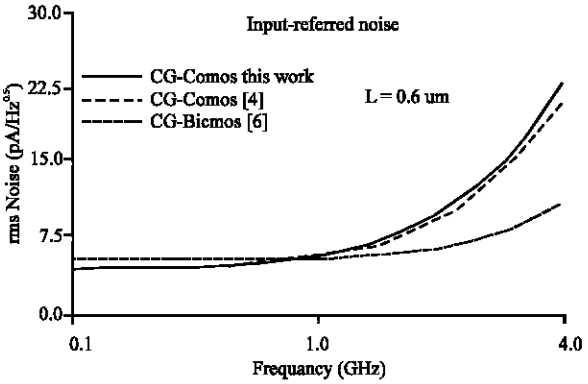


Fig. 8: Total mean input-referred current noise for L = 0.6 μm and 4.0 GHz bandwidth

Table 1: CMOS TIA design parameters

| | |
|---|---|
| -3 dB Bandwidth | 3.5 GHz |
| Transimpedance gain | 69.0 dB |
| Mean input current noise density | 21.2 pA/Hz$^{0.5}$ |
| Power dissipation | 44 mW |
| Input optical sensitivity | -20.4 dBm |
| IC technology | 0.8 μm CMOS |

deliberate study in this area and which takes into account other noise components as well as noise contribution by the pin photodiode in sub-micron technology, is being conducted.

The main design parameters of the new common-gate TIA are summarized in Table 1. This design performance compares well with similar IC Si-bipolar or GaAs technologies (Liu *et al.*, 2000; Minasian, 1987), dominating the GHz optical communication market for several years. The design also gives better performance features when compared to Park and Yoo (2003).

## CONCLUSIONS

A novel sub-micron total-CMOS common-gate transimpedance amplifier has been designed for optical communication applications. This total-CMOS approach has given more flexibility to optimize the circuit in order to achieve high performance. The new design shows superior performance compared to recent common-gate and common-base TIAs. Simulated results, using conventional 0.8 μm CMOS technology parameters, have shown a high transimpedance gain of 69 dB over a 3.5 GHz bandwidth, which is close to the technology $f_T$ of 10 GHz. In addition, the equivalent input noise current density as well as the DC power consumption have been minimized. The new design shows even lower noise and wider bandwidth now at 6.0 GHz, using a 0.6 μm pure CMOS technology. The above performance fairly approaches that obtainable with similar Si-bipolar or GaAs technologies. While optimizing the design for bandwidth, low noise and low power, little attention has been given to dynamic range and signal swing. However, now that the design is demonstrated, further work is aimed at optimizing other performance features.

## ACKNOWLEDGMENTS

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