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Design of Speed Independent Ripple Carry Adder

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Abstract: Any physical methods logic circuit design is based on using formal models of gates and wires. The simplest model of a gate is determined by only two parameters: (a) Boolean function is to be calculated, (b) fixed propagation delay. The simplest model of a wire is an ideal medium with zero resistance and consequently, with zero delay. In this study we propose an approach based on the physical nature of transitions in CL, using this idea for the design of speed independent ripple carry adder. We believe that each transition is actually a transfer of energy which can be naturally detected by physical methods.

Key words: Adder, speed independent, CL (combinational logic), Boolean function, OVD (output validity detector), SPPs (signal propagation paths)

INTRODUCTION

In speed-independent circuits transition duration can be arbitrary. So a centralized clock cannot be used. Instead special circuitry to detect output validity is applied. Besides, additional interface circuitry is needed to communicate with the environment in a handshaking manner. A speed-independent circuit can be seen as a module consisting of Combinational Logic (CL) proper, CL Output Validity Detector (OVD) and interface circuitry (Fig. 1). To enable OVD to distinguish valid output data from invalid ones, the redundant coding scheme was proposed (Thil, 2004). The main idea of the scheme is to enumerate all possible input and output data, both valid and invalid. The OVD must be provided with appropriate information on data validity. To realize the idea of redundant coding some constraints on CL design are imposed (Cheng, 2003).

- CL must be free of delay hazards, i.e., CL output data word must not be dependent on the relative delay of signal paths through CL.
- In changing between input states, any intermediate or transient states that are passed through must not be mapped by CL onto valid output states.

When these constraints were formulated, the circuit designers realised that not every Boolean description could be implemented in a speed-independent style. Other approaches to speed-independent module design were needed.

SIM design as a science has two branches: logical and physical. For a long time physical branch was overshadowed in spite of its competitiveness. The main properties of physical approach to SIM design are:

- Arbitrary coding scheme.
- Conventional procedure of operational unit design.
- Races of signals in SIM do not affect on its proper operation.

In this study we propose an approach based on the physical nature of transitions in CL. We believe that each transition is actually a transfer of energy which can be naturally detected by physical methods.

From the viewpoint of a radio engineer CL behaves like a radio transmitter. It emits radio frequencies in the 10^8-10^{10}Hz band modulated by signals of 10^6-10^8Hz. Obviously, the carrier wave is produced by gate switchings during transitions in CL. The modulating wave is produced by control schemes (OVD and interface circuitry) that detect transition completion and inform the environment about the readiness of CL. OVD is a kind of radio receiver that extracts the modulation envelope and

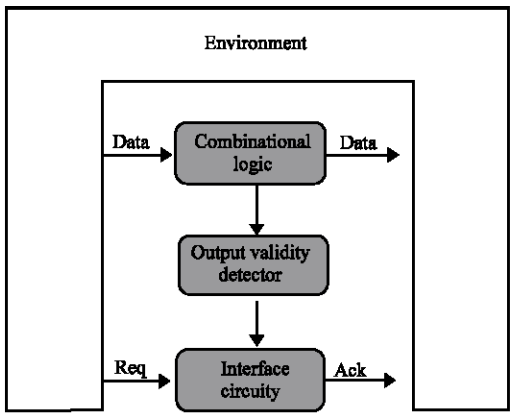

Fig. 1: General structure of speed independent logic circuit

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enhances the received signal. The main properties that OVD circuit must expose from a radio engineer's point of view are selectivity and high gain. Since the useful signals can propagate through non-conducting medium, OVD circuits can be coupled with CL indirectly.

Advances in semiconductor technology gave birth to two methods of transition detecting based on two kinds of the information carrying signal, namely electromagnetic radiation and current consumption. Frequency of the signal produced by switching logic gates is determined by gate delay.

For instance, CMOS network of 1-ns gates produces 1-GHz signal, ECL array of 100-ps gates gives 10-GHz radiation. Logic circuits consisting of 10-ps gates will emit infra-red radiation. That signal could be easily detected by photosensitive devices.

CURRENT CONSUMPTION DETECTION

Using current consumption of CMOS CL for output validity detection was proposed in 1990 (Izosimov *et al*., 1990). Contrary to the method of EMR detection this one is based on introducing direct coupling of source and receiver. While CL is in steady state it consumes current of about 10^{-9}-10^{-8}A which does not allow OVD switching. The interface circuitry gets information on CL output validity and in turn informs the environment about CL readiness to input data processing. When an input data arrives CL changes its state to transient, current consumption increases to 10^{-4}-10^{-2}A, which switches the OVD, thus informing the interface circuitry about output invalidity. The latter lets the environment know about CL business.

After the computations in the CL are finished, the current consumption decreases down to the steady state value and the OVD sends a signal of output validity.

Information carrying signal: Current consumption by CMOS CL contains useful information on CL state. CMOS CL is a network of CMOS gates, so the current consumed by CL is a superposition of currents consumed by CMOS gates included in the CL. Each CMOS gate contains PMOS transistor and NMOS transistor networks (Fig. 2). While a gate is in a steady state either the PMOS or the NMOS network is in a conducting mode. When a gate switches the non-conducting transistor network becomes conducting. There is usually a short period in switching time when both networks are in a conducting mode.

Generally, current consumed by a CMOS gate includes three components:

- Leakage current I_{lk} passing between power supply and ground due to finite resistance of non-conducting transistor network;

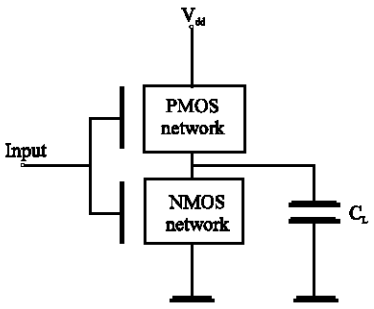

Fig. 2: Basic CMOS gate

- Short-circuit current I_{sc} flowing while both networks are in a conducting mode;
- Load capacitance C_L charge current I_{LC} flowing while a CMOS gate is switching from low to high output voltage via conducting PMOS network and C_L.

Spice simulation has shown (Thiel, 2004) that amplitude of current consumed by a typical CMOS inverter depends on C_L and is limited by the non-zero resistance of the conducting PMOS network (Fig. 3a). The integral of consumed current is proportional to C_L. When a gate switches from high to low output voltage, the component I_{LC} is negative by direction and negligible by value (Fig. 3b). It is evident, the switchings from high to low output voltage occur at the expense of energy accumulated in C_L during the previous switching from low to high output voltage. The component I_{sc} does not depend on direction in which a gate switches.

The component I_{LC} equals to $I_{LC} = C_L.V_{dd}.f$ where V_{dd} is a power supply voltage, f is a gate switching frequency. David Harris has investigated the component I_{sc} dependencies on C_L and rise-fall time of input potential signal. He showed that if both input and output signal have the same rise-fall time, the component I_{sc} cannot be more than 20% of summary current consumption (David Harris, 2001). However, when the output signal rise-fall time is less than input one, the component I_{sc} can be of the same order of magnitude as I_{LC}. In that case it must be taken into account. As to the component I_{lk}, it entirely depends on CMOS process parameters and for state of the art CMOS devices I_{lk} is about 10^{-15} -10^{-12} A.

So, the analysis of CMOS gate current consumption allows us to conclude that in transient state a CMOS gate consumes a current $I_\Sigma = I_{lk}+I_{sc}+I_{LC}$ and in steady state it consumes only $I_{lk} << I_\Sigma$. The difference between two states from the viewpoint of current consumption is several orders of magnitude. So, CMOS gate output validity detection is possible, both in principle and in practice.

Here we presented series-parallel model of computations in CL. We showed that in every moment

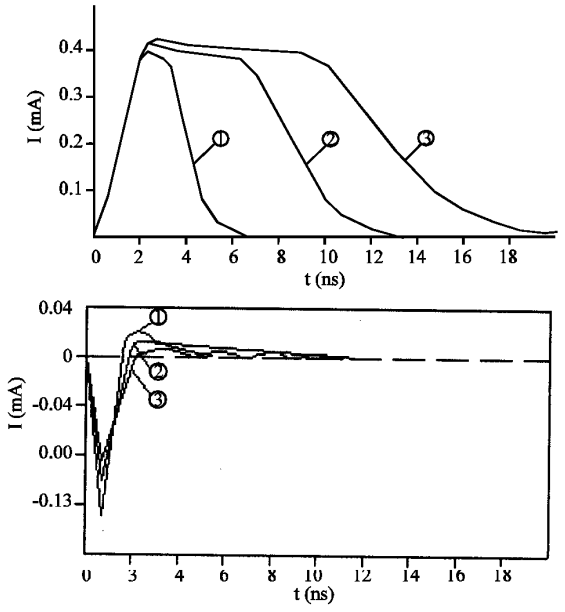

Fig. 3: CMOs gate AC characteristics (a) swishing from low to high; (b) swishing from high to low

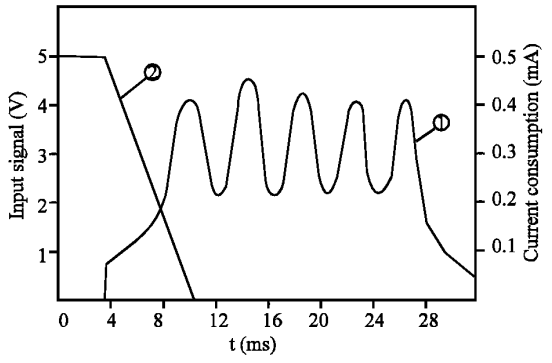

Fig. 4: Current consumed by a ten inverter chain (1) in response to input voltage signal (2)

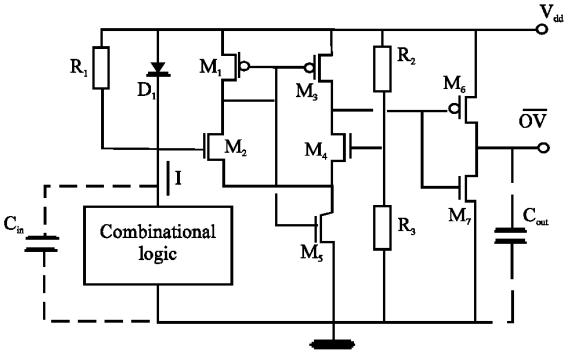

Fig. 5: The output validity detector

during switching current consumed by CL is a superposition of the currents consumed on the activated Signal Propagation Paths (SPPs). Now, considering CL implemented by CMOS devices we should note that while logical signal propagates through SPP the neighbouring gates switch in opposite directions. That is why a curve of current consumed by a ten inverter chain (Fig. 4) looks like a combination of crests and troughs. Nevertheless, in the very lowest point of the curve the current consumed by CL in a transient state remains several orders more than in a steady state.

OVD implementation: The proposed OVD circuit, shown in Fig. 5, is a threshold circuit translating an analog current signal I into a logical signal OV.

The OVD circuit contains a Current-to-Voltage Converter (CVC) consisting of the resistor R_1 and the diode D_1. The OVD also contains a comparator implemented by the MOS transistors M_1-M_7 and resistors R_2,,R_3. CMOS CL consumes the current I and introduces a capacitance C_{in}. The capacitance C_{out} represents the load caused by the interface circuitry. A low potential output signal of OVD corresponds to CL output validity. A high potential output signal corresponds to CL output invalidity. So, OVD generates OV signal in negative logic manner.

The transfer characteristics of CVC is determined by a system of three equations:

$$\begin{cases} I = I_r + I_d & (1) \\ \Delta V = \varphi_T \cdot \ln(I_d / I_0) + I_d r_b & (2) \\ \Delta V = I_r R_1 & (3) \end{cases}$$

where:

I = Input current of CVC
ΔV = A voltage drop on the CVC circuit
I_r = A current flowing through the resistor
R_1, I_d = Is a current passing through the diode
D_1, I_0 = A leakage current of the diode
r_b = Bulk resistance of the diode
φ_T = Stands for kT/q
k = Boltzmann's constant
T = Absolute temperature
q = charge of an electron.

Equations 1-3 determine the functional connection F between input current I and voltage drop ΔV:. $\Delta V = F(I)$ Graphic solution of the system is shown in Fig. 6.

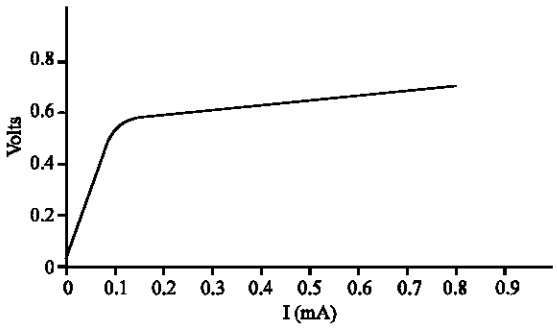

Fig. 6: Current-to-voltage converter characteristics

CVC parameters to be calculated are R_1 and r_b. Initial data for calculating R_1 are the threshold voltage drop ΔV_{th} and corresponding threshold input current I_{th}. Value I_{th} is determined by minimal current consumed by CMOS CL in transient state. Initial data for calculating r_b are maximal voltage drop Δ_{vmax} and corresponding maximal input current I_{max}. Value I_{max} is determined by the maximal number of gates in CL switching simultaneously and their load capacitances.

The comparator chosen is the CMOS ECL receiver proposed by (Izosimov *et al*., 1990). The circuit includes a single differential amplifier stage with built-in compensation for parameter variations, followed by a CMOS inverter. The comparator has 100 mV worst-case sensitivity in 1 m technology. Detailed static and dynamic analysis of the comparator circuit was given in (Izosimov *et al*., 1990).

The comparator compares input voltage signal V_{in} with reference voltage V_{ref}. If $V_{in} < V_{ref}$ the comparator output signal equals to logical zero which means that CL outputs are valid. Otherwise, $V_{in} > V_{ref}$, the comparator output signal equals to logical one which means that the outputs are invalid.

As it follows from the OVD circuit configuration,

$$V_{in} = V_{dd} - \Delta V \quad (4)$$

$$V_{ref} = V_{dd} \cdot \frac{R_3}{R_2 + R_3} \quad (5)$$

where V_{dd} is a voltage of power supply.

Equations (4) and (5) allow us to calculate the threshold voltage drop ΔV of the CVC circuit:

since, $$V_{dd} - \Delta V_{th} \approx V_{dd} \cdot \frac{R_3}{R_2 + R_3}$$

so $$\Delta V_{th} \approx V_{dd} \cdot \frac{R_2}{R_2 + R_3} \quad (6)$$

Table 1: Typical element values for the OVD circuit

Element	Value
Diode	$r_b = 100\ \Omega$
Resistors	$R_1 = 5.0\ k\Omega$
	$R_2 = 4.0\ k\Omega$
	$R_3 = 46.0\ k\Omega$
Power supply	$V_{dd} = 5.0$ V

If $0 < \Delta V < 500$ mV then the diode D_1 of CVC operates in the very small current region $I_d \approx 0$ and $I_d << I_r$.

So the component I_d in the Eq. 1 can be neglected and $I \approx I_r = \Delta V / R_1$.

For practical values of the ΔV_{th} threshold input current of the OVD circuit is reversely proportional to the resistance of R_1:. $I_{th} = \frac{1}{R_1} \cdot \Delta V_{th}$ Substituting Eq. 6 yields.

$$I_{th} = \frac{1}{R_1} \cdot \frac{R_2}{R_2 + R_3} \cdot V_{dd}$$

As to choosing value of r_b it must be done with regard to maximal voltage drop ΔV_{max}.

If $\Delta V > 750$ mV, the diode D_1 is in active mode and while $r_b << R_1$ the condition $I_r << I_d$ is true. So, in the large current region $I \approx I_d$ and Equation (2) determines an almost linear dependence between I and ΔV. For instance, if the maximal voltage drop $\Delta V_{max} = 900$ mV and maximal input current $I_{max} = 2$mA, then in accordance with the Equation (2) $r_b \approx 100\Omega$. Typical element values for the OVD circuit with $\Delta V_{th} = 400$ mV are given in Table 1.

The turn-on t_{on} and turn-off t_{off} delays of the OVD circuit depend on the OVD itself and the CMOS CL as well. (Switching the OVD output from low to high voltage is called turning-on and reverse switching is called turning-off).

Consider a piece of CMOS CL and its interaction with OVD circuit (Fig. 7). The piece is an SPP including N logic gates. Each gate is shown symbolically as a connection of PMOS and NMOS networks. All the capacitances affecting t_{on} and t_{off} can be brought down to three components:

- C_{Li} is the load capacitance of the I-th gate;
- C_{psi} is the power supply bus capacitance associated with the I-th gate;
- C_{in} is the input capacitance of the OVD circuit.

Let p_i is a probability of the I-th gate being in the state of high output potential. In this state the capacitance C_{Li} is connected with power supply bus through the low channel resistance of turned-on transistors in PMOS network of the I-th gate. Then

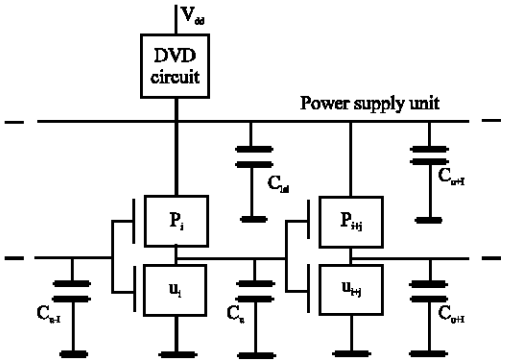

Fig. 7: Interaction of CMOS CL and the OVD circuit

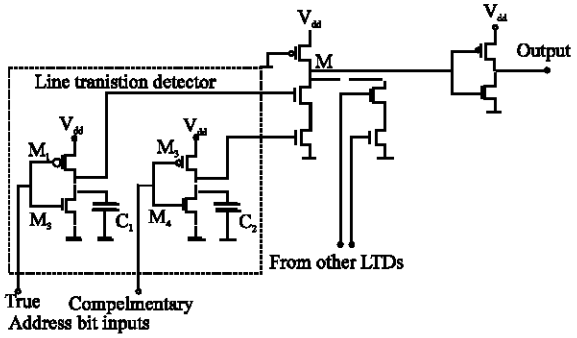

Fig. 8: CMOS bus transition detector

equivalent capacitance C_{eq} connected to the OVD circuit input equals

$$C_{eq} = C_{in} + \sum_{i=1}^{N} (p_i C_{Li} + C_{psi}) \quad (7)$$

where N is a number of gates in the considered SPP. Here the resistance of conducting PMOS network is assumed to be negligible.

Equation 7 is also true for CL including several SPPs. In that case summing must be carried out for all the gates belonging to CL.

Simulation shows that t_{on} and t_{off} are proportional to the OVD time constant $\tau = R_i C_{eq}$. It was also obtained that when N>20, the component under the sign of summation in Eq. (7) can be much larger than the component C_{in}. Due to voltage drop ΔV the effective power supply voltage is reduced and CL performance is decreased by about 35% (Yeh and Jen, 2000).

In order to make SIM operating faster special attention must be paid to reducing the capacitance introduced by CL.

Speed-independent address bus: The simplest case of CL is a scheme degenerated into a set of wires called a multi-bit bus. Let us develop the OVD circuit for such a CL.

Multi-bit bus consists of several lines. Each line can be considered as a medium for signal propagating from one end of the chip to another. Delay of signal propagation through a line depends on several factors (Ohban, 2002):

(a) Output impedance and symmetry of driver circuit;
(b) Initial state of the line: if driver is symmetrical, line switching from high to low voltage lasts shorter than reverse switching;
(c) Electrical properties of the line as a signal propagation medium (resistance of conducting layer and capacitances between the line and other wires next to it);
(d) Length of the line;
(e) Input impedance and sensitivity of receiving circuit.

Since different lines of the bus operate in different conditions (a-e), signal propagation delays are different, too. From the standpoint of environment the bus behaves like any other more complicated CL.

Asynchronous RAM designers use a bus transition detector since 2001 (Harris, 2001). Such a detector is usually based on double-rail address coding and two series connected transistors for each address bit. One of the transistors receives the true address signal and the other receives the complementary address signal of the particular address bit. For any steady state condition one of the transistors will be turned on and one will be turned off. There will be a finite rise and fall time during a transition of the address bit. There is a short time during which both transistors are conducting. The establishment of the conductive path provides the detection of the address transition. In the first asynchronous RAMs the output signal of the transition detector is used for bit line precharging and for enabling/disabling sense amplifiers and peripheral circuitry.

Self-timed RAM announced in 1990 (Izosimov *et al.*, 1990) used transition detectors not for address transition only but also for detecting read/write completion and address/bit line recharge completion as well.

The CMOS transition detector was invented in 1998 (Stelling *et al.*, 1998). This circuit is also based on double-rail coding and uses a pair of series-connected NMOS transistors (Fig. 8). The scheme for n-bit bus control

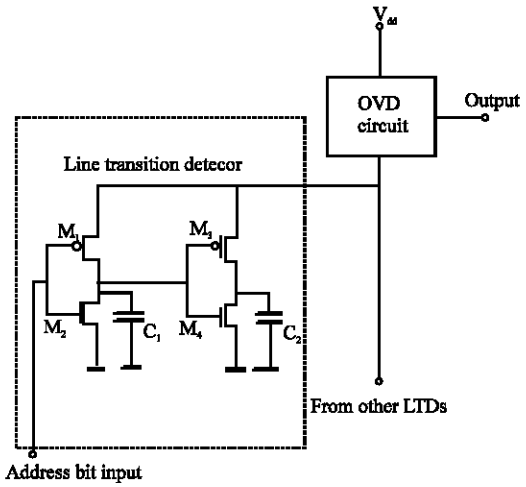

Fig. 9: Speed-independent bus

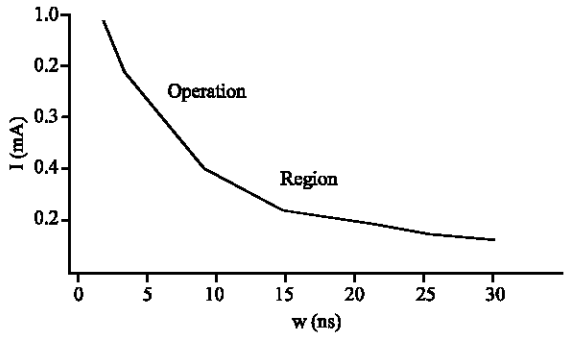

Fig. 10: Operation region of the OVD circuit

contains Line Transition Detectors (LTDs) and n AND-gates. Outputs of AND-gates are united in node M forming wired OR. The output inverter serves as a pulse shaper. Capacitors C_1 and C_2 are intended to prolong rise time of the LTD output signal (true and complementary). This is necessary for reliable detection.

The main drawback of the circuit is speed dependence. One can see that if true and complementary address bit signal have different propagation delays, the conducting path via NMOS transistors will never be formed.

Using the OVD circuit proposed in earlier as LTD we can avoid this drawback. Note that address transmission through the address bus is unidirectional. So to detect completion of bus transition it is enough to recognize the bus state at the destination end. For this purpose we modify CL to consist of n lines. The modification means introducing n LTDs, each actually a CMOS inverter chain. Each chain contains two inverters loaded with a capacitance (Fig. 9). Input of each LTD is connected with corresponding line of the bus at the destination end. Power supply pads of all LTDs are connected to the current input of the same OVD circuit.

The parameters of the input current signal for the OVD circuit are varied by

- Value of capacitances C_1 and C_2;
- Dimensions of MOS transistors M_1 -M_4.

Since all transitions in CL are of the same duration and can be lengthened to be outlast the OVD turning-on time, we simplify the interface circuitry by disallowing the asymmetrical delay.

Due to short duration of normal transition in this CL we must take into account the integral nature of the sensitivity of the OVD circuit. OVD sensitivity depends on both amplitude and width of input current pulse. Simulated operation region of the OVD circuit for current pulses shorter than 30 ns is shown in Fig. 10. It is obvious that in this case the threshold of the OVD circuit must be determined by threshold charge Q_{th} value. The OVD input charge Q equals

$$Q = \int_{t}^{t+w} Idt$$

to where I is OVD input current, t is a moment of time when transition occurs, w is a width of input current pulse. Turning-on condition for the OVD circuit is $Q = Q_{th}$.

The OVD circuit with typical parameters (Table 1) has a threshold charge value $Q_{th} = 4.0; 10^{-12}$ C. When $C_1 = C_2 = C_L$, the minimal value of C_L providing OVD capacity for operation is about $1.0.10^{-12}$ F.

Influence of transistors M_1 -M_4 dimensions on LTD delay d is determined by approximation:

$$d \sim \frac{1}{2} \cdot \left(\frac{1}{G_n} + \frac{1}{G_p} \right) \cdot C_L$$

where ~ is a sign of proportionality, G_n and G_p are the conductances of NMOS and PMOS transistors respectively ($C_L = C_1 = C_2$). Since

$$G_n \sim \left(\frac{W}{L} \right)_n \text{ and } G_p \sim \left(\frac{W}{L} \right)_p$$

where W and L are width and length of transistor channels of the corresponding conduction type, the LTD delay d is proportional to

$$\left(\frac{L}{W}\right)_n + \left(\frac{L}{W}\right)_p .$$

It has been obtained that for

$$\left(\frac{W}{L}\right)_n = 3.6 , \left(\frac{W}{L}\right)_p = 4.8 ,$$

C_L=1.0 pF and V_{dd}-ΔV = 5.0V the LTD delay d = 7.6 ns.

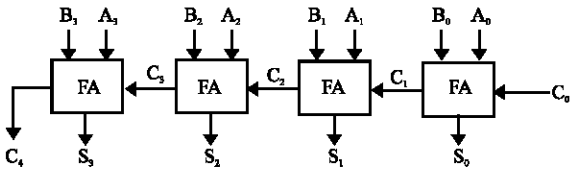

Fig. 11: General structure of a ripple carry adder

When LTD works jointly with the OVD in the speed-independent bus, the real value of the LTD delay will increase by 30-40% due to OVD's R_1 effect on the effective power supply voltage.

To determine the appropriate value of R_1 in the OVD circuit we must know threshold input current I_{th} corresponding to threshold voltage drop ΔV_{th} recommended to be equal to 400 mV.

Average input current I_{av} in transient state of one line is determined by the expression $I_{av} = C_L v$ where v is the average rate of increase in the output signal for an inverter included in LTD. For typical values $v = 1.010^9$ Volts per second and C_L = 1.0 pF, I_{av} = 1.0 mA. Accepting I_{th} = 0.4 mA and I_{max} = 2.0 mA we obtain R_1 = 1k and r_b = 100Ω.

Simulation has shown that in this case OVD turning-on delay can be approximated by an empirical expression: t_{on}(ns) = 8.1+0.1 n.

Where n is the address bus bit capacity. Total delay of recognizing address transition $t_{tot} = d\,g + t_{on}$ where g is a coefficient of the LTD delay increase due to reducing power supply voltage. As we showed above g 1.35. It can be seen that if n = 32, t_{tot} = 21.6 ns.

Speed-independent adder: The circuit we use in this section as a CL was a touch-stone for many speed-independent circuit designers for about four decades. We mean a Ripple Carry Adder (RCA) which is actually a chain of one-bit full adders (Fig. 11).

Each full adder calculates two Boolean functions: sum $s_i = a_i \oplus b_i \oplus c_i$ and output carry $c_{i+1} = a_i b_i + b_i c_i + a_i c_i$ where a_i, b_i are summands, c_i is input carry and stands for XOR operation.

As it was shown above the turn-on and turn-off delays of the OVD circuit are proportional to the equivalent capacitance C_{eq} associated with OVD circuit input. Capacitance C_{eq} depends linearly on a number of gates N in CMOS CL. To speed up a SIM it is necessary to reduce a number N. This can be reached by structural decomposition CMOS CL into subcircuits CL1, CL2, etc. Each subcircuit CLi is connected to its own detecting circuit OVDi or directly to the power supply if this subcircuit transition does not affect the transition duration in CL as a whole. Each detecting circuit OVDi generates its own OV signal which is combined with other OVDs' output signals via a multi-input OR (NOR) element. The output signal of that element serves as OV signal of the CMOS CL.

CONCLUSIONS

Despite the simplicity of addition, there isn = t a single best way to perform high-speed addition. The adder architectures are available from the simple but slow ripple carry adder to the fairly complex but fast carry look-ahead adder. The performance of adders also depends upon the choice of logic design style and the transistor sizes used. Hence there exist numerous possibilities of making changes in the adder designs because of which many designs can be developed and the performance of every design will differ from other designs.

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