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Sleep Transistor Sizing According to Circuit Speed, Silicon Area and Leakage Current in High-Performance Digital Circuit Modules

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Abstract: It is proposed that the power supply of key circuit modules could be gated to achieve significant reductions of leakage current, with minimal costs to circuit speed and die area in 0.25, 0.18 and 0.07 μm technologies. This study describes an extension to power supply gating using body overdrive and gate underdrive, analysis techniques to predict leakage current and performance parameters, a procedure for optimization of the sleep transistor size and simulation results that demonstrate the accuracy of the analysis and advantages of the approach. A leakage current estimation technique has been studied using the Berkeley Predictive Technology Model Parameters. An estimation technique has been verified using ISCAS85 combinational Benchmark test circuits. Finally the optimization algorithm has been verified using these same benchmark test circuits.

Key words: Low power, sleep transistor, sub-micron, leakage current, transistor scaling

INTRODUCTION

With the rapid progress in semiconductor technology, chip density and operating frequency have increased, making the power consumption in battery-operated portable devices a major concern. The goal of low-power design for battery-powered devices is to extend the battery service life while meeting performance requirements. Reducing power dissipation is also a design goal for non-portable devices since excessive power dissipation increases packaging and cooling costs and causes potential reliability problems.

Dynamic Power Management (DPM), which refers to a selective, shut-off or slow-down of system modules that are idle or underutilized, has proven to be a particularly effective technique for reducing power dissipation in such systems. Incorporating a dynamic power management scheme in the design of an already-complex system, however, is a difficult process that may require many design iterations and careful debugging and validation.

For the DPM approach to apply, it is required that each system module support at least two power states, ACTIVE and SLEEP. In the ACTIVE state, the module performs computations or provides services, while in the SLEEP state it does not perform any useful computation or service. It simply waits for an event or interrupt signal to wake it. The power consumed in the ACTIVE state is typically much higher than the SLEEP state, but SLEEP power, which depends on leakage current, is dramatically increasing in deep sub-micron technologies.

The goal of the study is to develop algorithms to predict the leakage current of deep sub-micron circuits in the SLEEP state and optimize the design of power supply gating with respect to ACTIVE performance and SLEEP power.

LEAKAGE CURRENT IN DEEP SUB-MICRON CMOS TRANSISTOR

Leakage current in short-channel MOS transistors results from a variety of mechanisms, as shown in Fig. 1 (Wilson, 2003). The most important components of leakage current are I_2, I_3 and I_7, which are weak inversion (sub-threshold), Drain Induced Barrier Lowering (DIBL) and gate oxide tunneling, respectively. Techniques described in this study serve to reduce DIBL-enhanced, sub-threshold leakage current.

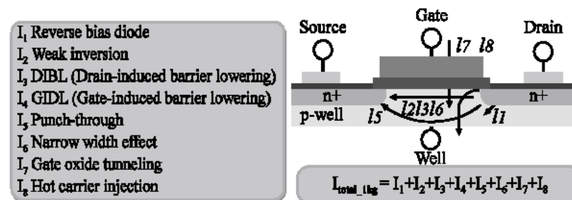

Fig. 1: Sources of leakage current in NMOS transistor

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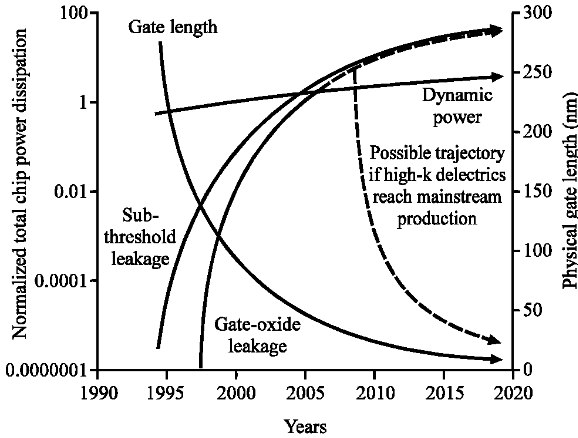

Fig. 2: Technology trend for both leakage current

Leakage current estimation is complicated by dependency of both the gate tunneling and sub-threshold currents on the nature of the input vector being applied to the test circuit. This input state dependency of sub-threshold leakage current has been extensively studied and exhibits the so-called stack effect (Siva *et al*., 2001).

Gate tunneling leakage current also depends on input state and on the device type. PMOS devices demonstrate gate oxide tunneling currents that are approximately one order of magnitude less than those in their NMOS counterparts. Furthermore gate oxide tunneling depends highly on gate oxide material and thickness. Technology trends show that new high-k dielectric materials might resolve VLSI gate leakage problems in the near future. Figure 2 shows total chip dynamic and static power dissipation trend forecasts based on the international technology roadmap for semiconductors (Sung Kim *et al*., 2003).

Models for CMOS leakage current: Sub-threshold channel current is the dominant leakage mechanism in deep sub-micron CMOS circuits. This V_{GS}/V_{SG} dependence of sub-threshold leakage current is modeled most simply by Eq. 1 and 2 and the exponential dependence on gate voltage is graphically shown in Fig. 3. In Fig. 3, the solid curve is a fit using the simple analytical model with λ_N and λ_P equal to 29.82 and 30.83, respectively, while the discrete data points are the result of BSIM SPICE simulation using the 70 nm Berkeley Predictive Technology Model (BPTM). Figure 4 has been used as a test schematic for capturing V_{GS}/V_{SG} dependence of sub-threshold leakage current for PMOS and NMOS transistor W/L = 70/70 nm (BPTM models http://www-device.eecs.berkeley.edu/~ptm).

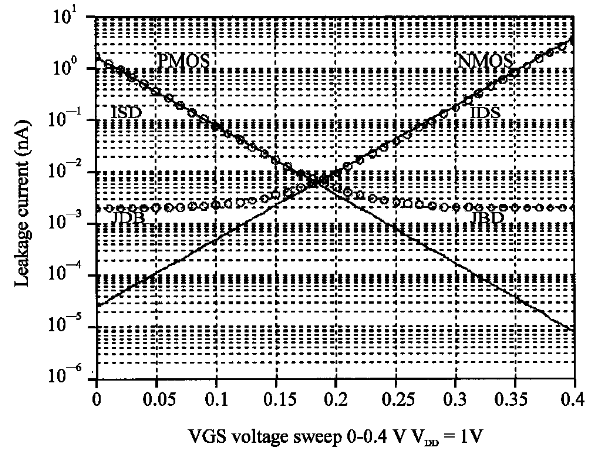

Fig. 3: Gate to source voltage dependency on leakage current

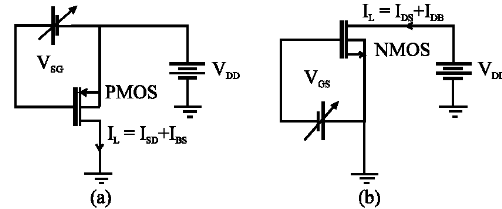

Fig. 4: Test schematic of gate to source voltage dependency on leakage current

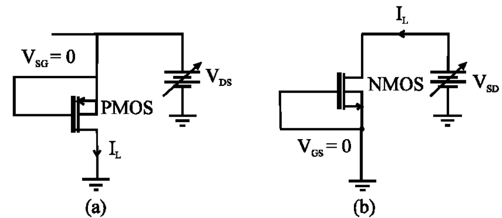

Fig. 5: Test schematic of drain to source voltage dependency on leakage current

$$I_{L-NMOS} = \left(\frac{W}{L}\right) Q_N e^{\lambda_N V_{GS}} \qquad V_{DD} = 1\,V \tag{1}$$

$$I_{L-PMOS} = \left(\frac{W}{L}\right) Q_P e^{\lambda_P V_{GS}} \qquad V_{DD} = 1\,V \tag{2}$$

Due to the DIBL effect, there is also an exponential dependence on V_{DS}/V_{SD}. Figure 5 has been used as a test schematic for capturing V_{DS}/V_{SD} dependence of sub-threshold leakage current for PMOS and NMOS transistor (unity width W/L = 70/70 nm). DIBL effect simply modeled by Eq. 3 and 4 and graphically illustrated in Fig. 6. In

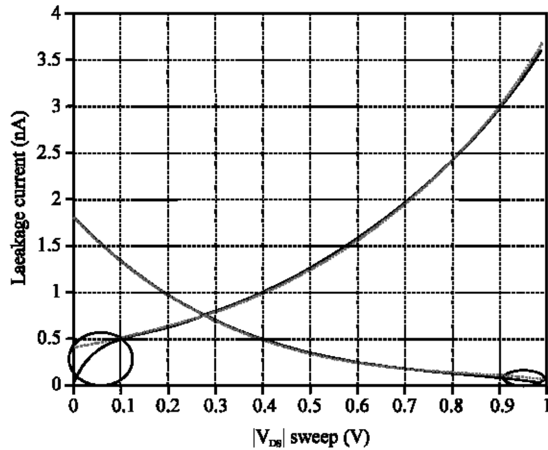

Fig. 6: Simulated and modeled leakage currents

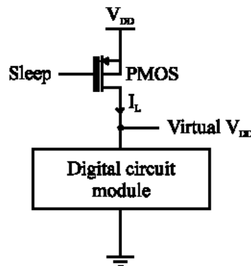

Fig. 7: Power supply gating using a PMOS transistor

Fig. 6, the solid curve is a fit using the simple analytical model with α_N and α_P equal to 2.21 and 3.23, respectively, while the dotted curve is a simulation result produced using BSIM SPICE with the 70 nm BPTM model.

$$I_{L\text{-}NMOS} = \left(\frac{W}{L}\right) K_N e^{\alpha_N V_{DS}} \qquad |V_{DS}| >> kT/q \tag{3}$$

$$I_{L\text{-}PMOS} = \left(\frac{W}{L}\right) K_P e^{\alpha_P V_{SD}} \qquad |V_{SD}| >> kT/q \tag{4}$$

Power supply gating using a PMOS sleep transistor: Here, we use a PMOS sleep transistor to investigate the effectiveness of power supply gating for Digital Module, it is shown on Fig. 7. We picked PMOS transistor as a sleep transistor, this is because the sleep transistor body needs to be biased for the body overdrive technique, which can be achieved standard CMOS process. On the Contrary NMOS sleep transistor requires twin-well process for the body overdrive (Anis *et al*., 2003).

In this case, however, we note that the effect of inserting the sleep transistor is to reduce the module supply voltage in the SLEEP state to a value virtual V_{DD} (V_{DD}') that is, in part, determined by the size of the sleep transistor. This reduced V_{DD}' leads to a module leakage that is less than that obtained without a sleep transistor.

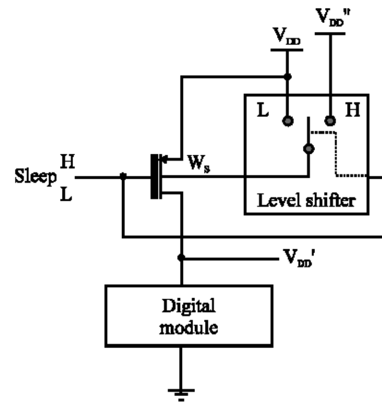

Fig. 8: Power supply gating using body overdrive

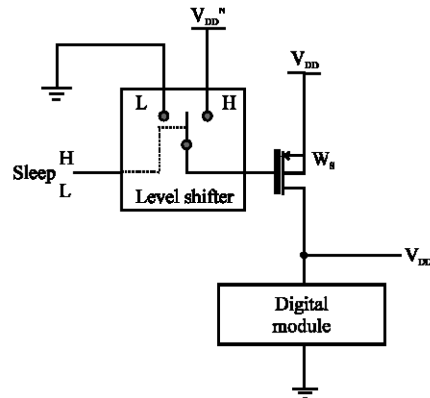

Fig. 9: Power supply gating with gate underdrive

Power supply gating using body overdrive: Power supply gating with body overdrive is a technique that dynamically changes the threshold voltage of the sleep transistor by modifying its body bias (Tschanz *et al*., 2003). When a reverse bias is applied to the body of a transistor, i.e., the body of a PMOS transistor is driven to a voltage V_{DD}'' that is greater than its source voltage V_{DD}, its threshold voltage is increased. As showed in Fig. 8, the body voltage of the PMOS sleep transistor should be set to V_{DD} during ACTIVE mode to achieve low threshold voltage and low on-resistance and set to V_{DD}'' during SLEEP mode to achieve high threshold voltage and low leakage.

Power supply gating using gate underdrive: As indicated in the Fig. 9, gate underdrive is implemented similar to body overdrive except that the level shifter is attached to the gate of the sleep transistor rather than its body. Gate underdrive reduces sub-threshold leakage current much more effectively than body overdrive, but there is the danger of damage to the gate oxide if excessive underdrive is used.

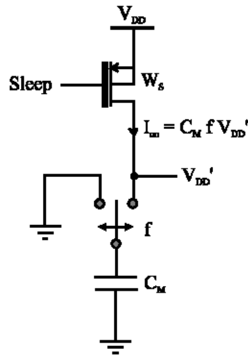

Fig. 10: Model for propagation delay and internal V_{DD}' in ACTIVE mode

Calculation of propagation delay in ACTIVE mode: When the circuit is ACTIVE, propagation delays in the module will be increased due to the non-zero on-resistance of the PMOS sleep transistor, as discussed with the aid of Fig. 10. During each low-to-high transition within the circuit module, a surge of current is drawn from the sleep transistor, creating a voltage drop and reducing the supplied V_{DD} to an internal level V_{DD}'. Since this circuit node will typically have a large capacitance, the current surges produced by many logic gates at different instants in time will be filtered to produce a dc voltage

$$V_{DD}' = V_{DD} - R_{ON} V_{DD}' C_M f \qquad (5)$$

where R_{ON} is the on-resistance of the sleep transistor, which is inversely proportional to sleep transistor width W_S and C_M is the total capacitance of switching nodes in the module and f is the average switching frequency.

The reduced supply voltage V_{DD}' determines the on-resistance of the transistors within the circuit module and propagation delay is proportional to on-resistance. Since $t_{PD} \propto R_{ON} \propto 1/(V_{DD} - |V_T|)$, where V_T is the threshold voltage of the MOS transistor, the relative propagation delay of the module with sleep transistor is

$$\frac{t_{PD}}{t_{PD}} = \frac{(V_{DD} - |V_T|)}{(V_{DD} - |V_T|)} \qquad (6)$$

In order to calculate V_{DD}', the on-resistance of the sleep transistor will be modeled using $R_{ON} = 1/[(W/L)_S \mu_p C_{ox} (V_{DD} - |V_T|)]$. Substitution into Eq. 2-5 yields:

$$V_{DD} = \frac{V_{DD}}{1 + \frac{C_M f}{\left(\frac{W}{L}\right)_S \mu_P C_{OX} (V_{DD} - |V_T|)}}, \qquad (7)$$

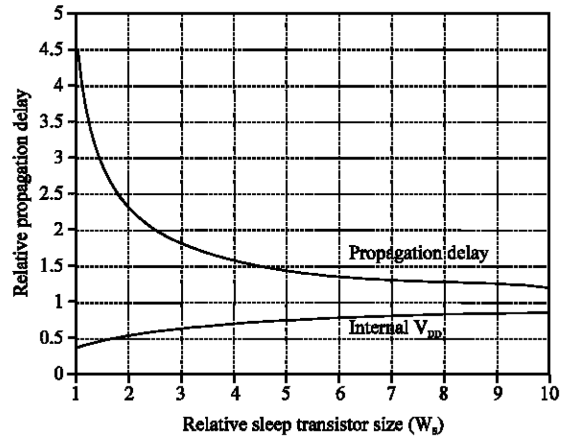

Fig. 11: Model for internal V_{DD} and propagation delay versus sleep transistor size

where $(W/L)_S$ is the sleep transistor size, μ_p C_{ox} are process parameters and V_T is the threshold voltage of the sleep transistor. Finally, Eq. 7 is substituted into Eq. 6 to determine the relative propagation delay.

$$\frac{t_{PD}}{t_{PD}} = \frac{(V_{DD} - |V_T|)}{\left[\frac{V_{DD}}{1 + \frac{C_M f}{\left(\frac{W}{L}\right)_S \mu_P C_{OX} (V_{DD} - |V_T|)}}\right] - |V_T|} \qquad (8)$$

The calculation of module capacitance C_M is less clear, but can be approximated by summing the gate oxide capacitance, including channel area as well as gate-drain and gate-source overlap, of every transistor in the module. Drain and source capacitance is ignored in this approximation, but this is reasonable since junction capacitance is typically a small fraction of gate capacitance and only a fraction of the source/drain junctions in a static CMOS logic circuit are switched when the output of a logic gate is switched. Thus, we will approximate

$$C_M = \Sigma (W_L C_{OX} + 2 W_L C_{OL}) \qquad (9)$$

where, W, L, C_{OX} and C_{OL}, are channel width, length, gate oxide capacitance and drain-source overlap capacitance respectively. The summation includes all transistors in the logic module.

A typical result of the V_{DD}' and propagation delay models is plotted in Fig. 11. In this plot, f, C_M, V_{DD}, $|V_T|$, μ_p (channel mobility) and C_{ox} are equal to 1 GHz, 100 fF, 1 V, 0.1 V, 35 cm^2/V sec and 21.6 fF μm^{-2}, respectively,

consistent with the 70 nm BPTM. The unit sleep transistor width is 0.07 μm. This plot demonstrates that relative propagation delay approaches one when sleep transistor size is adequately large. In this example, the internal V_{DD}' is 0.86 V_{DD} and the propagation delay penalty is 25% when the sleep transistor is 10 units wide.

VERIFICATION OF LEAKAGE AND PROPAGATION DELAY MODELS USING ISCAS85 BENCHMARK TEST CIRCUITS

The ISCAS85 Benchmark test circuits were used to study the behavior of leakage current in complex, static logic circuits and examine the accuracy of the estimation techniques for leakage current and propagation delay. Table 1 summarizes the contents of the circuits in this benchmark set. All of the gates are implemented using static CMOS logic circuits.

We estimate the sub-threshold leakage current for each ISCAS85 benchmark circuit, as a whole, by multiplying the average leakage current contribution from each gate by the number of gates and summing the results. In order to best compare estimated results with SPICE simulations, it is desirable to average across all possible input vector combinations. Such an approach is not practical for large circuits. Instead, we employ a more tractable alternative, choosing 100 input vectors at random and averaging the resulting calculated leakage currents. Such input vectors sets were created using a MATLAB uniformly distributed random number generator. The accuracy of this comparison between estimated results and SPICE simulation was determined by the size of the random input vector sets (Kucukkomurler, 2004).

Simulation of ISCAS85 leakage current using body overdrive and gate underdrive: The leakage current of ISCAS85 benchmark circuits using a PMOS sleep transistor with body overdrive and gate underdrive were simulated, analogous to the previous section and compared to the results with no sleep transistor and with a simple sleep transistor. The body overdrive and gate underdrive was 40%, i.e., 1.4 V for V_{DD} = 1 V for the 70 nm BPTM models. SPICE was used to simulate the leakage current with 100 randomly selected static input vectors applied to the ISCAS85 benchmark circuits. The values obtained by averaging the 100 resulting leakage currents for each configuration are presented in Table 2. Leakage current savings associated with each of the three sleep transistor configurations are promising. The fact that the relative reduction for each configuration is comparable can be attributed to the fact that sleep transistor width has been set to 10% of the total module gate width.

Table 1: ISCAS85 benchmark test circuits estimated and simulated leakage current

ISCAS85 circuits		Estimated and simulated leakage current			
Circuits name	No. of gates	Estimated μA (avg.)	Simulated μA (avg.)	Error (±)	Relation error (%)
c17	6	0.038	0.037	+0.001	27
c432	180	1.050	1.280	-0.230	-17
c499	517	3.070	3.450	-0.380	-11
c880	325	1.940	2.410	-0.470	-19
c1355	488	2.910	3.340	-0.430	-13
c1908	425	2.560	3.060	-0.500	-16
c3540	890	5.430	6.250	-0.820	-13
c6288	2338	14.010	17.850	-3.840	-21

Table 2: ISCAS85 simulated leakage currents with and without sleep transistor

		Leakage with sleep transistor		
ISCAS85 circuits units	w/o sleep transistor (μA)	w sleep (nA)	Body overdrive (nA)	Gate underdrive (pA)
c17	0.037	5.50	1.12	2.02
c432	1.280	165.12	34.94	2.73
c499	3.450	430.23	89.53	3.85
c880	2.410	320.45	67.15	3.43
c1355	3.340	444.32	94.45	3.96
c1908	3.060	395.23	81.05	3.68
c3540	6.250	905.78	188.02	5.93
c6288	17.850	2543.56	435.45	10.99

OPTIMIZATION OF THE SLEEP TRANSISTOR SIZE RESPECT TO PROP. DELAY, WIDTH AND LEAKAGE

Optimization of the sleep transistor depends on the cost function of the parameters: Leakage, width and delay. To better understand the trade off we begin by assigning equal cost for all three parameters and optimize the sleep transistor size accordingly.

$$\text{Cost} = \eta_{pd} t'_{pd} + \eta_l I'_l + \eta_w W'$$

where η_{pd}, η_l, η_w, are waiting cost factors and t_{pd}', I_l', W' are the relative propagation delay, leakage current and transistor width, respectively. Waiting cost factors are initially chosen to be equal ($\eta_{pd} = \eta_l = \eta_w = 1/3$). However those cost factors can assign to the different values according to importance of the parameter for a specific application. In addition to that optimizing sleep transistor size will perform for underdrive 0, 0.2 and 0.4 V. The optimization calculation have been made for all ISCAS85 test circuits but only some of the results have been plotted and reminder of the results have been tabulated.

Since $\Sigma\eta = 1$ and relative parameters have value 1 when compared to the ungated circuit, cost is 1 when the gated circuit has the same quality as the ungated circuit.

Table 3: Optimum sleep transistor width for ISCAS85 test circuits

ISCAS85 circuits transistor unit widths)	Optimum sleep transistor width (unit widths)		
	V_{GS} = 0 V (% W overhead)	V_{GS} = 0.2 V (% W overhead)	V_{GS} = 0.4 V (% W overhead)
17 ($12W_P$+$24W_N$)	$13.2W_P$ (6.66)	$2.15W_P$ (10.75)	$215W_P$ (10.75)
432 ($495W_P$+$601W_N$)	$48W_P$ (7.01)	$77W_P$ (11.07)	$78W_P$ (11.21)
499 ($1095W_P$+$1509W_N$)	$98W_P$ (6.14)	$158W_P$ (9.90)	$159W_P$ (9.96)
880 ($907W_P$+$1357W_N$)	$87W_P$ (6.41)	$139W_P$ (10.24)	$140W_P$ (10.31)
1355 ($1082W_P$+$1990W_N$)	$118W_P$ (6.76)	$192W_P$ (11.00)	$192W_P$ (11.00)
1908 ($1048W_P$+$1390W_N$)	$94W_P$ (6.22)	$150W_P$ (9.93)	$151W_P$ (10.00)
3540 ($2555W_P$+$3685W_N$)	$235W_P$ (6.21)	$377W_P$ (9.97)	$378W_P$ (9.99)
5288 ($4848W_P$+$10890W_N$)	$602W_P$ (7.10)	$963W_P$ (11.36)	$964W_P$ (11.37)

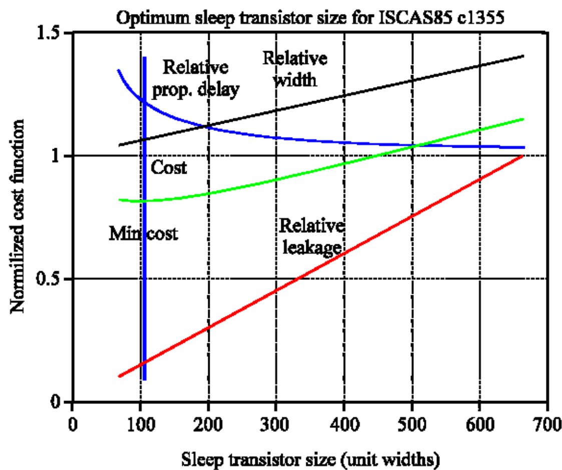

Fig. 12: Optimum sleep transistor width for underdrive 0 V

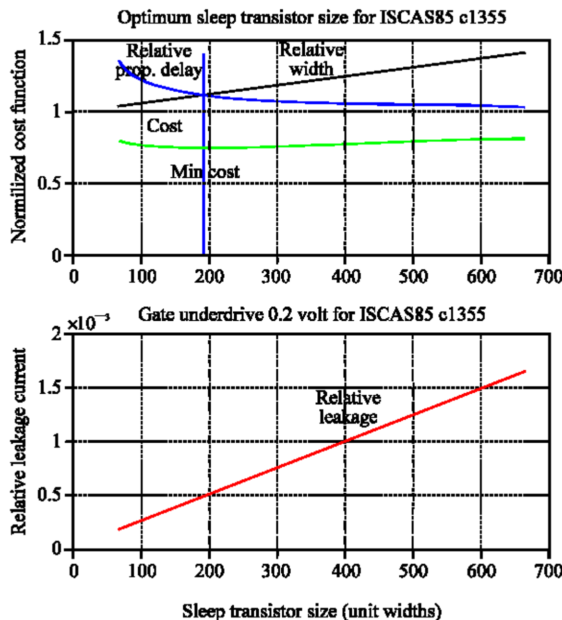

Fig. 13: Optimum sleep transistor width for underdrive 0.2 V

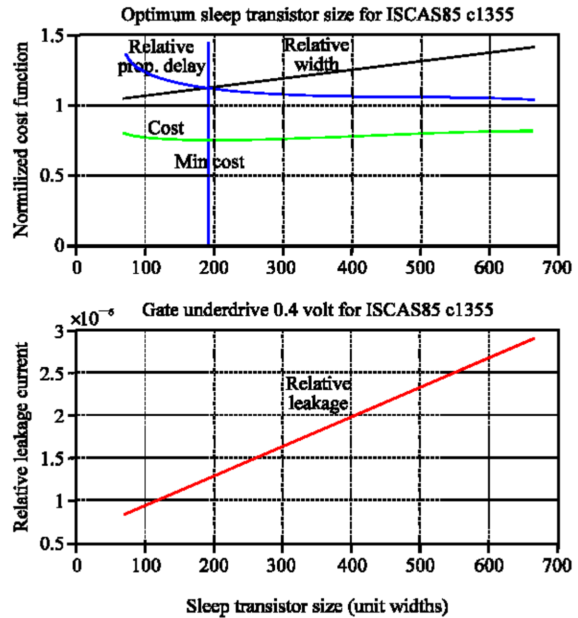

Fig. 14: Optimum sleep transistor width for underdrive 0.4 V

A cost less than 1 is an improvement in circuit quality. Leakage current, propagation delay, width overhead normalized relative to the without sleep transistor case and cost function has been plotted. Minimum cost has been determined according to waiting factor parameters. Optimum sleep transistor width for V_{GS} = 0 V is around 10% of the total circuit width. However the optimum sleep transistor is wider when V_{GS} underdrive increases to 0.2 and 0.4 V. Optimum sleep transistor size has been plotted for three cases for the c1355 circuits on Fig. 12-14, respectively. Optimum sleep transistor size for rest of the ISCAS85 test circuit has been tabulated for V_{GS} equal to 0, 0.2 and 0.4 V on Table 3.

CONCLUSIONS

Leakage current estimation has been successfully achieved and verified using ISCAS85 test circuits. Sleep transistor size optimization with respect to module propagation delay, leakage current and total transistor width have been achieved and verified using ISCAS85 test circuits. The estimate of propagation delay has been shown to be quite accurate. The estimate of the leakage current is about double simulation when gate underdrive is not used since the leakage of the sleep transistor is comparable to the module. With gate underdrive, the estimate of leakage current is quite accurate.

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