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Modeling and Simulation of DSP Controlled SV PWM Three Phase VSI

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Abstract: The present research is concerned with the development of two space vector pulse width modulated VSI models using the software package Matlab. The theoretical principles underlying the space vector modulation technique are presented but have been limited to the few relations needed for the model implementation. The first model, the formulation of which is based on the concept of switching function associated with the semiconductor power switches, is a switched mode inverter while the second model, the sine mode inverter, is formulated in terms of the duty times cycles of the pole switches is a nearly perfect sine wave space vector controlled generator. By comparison to the switched mode inverter, the sine mode inverter exhibits a larger bandwidth to frequency demand. The reliability of the sine mode model has been checked against the experimental results available in the literature provided by Analog Device Corporation.

Key words: SV PWM modelling, VSI inverter, switching function, DSP modulator

INTRODUCTION

Speed control of ac motor, which requires concomitant variation of the frequency and stator voltage to keep the air gap flux to its rated value, was mainly implemented by PWM controlled inverters. In the last two decades, a more flexible power dc to ac power conditioning technique, space vector PWM (Broeck *et al*., 1988), has became increasingly popular in high performance ac servo drives applications. Unlike conventional PWM control strategies, where the determination of the switching pattern of the inverter power switches is in essence an analog signal processing problem, SV PMW, in contrast, deals with the three phase inverter as a unique space vector using the Clark's Transformation. More importantly, because of the placement of the target voltage space vector, representing the desired inverter output voltage, is an anticipative process, this technique is easily implemented using dedicated microcontrollers and DSP processors (ADCorp/AN401, 2000; Texas Instrument/SPRA524, 1999). Because of the availability of dedicated timers for SV PWM pulse pattern generation, within most of present DSP and software routines for implementing reference frame transformations, field oriented control of ac drives can be directly formulated in terms of space vector theory (Vas, 1999; Leonhard, 1997). Performance assessment of sv pwm control strategies through theoretical investigation and modelling is another present field of interest (Pinheiro *et al*., 2003). Although several models have been reported in different publications, they are either formulated in terms of S-function, state variable model (Pinheiro *et al*., 2003) or given as SUMILINK black boxes. Besides the inevitable mathematic formulation of these models, they do neither give the physical understanding of the model nor provides the flexibility for parameter variation for performance analysis. This paper proposes a new space vector pwm Simulink modulator which emulates DSP implementation of a space vector modulator.

SPACE VECTOR CONTROL STRATEGY

In the 180° square wave VSI inverter, shown in Fig. 1, the three phase output voltages are synthesised according to a predetermined switching pattern of the semiconductor switches.

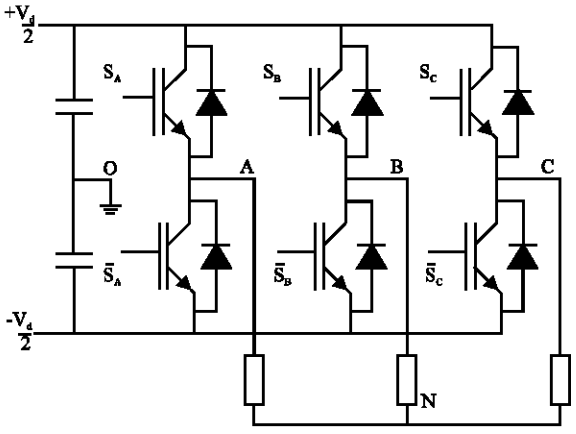

Fig. 1: Topology of the VSI

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Within one sixth of a period the output voltage is constant because the conduction times of any semiconductor switch is held constant over 180° electrical degrees. By shifting the gating signals from each other by 60°, the resulting output phase voltage is a six steps approximation of a sinusoidal wave. These discrete operating states of the inverter can be described by a space vector

$$\bar{v}_k = \begin{cases} \frac{2}{3} V_d e^{j(k-1)\frac{\pi}{3}} & \text{for } k = 1 \div 6 \\ 0 & \text{for } k = 7, 8 \end{cases} \quad (1)$$

which represents the stator phase voltages and two additional null vectors mapped into the origin of the stationary reference frame. In contrast, the space vector PWM control strategy consists of elaborating a switching pattern of the power semiconductor switches, within a sector, by varying the conduction time of the semiconductor switches in order to impose a discrete sinusoidal variation of the output phase voltage between two consecutive states of the six step inverter. By switching at high frequency the power switches according to a predetermined pattern the tip of the reference space vector, which represents the desired approximation of the output voltage, is forced to follow a smooth circular path. This objective is met by building the target reference space vector from the time weighted combination of two adjacent sampled vectors. In terms of volt-second, the averaging process within a sampling period is

$$\frac{1}{T}\int_0^T \vec{V} * dt = \frac{1}{T}\int_0^{t_1} \vec{V}_1 dt + \frac{1}{T}\int_0^{t_2} \vec{V}_2 dt \quad (2a)$$

Hence

$$\vec{V}* = \frac{t_1}{T}\vec{V}_1 + \frac{t_2}{T}V_2 \quad (2b)$$

where t_1 and t_2, for instance, are the time to be spent in the active states 100 and 110.

According to Fig. 2, which shows the reference vector $\vec{V}^*$ for a particular angular position θ, into the stationary stator reference frame $\alpha\beta$

$$V * e^{i\theta} = \frac{t_1}{T}\frac{2}{3}V_d e^{i0} + \frac{t_2}{T}\frac{2}{3}V_d e^{i\frac{\pi}{3}} \quad (3)$$

The active state durations are finally found from the previous relation as

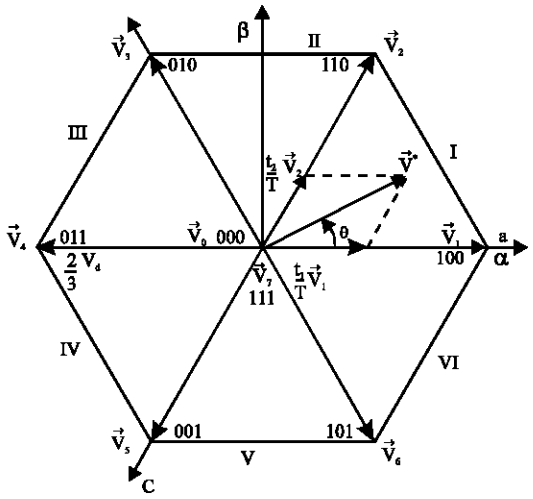

Fig. 2: Inverter operating states

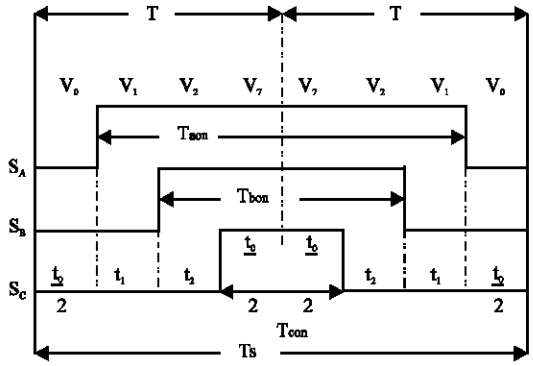

Fig. 3: Switched sequence required to syntheses the target space vector in the first sector

$$\frac{t_1}{T} = m\frac{\sin(60^\circ - \theta)}{\sin 60^\circ}, \quad \frac{t_2}{T} = m\frac{\sin\theta}{\sin 60^\circ} \quad (4)$$

where $m = \frac{3}{2}\frac{V^*}{V_d}$ is the modulation index.

Although infinite vector samples can be obtained within a sector, their components are always linearly dependent on the base vectors delimiting a given sector. For that reason, only two adjacent switching states say (100 and 110) are required to synthesise the current reference vector. Figure 3 shows the switching pattern required to synthesise the target vector in sector one.

To reduce the switching frequency of the inverter, the next position of the space vector is obtained by changing the conducting state of only a single power switch. A transition is made by including a null state between every two target vectors. The duration of the null vector is the remaining time from the switching period.

$$t_0 = t_7 = T-(t_1+t_2) \quad (5)$$

Therefore a switching sequence includes always a starting null vector, the required switching pattern, finally ending by a null vector; the reverse sequence is then applied for the next sampling period. If the time application of the null vector is divided equally Texas Instrument/SPRA524, 1999), a symmetrical space vector modulation is obtained.

The maximum output phase voltage is obtained when the reference space vector lies in the middle of the first sextant. In that case

$$\vec{V}^*_{max} = \frac{1}{2}\vec{V}_1 + \frac{1}{2}\vec{V}_2 = \frac{t_1}{T}\vec{V}_1 + \frac{t_2}{T}\vec{V}_2 \quad (6)$$

therefore $t_0 = 0$, no time is then available for a null vector insertion to enable smooth transition between two consecutive target vectors. Over-modulation, is reached for

$$V^* > V^*_{max} = V_m \cos\frac{\pi}{6} = \frac{\sqrt{3}}{3}V \quad (7)$$

i.e., for m>0.866, is used in some applications to boost of the inverter output voltage. Although two different over-modulation modes are available, only mode I, suitable for Simulink implementation, has been used, the active switching durations of which are calculated according to

$$\frac{t_1}{T} = \frac{\sqrt{3}\cos\theta - \sin\theta}{\sqrt{3}\cos\theta + \sin\theta},\ t_2 = T - t_1\ t_0 = 0 \quad (8)$$

Simulink model of the SV PWM VSI: By comparison to the space vector modulator proposed by Math Works (2004). which is made up from seven blocks, the present models include only four blocks connected in cascade.

SWITCHED MODE INVERTER

Active state computation block: In ac drives, the control effort signal of the inner current loop represents the reference voltage, whereas in an open loop configuration this signal

$$v^* = v_\alpha + jv_\beta,\ v^* = V^* e^{i\theta} \quad (9)$$

is derived from the Clark's transformation of the desired three phase output voltage. The simulation of the on time duration is carried out, according to relations 4 and 8, by sampling, at fixed frequency the reference space vector.

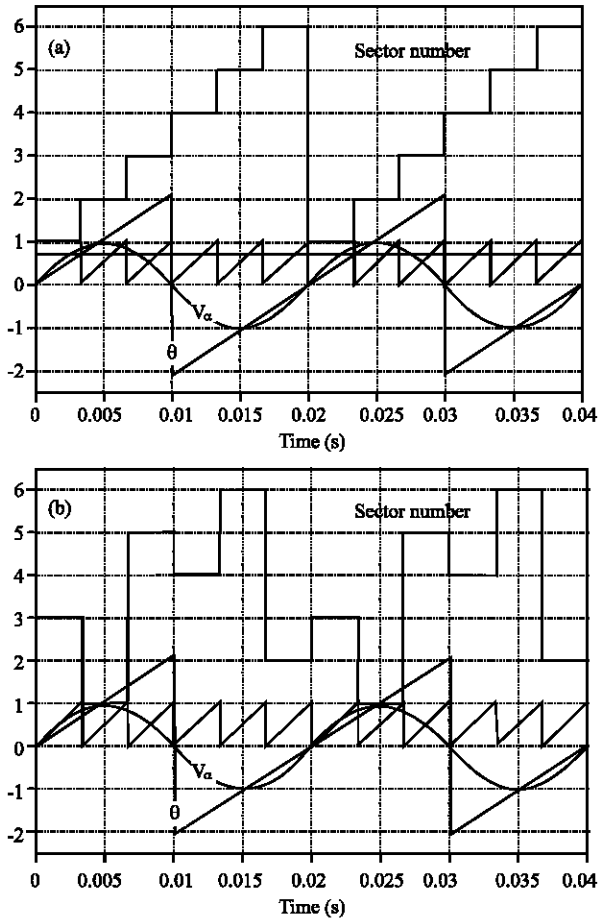

Fig. 4: Sector number determination

Since the time duration values remain the same within an interval of 60°, a modulus block is used to divide, a time period of V^*, into six intervals.

Figure 4 shows some features of this block. Depending on the sign of t_0, the linear or over modulation mode is selected; through a selector bloc, the resulting output is fed to the next block, the task of which is to compute the duty time cycle of each inverter leg.

Duty cycle computation block: Its purpose is to assign the on duty time duty cycles T_{aon} T_{bon} and T_{con}, to the right inverter leg; such a task requires the knowledge of the sector number in which the reference vector is currently lying. Two techniques have been used to simulate the sector number as a sub block. The first, used with DSP (Texas Instrument/SPRA524, 1999), is not suitable for Simulink programming as it can be seen from Fig. 4b. The second relies on the sampled magnitude and position of the reference vector, carried out in the previous block, to retrieve the sector number stored in a two dimensional look up table. In the first sector the on duty time cycles

T_{aon} T_{bon} and T_{con}, shown in Fig. 3, are related to the inverter the active state duration and through the matrix formulation.

$$\begin{bmatrix} T_{aon} \\ T_{bon} \\ T_{con} \end{bmatrix} = 2\begin{bmatrix} 1 & 1 & 1 \\ 0 & 1 & 1 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} t_1 \\ t_2 \\ \frac{t_0}{2} \end{bmatrix} \quad (10)$$

The element of the matrix can be found from the required gating signal (Texas Instrument/SPRA524, 1999), applied to the upper power switches of the six steps inverter. To each sector corresponds a well defined matrix (Texas Instrument/SPRA524, 1999). In the simulation, the on time duty cycle are normalised with respect to the sampling period of the reference space vector.

Switched mode inverter block: The final block consists of the control and the six steps inverter blocks. By comparing the on time duty signals generated by the previous block with a 10 KHz frequency triangular carrier wave, the gating pulses of the inverter power switches are produced using a relay block and then fed to the inverter block. The power inverter has been implemented in terms of the switching function g_i associated with each power switch. The switching function g_i of a given power switching can assume either 1 or 0 according to its conducting state. Since, two power switches of the same leg can not be on simultaneously, the switching function of the phase α, for instance, is defined as

$$g_a + g_{\bar{a}} = 1 \quad (11)$$

The output phase voltages, in terms of the switching functions, are

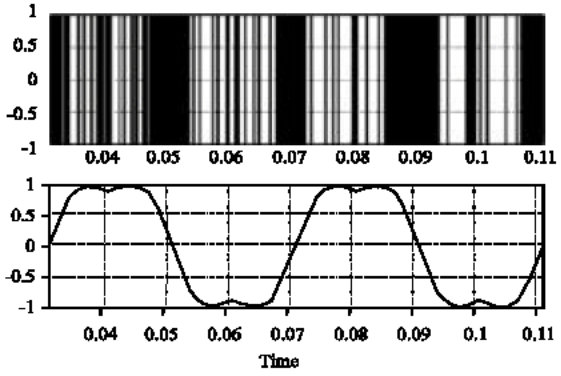

Fig. 5: Normalized pole voltage at f = 25 Hz

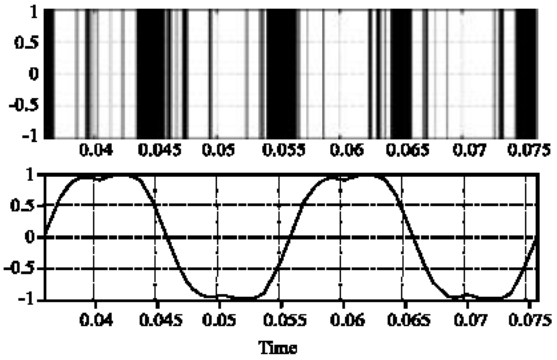

Fig. 6: Normalized pole voltage at f = 50 Hz

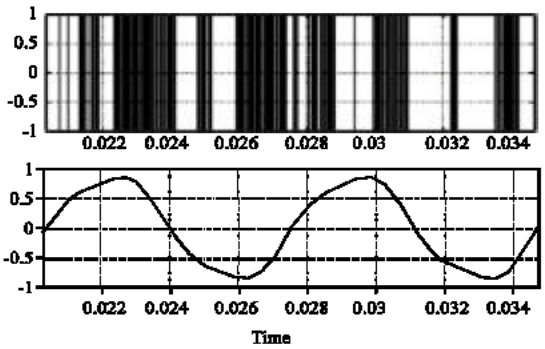

Fig. 7: Normalized pole voltage at f = 140 Hz

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{V_d}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} g_a \\ g_b \\ g_c \end{bmatrix} \quad (12)$$

Hence the output stage of the switched mode inverter in modelled merely by a standard matrix multiplication bloc.

Simulation of the switched mode inverter: Figure 5 to 7 show the inverter pole voltage for the operating frequencies of 25, 50 and 140 Hz at or the maximum value of the modulation index m = 0.866 which corresponds to the upper limit of the linear mode of the space vector modulation technique.

As it can be expected from relation 12, the output voltage at the inverter pole is made up from a voltage pulses which result from the switching action of the semiconductor switches as shown in the top curves of each figure. The continuous curves represent the corresponding pole voltage after filtering the chopped voltage using a low pass filter. It can be seen that for the frequency of 25 Hz, this signal is the typical signature of space vector modulation. Figure 6 shows that the switched mode inverter still behaves satisfactory in accordance with the space modulation technique up to 50 Hz.

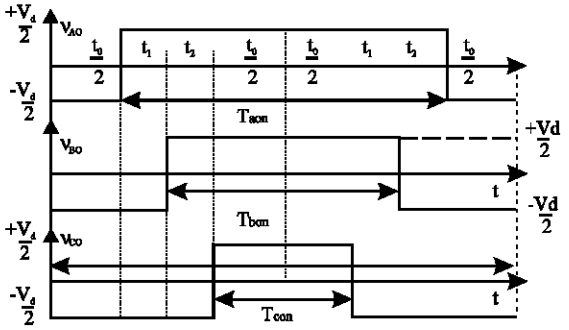

Fig. 8: Pole voltage waveforms in the first sector

In contrast, at frequency of 140 Hz, the switched mode inverter model is no longer able to reproduce this typical waveform owing to the high harmonic generation due to the high frequency commutation of the inverter power switches. To overcome this obvious limitation as far as the frequency response of the inverter is concerned another inverter model has been developed.

CONTINUOUS MODE INVERTER

The formulation of the sine mode or continuous SV PWM inverter is derived from the computation of the average pole voltage of each phase.

From Fig. 8, the average pole voltage of phase in sector one can be found as

$$v_{AO}(\theta) = v_{AN} + v_{NO} = \frac{V_d}{2}\frac{1}{T_s}(2t_1 + 2t_2) = d_{aon}V_d - \frac{V_d}{2} \quad (13)$$

where $d_{aon} = \frac{T_{aon}}{T_s}$ is the on time duty cycle of the semiconductor switch S_A of the inverter.

Similar relations can be derived for the remaining phases.

$$\begin{aligned} v_{BO}(\theta) &= v_{BN} + v_{NO} = d_{bon}V_d - \frac{V_d}{2} \\ v_{CO}(\theta) &= v_{CN} + v_{NO} = d_{con}V_d - \frac{V_d}{2} \end{aligned} \quad (14)$$

The offset voltage v_{NO} is found from the previous relations bearing in that the load voltage should form a balanced three system voltage

$$v_{NO}(q) = \frac{1}{3}V_d(d_{aon} + d_{bon} + d_{con}) - \frac{V_d}{2} \quad (15)$$

Finally, the phase voltages are

$$\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \frac{V_d}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} d_{aon} \\ d_{bon} \\ d_{con} \end{bmatrix} \quad (16)$$

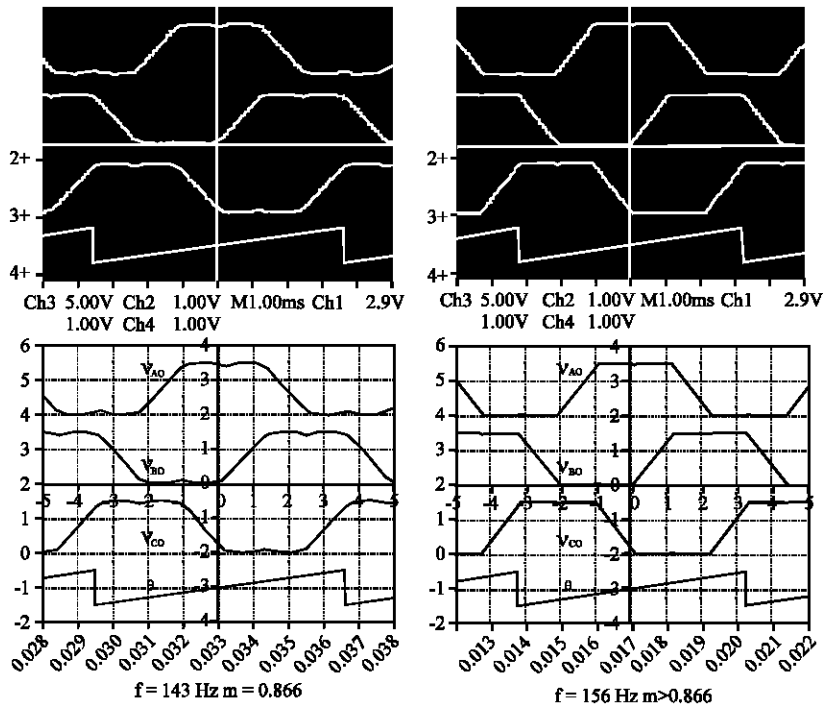

Fig. 9: Comparison between actual and simulated pole voltage waveforms

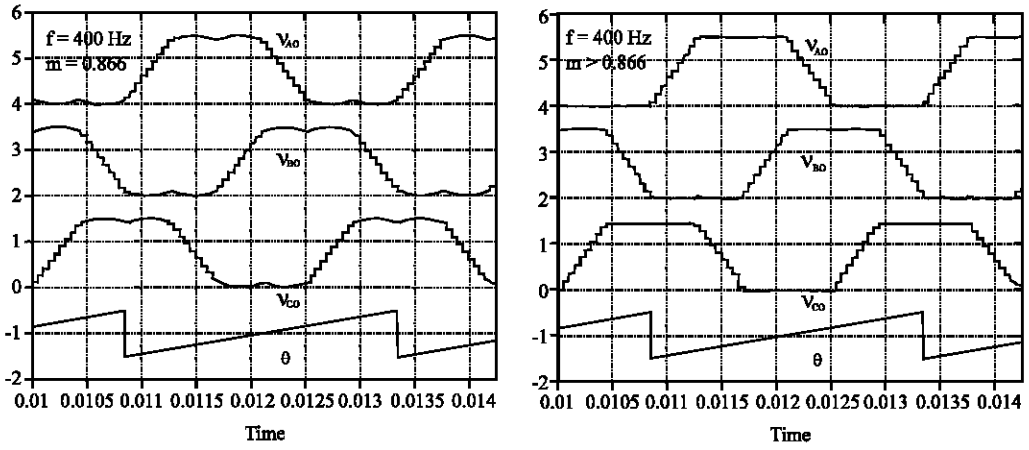

Fig. 10: Simulated pole voltage waveforms at f = 400 Hz for linear and over modulation mode

Examination of relation 12 and 16 shows that the mathematical formulation of both inverter models is the same except for that the first is expressed in terms of a switching function while the second is expressed in terms of the pole duty cycle. Both models share the same computational blocks, they differ only from the inverter model formulation.

The switched mode inverter will reproduce at its output the pulse train of the switching function whereas the sine mode inverter is expected to produce continuous voltage waveform since the on time duty cycle d_{aon}, d_{bon}et d_{con} are a piecewise continuous function of times.

Simulation of the sine mode inverter: The validity of the sine mode inverter model has been checked by comparing the results of the simulation with the experimental data available in reference (Analog Device Corp/AN401, 2000).

Simulations of the sine mode inverter have been carried out for the linear and over modulation mode as shown in Fig. 9. Figure 10, which corresponds at a frequency of f = 400 Hz, has been included to show the stiffness response of the model to frequency demand. This comparison gives a full measure of the reliability of the sine mode model which emulates faithfully the DSP space vector implementation with the ADMC401 (Analog Device Corp/AN401, 2000).

CONCLUSIONS

Two space vector pwm modulated inverter models have been presented; their respective performances have been assessed by comparing their frequency response. The reliability of the sine mode inverter model has been confirmed through comparison with the experimental results kindly provided by the Mixed Signal DSP Group of Analog Devices Corporation.

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