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Design of a Low-Voltage High-Speed Switched-Capacitor Filters Using Improved Auto Zeroed Integrator

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Abstract: The low-voltage high-speed auto zeroed integrator characteristics is improved by applying current steering mechanism in the opamp structure of the integrators and utilizing the non-linear properties of switches. The proposed design results in considerable reduction of power dissipation. Based on this improvement a band-pass filter with centre frequency of 1 MHz and clock frequency of 6 MHz is designed. Furthermore a new circuit for implementation of an auto-zero low-pass filter is presented. Based on this configuration a fourth order low-pass switched capacitor filter with cut off frequency of 600 KHz and clock frequency of 6 MHz is presented. The proposed circuits are simulated using HSPICE and 0.25 μm CMOS technology at 1.5 V supply voltage.

Key words: Auto zeroed integrator, high-speed circuit, low-voltage circuit, analog integrated circuit, switched capacitor filter

INTRODUCTION

The main difficulty of low-voltage switched-capacitor (SC) circuit design is the driving voltage of the input CMOS switches. Two conventional approaches for low-voltage SC design using standard CMOS technologies are currently implemented. The first one is the bootstrapping method (Dessouky and Kaiser, 2001) in order to generate higher clock voltages to drive the gate voltage of the input switches, although the existence of on-chip high voltages is a danger for deep-submicrometer CMOS processes (Guan *et al*., 2001). The second one is the switched-opamp method (Sauerbrey *et al*., 2002; Cheung *et al*., 2002). The opamp in the integrator is turned on and off to transfer voltage signals to the next integrator stage, so no input switch is required to sample the input voltage. Switched opamp method is a real low-voltage SC circuit, but it is not suitable for high-speed SC circuit applications due to turning on/off time of the opamp. Another example of non switched mode approach is the GM-C filters which are designed and presented in low voltage applications (Garcia-Ortega *et al*., 2007). Recently the auto-zeroed integrator (AZI) and its application for low-voltage SC circuits was reported by Wang and Embabi (2003), where the basic AZI circuit (Bidari *et al*., 1999) was modified for the design of low-voltage and high-speed SC without bootstrapped clock voltage. Based on the previous study reported by Wang and Embabi (2003), here a two mode clock controlled opamp is utilized in order to reduce the power consumption and settling time of the auto-zeroed integrator circuit. First the basic modified AZI block and the new opamp structure are explained. Then a band-pass filter with centre frequency of 1 MHz and clock frequency of 6 MHz based on the above idea is designed, explained and compared to the previous study. Finally a new structure for implementation of the low-pass filter using AZI is presented. The capacitor coupling input in the conventional AZI circuits does not allow designing of low-pass filters. This short coming is solved by designing an additional input stage. Based on this design a fourth order Chebyshev filter with pass frequency of 600 kHz and clock frequency of 6 MHz is designed and simulated.

IMPROVED AZI CIRCUIT

The high speed low-voltage SC filter can be realized by cascading of AZI blocks. Figure 1 shows the basic differential AZI block. The complete description of the circuit is explained by Wang and Embabi (2003) and Rashtian and Hashemipour (2006). Equation 1 shows the mathematical sequence in time domain and Eq. 2 shows the Z-domain transfer function of this circuit if the input of the AZI circuit comes from the output of another AZI block.

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$$V_o(n-\frac{1}{2})T = \frac{C_1}{C_{i2}}V_i(n-1)T + V_o(n-\frac{3}{2})T \quad (1)$$

$$\frac{V_o}{V_i}(z) = \frac{C_1}{C_{i2}}\frac{z^{-1/2}}{1-z^{-1}} \quad (2)$$

It is important to notice that all switches in this circuit are nMOS transistors whose sources are connected to the common-mode voltage V_{CM} and the gates are stimulated at the supply voltage V_{DD}, which is expressed as $V_{GS}(on) = V_{DD}-V_{CM}$. This means that V_{GS} is not signal dependent, so charge injections and clock feed-through are cancelled in fully differential structure. If we assume that $V_{CM} = 0.5V$ to keep a reasonable output swing range to satisfy the requirement of $V_{GS}>V_{TH}$ to turn on a switch ($V_{TH} \approx 0.6V$), the supply voltage should be $V_{DD} > V_{TH} + V_{CM} > 1V$. This explains why AZI can work at 1.5 V in 0.25 μm CMOS technology.

In phase (φ_1) in Fig. 1, the output and input of the op-amp are connected together by the action of switches (M6 and M8) and the final value of the output voltage is a dc voltage (V_{CM}). Doing so, the linear action of the opamp is not critically essential and setting of the output voltage at V_{CM} can be done by external switches. In this approach the output stage of the opamp is operated in two current mode levels by the current steering action of the transistors M_{5B}-M_{8B} as shown in Fig. 2.

The W/L ratio of the current steering transistors is ten times greater than M_5-M_8. The current steering mode is controlled by transistors M_{5C}-M_{8C}. In the integration phase (φ_2), the output stage current is normal but in the other phase (φ_1) it is under low current condition. This can be called as pseudo switched opamp configuration with an improved characteristic of power consumption without speed reduction characteristics of switched opamps. In the phase (φ_1) the output voltage is set to V_{CM} by the non-linear action of nMOS switches M_{17} and M_{18}. Unlike the switched opamp technique, the nonlinear action of these switched transistors and the linear action

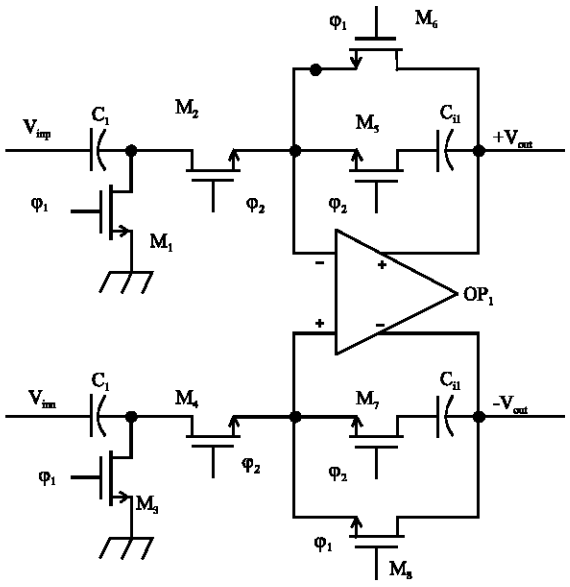

Fig. 1: Basic auto zeroed integrator circuit

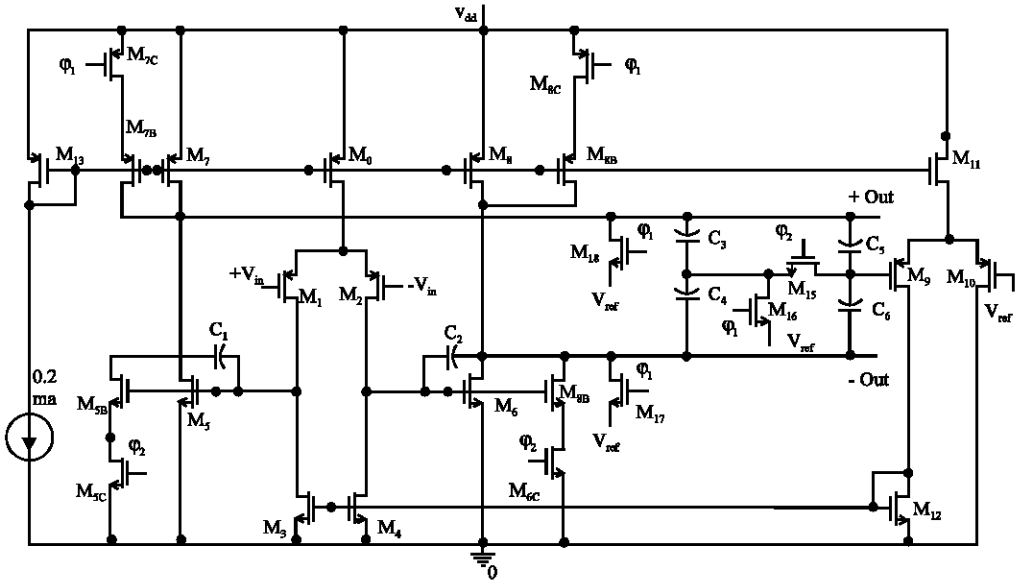

Fig. 2: Modified op-amp

of opamp without current steering transistors i.e., (M_{5B}-M_{8B}) will result in the same final steady state value with reduced power consumption. It means that the nMOS switches M_{17} and M_{18} are only used to reduce the settling time. The fast action of common mode feedback is critically important in high speed switched capacitor circuits (Hernandez-Garduno and Silva-Martinez, 2006) (Choksi and Carley, 2003). In this study, a unique dynamic common-mode detection circuit (C_3~C_6) working at 1.5 V without any signal-dependent switch is utilized. The detected common-mode voltage is compared to V_{CM} through M_9 and M_{10}. The result is fed back to the input stage of the opamp through a current mirror. Both C_3 and C_4 are discharged in φ_1 (the integrating phase) because the outputs are auto-zeroed by M_{17} and M_{18}. In φ_2, output voltages are sampled by C_3 and C_4 and integrated with C_5 and C_6. These four capacitors and the switches perform as an RC voltage divider.

BAND-PASS FILTER DESIGN

Figure 3 shows the schematic circuit of the band-pass filter (Wang and Embabi, 2003) with capacitor values of (C_1 = 0.5, C_2 = 2.31, C_{i1} = 1.95, C_{i2} = 2.15, C_c = 0.3, Cf = 1.92) pF. The clock frequency is set to 6 MHz with centre frequency of 1MHz and Q = 8.

Assuming the output of the first and second stage to named V_1 and V_2, respectively then:

$$V_1(n-1)T = -\frac{C_1}{C_{i1}}V_1(n-1)T - \frac{C_f}{C_{i1}}V_2(n-\frac{2}{3})T + V_1(n-2)T + \frac{C_1}{C_{i1}}V_1(n-\frac{2}{3})T \quad (3)$$

$$V_2(n-\frac{1}{2})T = \frac{C_2}{C_c+C_{i2}}V_1(n-1)T + \frac{C_{i2}}{C_c+C_{i2}}V_2(n-\frac{2}{3})T \quad (4)$$

From Eq. 3 and 4 the z-domain transfer function is given by 5:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{0.241\,(z^{-1} - z^{\frac{-1}{2}})}{1 - 0.0949\ z^{-1} + 0.877\ z^{-2}} \quad (5)$$

Output of the improved circuit and the previous study (Wang and Embabi, 2003) are compared in Fig. 4 at an input frequency of 1 MHz and $V_{p\text{-}p}$ = 1.2 V. For assessment of fall time improvement in proposed method a small part of Fig. 4 is magnified in Fig. 5.

As shown in Fig. 5, the fall time is improved by the non-linear action of switches (M_{17} and M_{18}) in the proposed opamp. Simulated results show a remarkable reduction (~32%) in the power consumption of this circuit compared to previous study. Figure 6 is acquired by using of more than 100 transient simulation results.

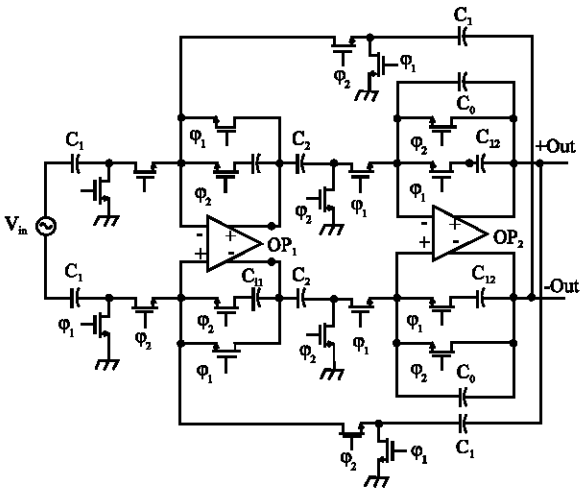

Fig. 3: Band-pass SC filter

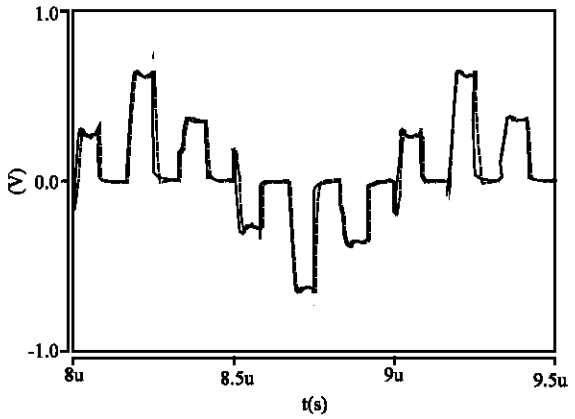

Fig. 4: Simulated output of differential band-pass filter at 6 MHz clock frequency

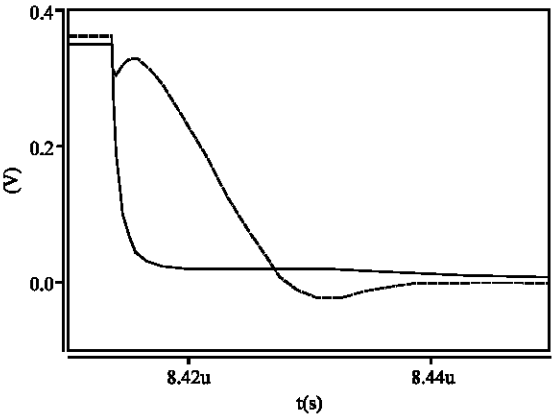

Fig. 5: Zoomed area of Fig. 4

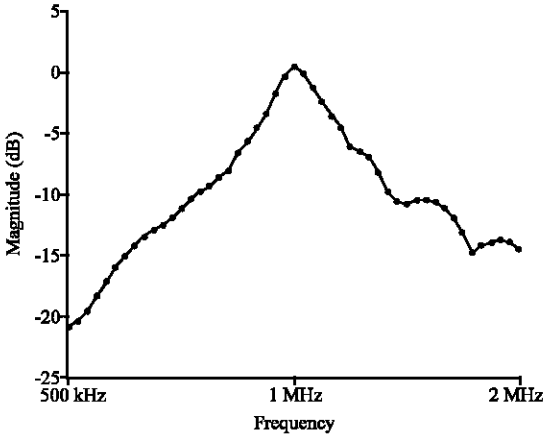

Fig. 6: Band-pass filter frequency response

LOW-PASS FILTER DESIGN

The input coupling capacitor, which is used in the input of conventional AZI circuits, prevents applying the AZI circuit to be realized as a low-pass filter. This problem is eliminated by the addition of an input circuitry (OP_0 and related components) as shown in Fig. 7 where this technique is used in a 2nd order low-pass filter. In φ_1 the output of OP_0 is set to Vcm and in φ_2 OP_0 is acting as a buffer with gain of (-1). It is obvious that the correct action of this stage depends on the relative accuracy of resistances and absolute accuracy is not crucially important.

Based on the above idea, Eq. 6 and 7 are obtained in the output of OP_1 and OP_2, respectively.

$$V_1(n-1)T = -\frac{C_f}{C_{i1}}[-(V_2(n-\frac{3}{2})T)] + V_1(n-2)T - \frac{C_1}{C_{i1}}(-V_1(n-\frac{2}{3})T) \quad (6)$$

$$V_2(n-\frac{1}{2})T = -\frac{C_2}{C_c + C_{i2}}V_1(n-1)T + \frac{C_{i2}}{C_c + C_{i2}}V_2(n-\frac{2}{3})T \quad (7)$$

Using the circuit shown in Fig. 7 and cascading them with the capacitor values of (C_1 = 0.89, C_2 = 0.61, C_{i1} = 2, C_{i2} = 2, C_c = 1.06 and C_f = 0.89) pF for the first stage and (C_1 = 0.69, C_2 = 1, C_{i1} = 1, C_{i2} = 2, C_c = 0.38 and C_f = 0.69) pF for the second stage, a low-pass fourth order Chebyshev filter is realized.

The circuit for the 4th order filter is further simplified by the fact that the designed input stage is no longer necessary for the input of the second cascaded biquad stage. This is due to the fact that the output of the first biquad stage is set to V_{CM} in φ_2 inherently. Using the above capacitor values and Eq. 6 and 7 the transfer function in z domain is obtained in 8.

$$H(z) = \frac{0.089\,z^{-1}}{1-1.566\,z^{-1}+0.65\,z^{-2}} \times \frac{0.0345\,z^{-1}}{1-1.494z^{-1}+0.839\,z^{-2}} \quad (8)$$

Figure 8 shows the differential output of the designed low-pass filter with input voltage of 1.2 V p-p and cut off

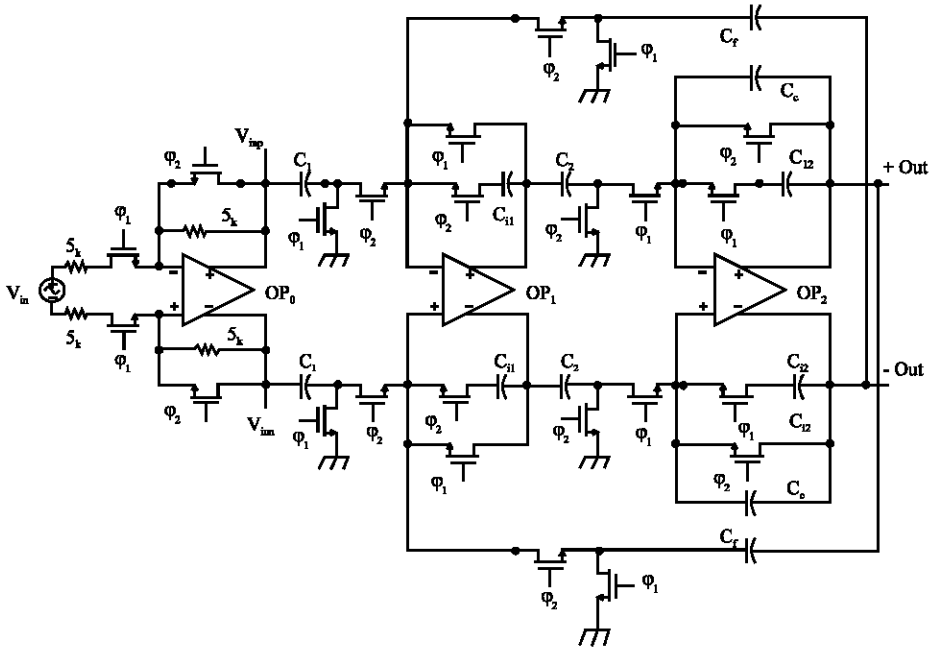

Fig. 7: Second order low-pass circuit

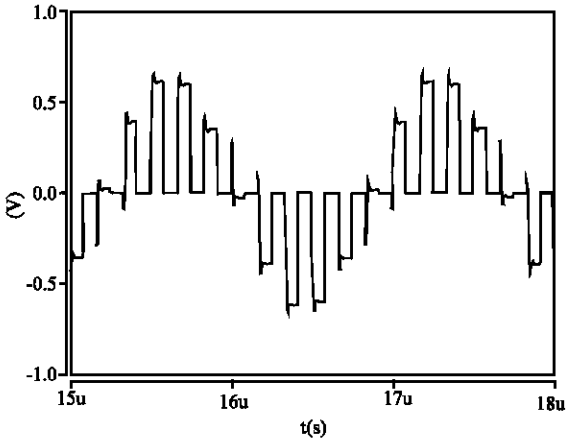

Fig. 8: Differential output of the Low-pass filter with 1.2 v_{p-p} input at 600 kHz

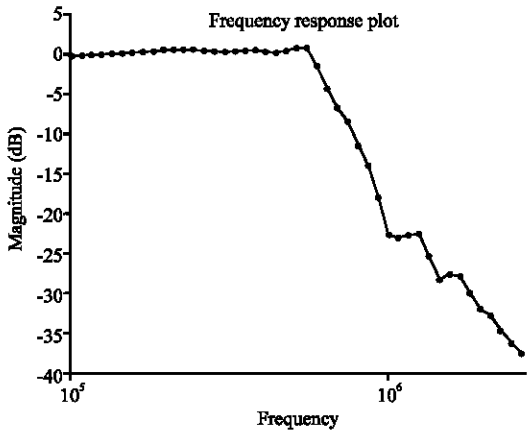

Fig. 9: Low-pass filter frequency response

frequency of 600 kHz at the clock frequency of 6 MHz. Frequency response of the designed filter is shown in Fig. 9. This plot is drawn using more than 100 HSPICE real time simulation.

CONCLUSION

The auto zeroed integrator performance is improved by a current steering method and the application of non-linear characteristics of the switched transistors. Based on this method, a band-pass filter with centre frequency of 1 MHz and clock frequency of 6 MHz with quality factor of 8 is designed and simulated. A ~32% reduction in power consumption and a reduction in fall time are also observed. The short come of the AZI circuit in the realization of switched capacitor low-pass filter has been overcome by addition of an input circuitry. Based on this improvement, a low-pass 4th order filter with cut off frequency of 600 kHz and sampling frequency of 6 MHz with differential output swing of 1.4 volt with 1.5 volt supply is designed and simulated using 0.25 μm technology.

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