Journal of Applied Sciences

ISSN 1812-5654

science alert

ANSInet
an open access publisher
http://ansinet.com

Journal of Applied Sciences 8 (11): 2008-2020, 2008
ISSN 1812-5654

Behavioral Modeling and Simulation Techniques for Substrate Coupling Analysis in Phase Locked Loop

[1,2]G.R. Karimi, [2]S. Mirzakuchaki and [2]A. Abrishamifar
[1]Department of Electrical Engineering, Faculty of Engineering,
Razi University, Kermanshah 67149, Iran
[2]Department of Electrical Engineering, IUST, Tehran 1686-13114, Iran

Abstract: Phase-Locked Loop (PLL) is widely used in Radio-Frequency (RF) and mixed-signal integrated circuits. This circuit experiences substrate coupling due to the simultaneous circuit switching and power supply noise which translate to phase noise and timing jitter. Substrate coupling noise is a key problem in today's large mixed-signal systems. This noise is caused by the coupling of digital part and can perturb analog circuits through common substrate. The estimating and accurate modeling of noise coupling effects is a major challenge for designers. Using behavioral models to perform system simulation at behavioral level is currently a popular solution to verify mixed-signal systems. A behavioral modeling approach allowing a systematic design of PLL with substrate coupling consideration is discussed here. This approach allows the designer to maintain a grasp of the fundamentals using coarse models at the early stage of the design and to eventually gain insight on the lower order effects by gradually increasing the level of detail as the design develops. Behavioral models of the PLL relating to noise analysis as well as intrinsic functionality are abstract from transistor level circuit analysis results. In this paper, we propose two methodologies to model phase noise or jitter (a key specification for phase-locked loops) using a piecewise linear (PWL) behavioral modeling and also by VHDL-AMS. A comparison between the results obtained by our models and those obtained by HSPICE simulation proves the validity of accuracy of the predicted models.

Key words: Jitter, phase-locked loop (PLL), phase noise, power/ground bounce, substrate noise, voltage-controlled oscillator (VCO)

INTRODUCTION

The continued scaling of CMOS technology, along with the progress in the design of high frequency analog and mixed-signal CMOS circuits, has enabled the integration of many of the functions needed to implement a broadband communication system on a single CMOS chip. A significant challenge in system-on-a-chip integration is the need to implement broadband analog circuits on the same die as the large complex digital circuits. Fast switching logic components inject current into the substrate causing voltage fluctuations which can affect the operation of sensitive analog circuitry due to body effect change in transistors' threshold voltages (Su *et al*., 1993). Figure 1 shows this problem.

With this high integration complexity and with increasing circuit speeds, the detrimental effect of substrate coupling becomes more and more severe in design considerations. Also, knowledge of substrate noise can help the designers to optimize the layout of their circuits. The substrate coupling effects in integrated circuits can be verified by computing the substrate parasitic impedances between all circuits' parts that inject noise into the substrate or/and are sensitive to it. The information about substrate coupling can be useful to circuit designers because it helps them to quickly identify and then remedy the dominant sources of coupling and also to avoid expensive redesigns and multiple fabrications runs (Miguel and Vargas, 2000). Thus, it is becoming more and more apparent that substrate noise is

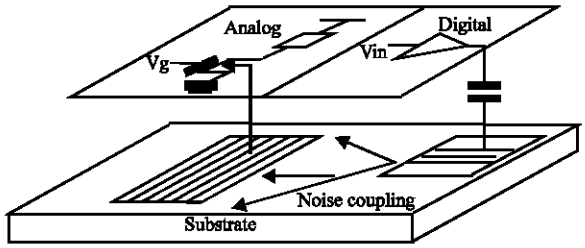

Fig. 1: The substrate noise coupling problem

Corresponding Author: Gholam Reza Karimi, Department of Electrical Engineering, Faculty of Engineering, Razi University, Kermanshah 67149, Iran Tel: (+98) 21 73913714 Fax: (+98) 21 73913713

a topic that merits further and more detailed investigation. The ever-increasing demand to integrate all circuit components on the same chip gives rise to some critical noise tolerance requirements for sensitive analog circuits (e.g., PLL circuits) inside the chip. PLLs are ubiquitous circuit blocks in RF and mixed-signal integrated circuits. They are extensively utilized as on-chip clock generators to synthesize and de-skew a higher internal frequency from the external lower frequency (Heydari, 2004). In wireless communications, they are utilized as frequency synthesizers to synthesize an accurate output frequency (Kundert, 1997). In all of the above applications, the random temporal variation of the phase, or jitter, is one of the most critical performance parameters. Jitter represents the deviation of zero crossings of a periodic waveform from their ideal points on the time axis. The deviation of zero crossings of the waveform synthesized by the PLL causes the setup and hold-time violations in digital circuits that use the PLL as clock generator and therefore, leads to data transmission errors and functionality failure.

While circuit-level simulation provides accurate results, it requires extensive computation over extended time periods, especially when performing transient analysis of complex circuits such as those involving PLL circuits (Heydari, 2004). As a result, accurate simulation of PLLs is of great practical importance. Direct time domain simulation of PLLs at the circuit level in SPICE is typically impractical because of its great inefficiency. PLL transients can last hundreds of thousands of cycles, with each cycle requiring hundreds of small time steps for accurate simulation of the embedded Voltage-Controlled Oscillator (VCO). For instance, in circuit level simulation, if it is performed with a 10 psec time step for measurement of jitter from 10 psec to 50 μsec tracking time, as many as 5 million points would be calculated! Extremely high simulation time and nonlinear characteristics of mixed mode analog-digital PLLs results in major bottlenecks to design a stable PLL system.

Very often, however, it is necessary to simulate the system in a coarse but fast way in order to gain initial design guidance. For example, speed is more critical than accuracy when simulations need to be repeated in order to identify key parameters in the design. In these cases, a behavioral level modeling technique can be a powerful option to exploit trade-offs between simulation time and accuracy. In this context, behavioral simulation for PLLs has been studied from several perspectives, including noise considerations (Heydari, 2004; Kundert, 1997; Perrott, 2002).

Previous studies demonstrate mathematical and macro modeling technique for each block of the PLL (Kundert, 1997; Perrott, 2002). Another approach is to simulate the tracking and phase noise of a PLL using higher level analysis such as algebraic and differential equations. The parameters of a PLL are not well predicted using linear or mathematical models, due to nonlinear behavior of the PLL prior to locking (Donnay *et al*., 1996; Liu and Sangiovanni-Vincentelli, 1992; Chang *et al*., 1992). All of these approaches do not suggest a real-time based jitter simulation. In current SOC era, the substrate coupling must be considered, but in most presented approach, this phenomenon has not yet been seriously addressed. The goal of this paper is to predict the effect of substrate coupling on charge pump PLL (CPPLL) parameters. This is accomplished by using an efficient analytical model for substrate. The analytical model is verified by simulation of a CMOS CPPLL circuit designed in a 0.35 μm standard CMOS process surrounded by switching inverters' chain that emulate the switching of digital circuits.

BACKGROUND ON SUBSTRATE COUPLING MODELING AND PROBLEM FORMULATION

Several approaches have been presented in the past to attempt to quantify the effects of noise coupling through the substrate. Examples of such techniques include Finite Element Method (FEM), Boundary Element Method (BEM) and Finite Difference (FD) numerical methods for computing all of the currents and voltages in the substrate (Wemple and Yang, 1995; Costa *et al*., 1999; Stanisic *et al*., 1994; Gharpurey and Meyer, 1996; Koukab *et al*., 2004). Unfortunately, such methods are impractical for anything but simple problems, because these methods rely on volume meshing of the entire substrate. The number of unknowns resulting from the discretization can easily become very large and so lead to consuming large amount of memory and long run time. In this study, we present an efficient analytical method for evaluation of substrate coupling. The proposed method is based on a Green's function that plays a key role in speed-up and convergence of extraction process by avoiding high memory usage and long computation times.

Proposed analytical model : In this section we propose the analytical model by defining a Green function for evolution of substrate cross talk. Assuming the electrostatic approximation, the substrate can be modeled as a stratified medium composed of several homogeneous layers characterized by their conductivity, as shown in Fig. 2. On the top surface a number of ports or contacts are defined, which correspond to the areas where the

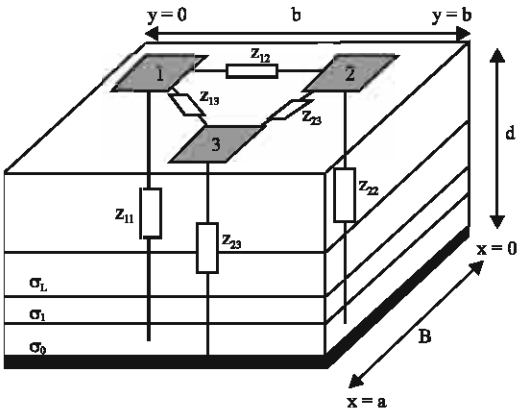

Fig. 2: 3D substrate profile

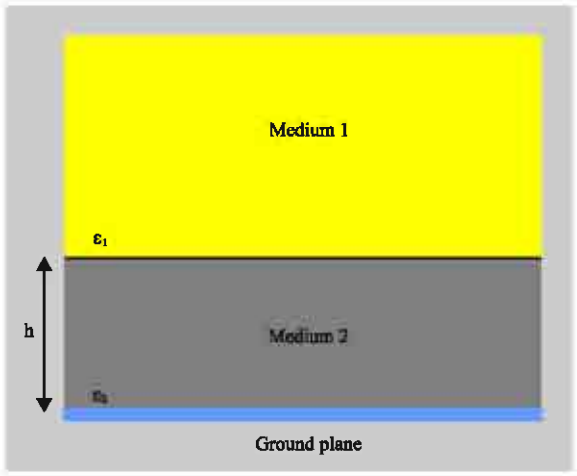

Fig. 3: Illustration of the substrate for calculating the green's function (Masoumi *et al*., 2002)

designed circuit interacts with the substrate. Examples include possible noise sources or receptors, such as contacts from substrate or well to supply lines, drain/source/channel areas of transistors, etc.

Parasitic elements extraction: Using electrostatic approximation and applying the Green's theorem, the potential at some observation point r = (x, y, z) due to a unit current injected at some source point r′ = (x′, y′, z′) can be fined as:

$$\phi(r) = \int_V \rho(r')G(r,r')dv \qquad (1)$$

where, ρ is the source current density and G(r, r′) is the Green's function of substrate impedance, which accounts for this problem's boundary and interface conditions. Once the Green's function of the medium has been determined, it is possible to compute the parasitic elements. For the substrate considered here, the boundary conditions are Dirichlet boundary for voltage (ϕ = 0) at the ports where the potential is specified and Neumann boundaries (∂ϕ/∂n = 0) at the specified field and the mixed boundary conditions over the remaining portion. With state of the art IC technology, all devices and related contact geometries, such as substrate taps, ground ring and drain/source diffusions of MOSFETs, are located near the top surface of substrate. Whereas the thickness of these structures is a fraction of a micron, the *flattening* approximation of the geometries (two-dimensional) onto the surface of the chip can be used (Koukab *et al*., 2004; Masoumi *et al*., 2001a). For this case, all the source and observation points are at the substrate contacts which are on the top surface (z = z′ = 0). Using this approximation, the volume integral in (1) reduces to a surface integral as:

$$\phi(x,y) = \int_S \rho_s(x',y')G(x,y,x',y')ds \qquad (2)$$

where ρ_s is the surface current density.

So, the expression (2) appears as an integral equation. By computing an integral involving the Green's function over the appropriate contact surfaces, we can derive the parasitic impedance z_{ij} as follows (Masoumi *et al*., 2001b)

$$z_{ij} = \frac{(1/jw)}{S_i S_j}\int_{S_i}\int_{S_j} G(r,r')ds_i ds_j \qquad (3)$$

Analytical green's function: The green's function is useful as a solution technique in many problems such as full electromagnetic calculations or diffusion problems (Gharpurey and Meyer, 1996). The Green's function for the substrate provides the potential generated by point source. G(r, r′) stands for ratio between the potential at point r and the current at point r′. Once the Green's function of the medium has been determined, it is possible to compute the parasitic elements. The proposed method is similar to Masoumi *et al*. (2002). The approach is based on point-form approximation method and on the usage of the image theory. As a result, the Green's function for the substrate (Masoumi *et al*., 2002) shown in Fig. 3 is:

$$G(x',y',x,y) = \frac{1}{4\pi\varepsilon_1}\left[\frac{1+\eta}{\sqrt{(x'-x)^2+(y'-y)^2}} + \frac{\eta^2-1}{\eta}\left[\frac{1}{2h}\ln\left(\frac{1}{1-\eta}\right) + \sum_{n=1}^{N}\left(\frac{\eta^n}{\sqrt{(x'-x)^2+(y'-y)^2+(2h)^2n^2}} - \frac{\eta^n}{2hn}\right)\right]\right] \qquad (4)$$

where, σ is the conductivity for each layer and d is the thickness of the substrate. To derive the parasitic element, Eq. 3 must be calculated. The solution approach is similar

to (Masoumi *et al*., 2002). At first, the four-fold integrals can be calculated as follows:

$$A1 = \int_{y1}^{y2}\int_{x1}^{x2}\int_{0}^{\Delta y}\int_{0}^{\Delta x}\frac{1}{\sqrt{(x-x')^2+(y-y')^2}}dxdydx'dy' \quad (5)$$

$$A2 = \int_{y1}^{y2}\int_{x1}^{x2}\int_{0}^{\Delta y}\int_{0}^{\Delta x}\frac{1}{\sqrt{(x-x')^2+(y-y')^2+k^2}}dxdydx'dy' \quad (6)$$

In this case, we consider two panels with the areas S1 and S2, as shown in Fig. 4 (Masoumi *et al*., 2002).

It can easily be shown that A1 is represented by the following expression:

$$\begin{aligned}A_1 = {} & f_1(x_2,y_2)-f_1(x_2,y_1)-f_1(x_1,y_2)+f_1(x_1,y_1)\\ & -f_1(x_2,y_2-\Delta y)+f_1(x_2,y_1-\Delta y)+f_1(x_1,y_2-\Delta y)\\ & -f_1(x_1,y_1-\Delta y)-f_1(x_2-\Delta x,y_2)+f_1(x_2-\Delta x,y_1)\\ & +f_1(x_1-\Delta x,y_2)-f_1(x_1-\Delta x,y_1)+f_1(x_2-\Delta x,y_2-\Delta y)\\ & -f_1(x_2-\Delta x,y_1-\Delta y)-f_1(x_1-\Delta x,y_2-\Delta x)\\ & +f_1(x_1-\Delta x,y_1-\Delta x)\end{aligned} \quad (7)$$

Similarly, A2 is represented as in (7) by substituting f_1 with f_2. f_1 and f_2 are given by:

$$\begin{aligned}f1(x,y) = {} & \frac{1}{2}xy^2\sinh^{-1}\left(\frac{x}{|y|}\right)+\frac{1}{2}x^2y\sinh^{-1}\left(\frac{y}{|x|}\right)\\ & -\frac{1}{6}(x^2+y^2)^{3/2}+\frac{1}{6}|x|^3+\frac{1}{6}|y|^3\end{aligned} \quad (8)$$

and

$$\begin{aligned}f2(x,y,k) = {} & \frac{1}{2}x(y^2-k^2)\sinh^{-1}\left(\frac{x}{\sqrt{y^2+k^2}}\right)\\ & +\frac{1}{2}xk^2\sinh^{-1}\left(\frac{x}{|k|}\right)+\frac{1}{2}yk^2\sinh^{-1}\sinh^{-1}\left(\frac{y}{|k|}\right)\\ & +\frac{1}{2}y(x^2-k^2)\sinh^{-1}\left(\frac{y}{\sqrt{x^2+k^2}}\right)+\frac{1}{3}|k|^3\\ & -kxy\tan^{-1}\left(\frac{x}{k\sqrt{x^2+y^2+k^2}}\right)\\ & -\frac{1}{6}\sqrt{x^2+y^2+k^2}(x^2+y^2-2k^2)\\ & +\frac{1}{6}\sqrt{y^2+k^2}(y^2-2k^2)+\frac{1}{6}\sqrt{x^2+k^2}(x^2-2k^2)\end{aligned} \quad (9)$$

The above functions (f_1 and f_2) can be derived by using the mathematical techniques such as the integral properties of the hyperbolic sinusoidal function. It can be seen that f_1 and f_2 are even functions. So for extracting the impedances to backplane, when i = j or $x_1 = y_1 = 0$, $x_2 = \Delta x$, $y_2 = \Delta y$, for simplification, A_1 and A_2 can be rewritten as:

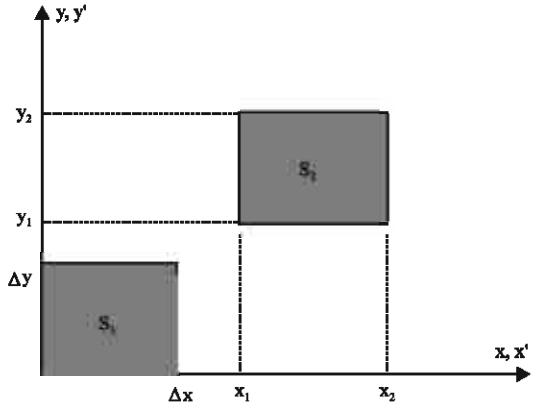

Fig. 4: Illustration of the contacts areas (Masoumi *et al*., 2002)

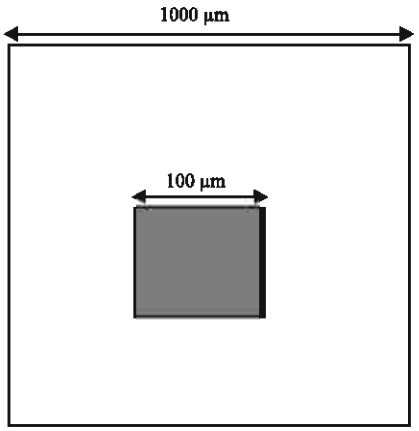

Fig. 5: Single square contact substrate problem (Masoumi *et al*., 2002)

$$A_1 = 4f_1(\Delta x,\Delta y) \quad (10)$$

$$A_2 = 4f_2(\Delta x,\Delta y,k) \quad (11)$$

Validation of the proposed model (simulation results): In order to demonstrate the accuracy and efficiency of the proposed model, we present several examples and compare the results with those obtained by other methods. At first, we use the single square-contact substrate profile of dimension 100 μm located on the substrate of h = 100 μm height and ρ = 10 Ω-cm as shown in Fig. 5. Table 1 shows the simulation results using the discrete cosine transform method (DCT), finite difference method reported in (Gharpurey and Meyer, 1996), the method in (Masoumi *et al*., 2001b) and our proposed method. As seen in this table the accuracy of the mentioned methods is comparable.

For further verification of accuracy of proposed Green's function and analytical technique, we consider

Table 1: Resistance of a single square contact by several techniques

Technique	Memory usage	Run time (sec)	Resistance (ohm)
DCT (Koukab *et al*., 2004)	263 k	1+75 (DCT)	340.0
FD (Koukab *et al*., 2004)	547 k	674	318.0
Analytical integration (Masoumi *et al*., 2002)	Negligible	10.02 m	342.8
Present study	Negligible	90.2 m	340.2

Table 2: Selected set of extracted resistances (in kΩ) for the example layout shown in Fig. 7 by several techniques

Technique	$R_{3,4}$	$R_{25,50}$	$R_{33,34}$
Analytical integration (Masoumi *et al*., 2002)	59.297	503.437	60.980
IE3D	61.333	450.343	62.734
Present study	63.141	496.365	63.163

the configuration of a mixed-signal circuit investigated (Costa *et al*., 1999). The layout for the example problem is a 52-contact on a substrate with h = 400 μm height and ρ = 15 Ω-cm as shown in Fig. 6. As can be seen from Fig. 6, the contacts for this problem are of varying dimensions, which is typical for a mixed-signal design.

We apply the proposed technique to this problem. Table 2 shows a selection of relevant resistances computed using the method in (Costa *et al*., 1999), IE3D simulator and our analytical based method. IE3D is a 3D, full wave, method of moment, integral equation electromagnetic simulator (Zeland Comp. homepage). Simulation results of these techniques are comparable and show a good agreement with each other. The total runtime for the proposed extraction technique applied to the 52-contacts problem is 120.40 sec carried out on the PC Centrino 1.8 GHz. The computational cost for method claimed in Koukab *et al*. (2004) is 8405.64 sec by Sun Ultra Space 1 and for method in Masoumi *et al*. (2002) is 18.67 sec by Sun Ultra 12 workstation.

As can be seen, in terms of computational cost, a very good factor of speed-up has been obtained. The last example is on the parasitic capacitances extraction C_{11} and C_{21} between two square-contacts of dimension 10 μm located on a substrate with 400 μm height. Figure 7 shows good agreement of IE3D simulation result with proposed analytical technique. As shown in Figure 7, C_{11} is almost independent of the distance between the contacts, but C_{21} has an inverse dependency on the distance. The simulation results show that in the proposed technique, only direct arithmetic calculations are needed to be computed and there is no need for huge data to be stored. We use this model for extraction of resistances of substrate model which can then be used in a circuit simulator.

BUILDING BLOCK OF PLL

Although the phase locked loop is simple in principle, its monolithic implementation involves many subtleties and it continues to be an area of intense study. In this study,

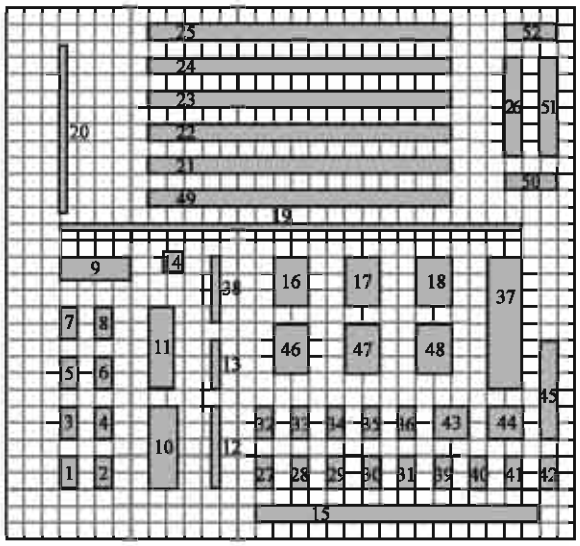

Fig. 6: The layout for the example problem is a 52-contact on a substrate with h = 400 μm and ρ = 15 Ω-cm

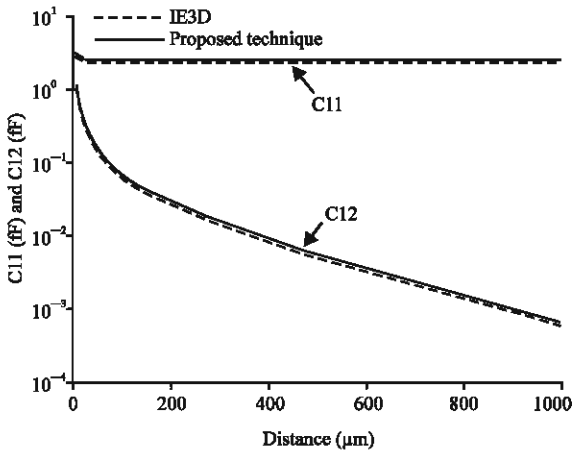

Fig. 7: Comparison of two different methods for parasitic capacitances extraction

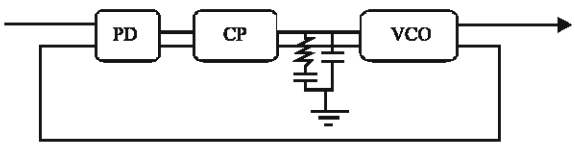

Fig. 8: The basic building blocks of PLL

we use a basic structure of PLL as shown in Fig. 8. A comprehensive functional description of the charge-pump PLL can be found in many textbooks on analog/RF integrated circuits (Razavi, 2001, 1996). The external periodic 9 signal which is normally generated by a crystal circuit acts as one input of a phase-frequency detector

(PFD). The internal clock drives the other input of PFD. The PFD compares the leading edges of its inputs and generates two pulsed signals, UP and DOWN. The pulse widths of the UP and DOWN output terminals depend on the phase deference between the two inputs of the phase detector. The output signals of PFD then drive a charge pump circuit followed by the loop filter. The charge-pump circuit, via two switches, either injects, subtracts, or leaves unchanged the charge stored across a capacitor in the loop filter. The output voltage of the loop filter controls the frequency of the VCO. The loop is a negative feedback loop and if the input frequency is in the capture range of the PLL, then after some elapsed time called the acquisition time, the PLL is locked to the input frequency.

First, we design the blocks of the PLL separately. In this research by considering the stability conditions, we design the PLL with 1 MHZ bandwidth and 500 MHZ output frequency.

Phase-Frequency Detector (PFD): Common types of PFD circuits are the structures with D flip-flop and RS latch. But these circuits suffer from the dead zone effect. To minimize the PLL static phase error, it is desirable to eliminate this dead zone and the non-linearity when PLL is in steady state. So, we use the circuit for PFD with structure shown in Fig. 9. It is a modified version of the design in Reference (Maneatis, 1996).

Charge pump and loop filter: The charge pump circuit is driven by Up and Down signals. Figure 10 shows the common Charge pump structure with a second order low pass filter. In typical designs, the capacitance C1 is often much larger than C2 to obtain a reasonable phase margin. The values of the current sources and elements of the filter are determined according to the stability conditions of PLL.

Figure 11 shows the simulated results of the charge pump and filter combination. As shown from these results, the pulse widths of the UP and DOWN output terminals depend on the phase deference between the two inputs of the phase detector. The output signals of PFD then drive a charge pump circuit followed by the loop filter.

VCO circuit: The design of oscillators itself is a very broad topic and a rather independent one. Since the focus of this paper is about the CMOS implementation, the discussion will be limited to this scenario. Two commonly used monolithic VCO topologies will be used: (1) LC tank oscillator and (2) ring oscillator. Ring oscillators are more widely used in integrated systems

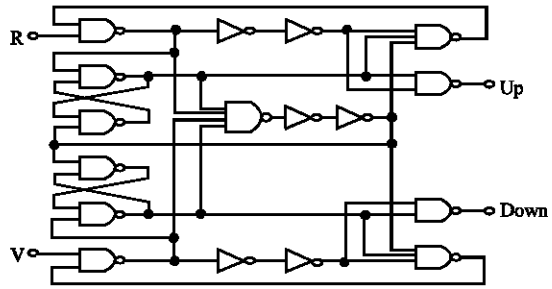

Fig. 9: Phase frequency detector

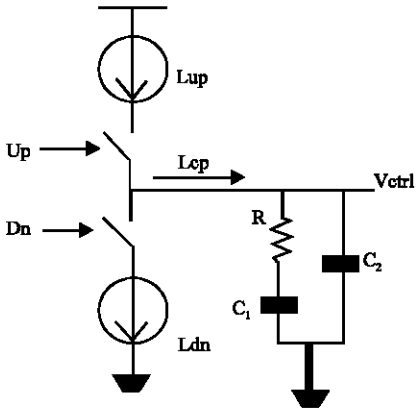

Fig. 10: Charge pump and low pass filter

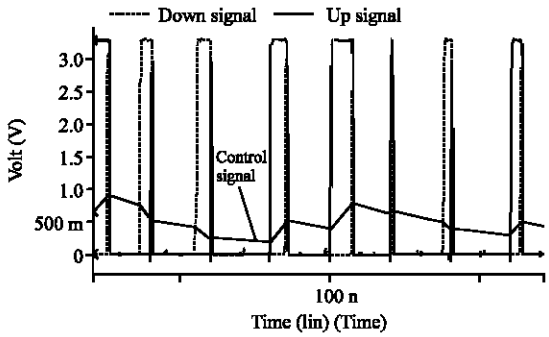

Fig. 11: Simulated results for PFD-LPF

than LC oscillators because they are easy to implement at rather low cost. A ring oscillator topology used in this paper is shown in Fig. 12.

Since a core component of the PLL is the voltage controlled oscillator (VCO), the characteristic transfer curve relating output frequency to the VCO input voltage is critically important in abstracting the PLL behavioral model. Hence, the VCO is simulated at the circuit level with varying input voltages; the nonlinear characteristics of the VCO is then determined (Fig. 13). These characteristics are later used in behavioral modeling for more accurate design.

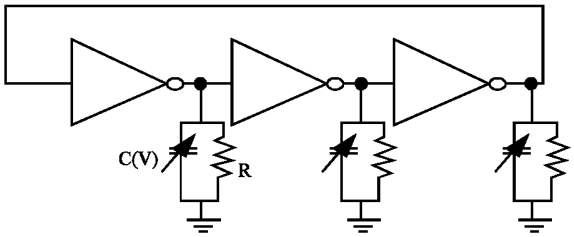

Fig. 12: The schematic of the used oscillator

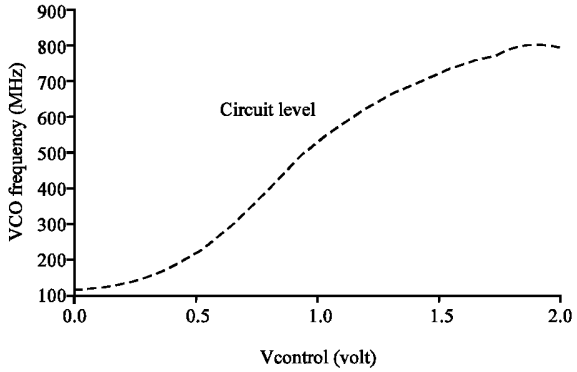

Fig. 13: VCO gain curve of VCO circuit

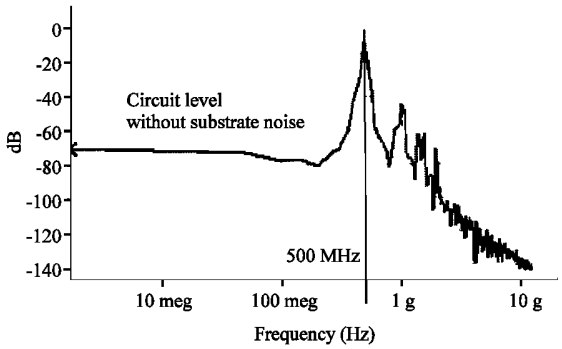

Fig. 14: VCO output spectrum

The output spectrum frequency of VCO, in circuit level simulation, is shown in Fig. 14.

PLL NOISE MODEL

The system block diagram of a PLL along with all of the relevant noise sources is shown in Fig. 15. The average power-spectral densities (PSD) of environmental noise sources, such as substrate noise are much greater than those of device noise sources, such as thermal noise (Heydari, 2003; Heydari and Pedram, 2002; Badaroglu *et al*., 2002). As a result, the PLL jitter due to various device noise sources is negligible compared to the jitter due to the environmental noise sources (Hajimiri, 2001; Kim *et al*., 2005).

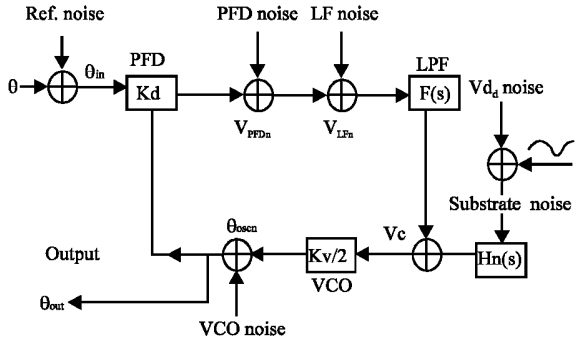

Fig. 15: Block diagram of PLL with all the relevant noise sources

In the locked loop condition, the following equation shows all of the phase noise contributions in the PLL loop

$$\theta_{out} = \left[\theta_{in} - \theta_{pdn} + \frac{V_{PFDn} + V_{LFn}}{K_d}\right] \cdot \frac{G(s)}{1+GH(s)} + \theta_{oscn} \cdot \frac{1}{1+GH(s)} + V_{ddn,Subn} \cdot \frac{H_n(s)}{1+GH(s)} \cdot \frac{K_v}{s} \quad (12)$$

Where:

$$GH(s) = \frac{K_d K_v F_{LP}(s)}{s}$$

is the open loop gain.

In general, all constituent loop components may contribute noise and jitter to the PLL output. The effect of noise on the phase detector performance has been studied (Kroupa, 1982). The phase detector is not, however, a major contributor to the PLL phase noise and jitter. The phase detector fluctuations due to substrate noise are largely attenuated using a differential architecture and also by means of the PLL loop filter. As a result, timing jitter in a PLL is mainly associated with two important noise sources induced by substrate noise:

- Noise at the input
- Phase noise of the VCO

The loop bandwidth as well as the peaking of the loop frequency response of the PLL determines which noise source has the dominant impact on the PLL timing jitter. The noise at the input propagates through the same signal path as the input signal to the PLL. Therefore, the noise transfer function for the input noise is identical to the signal transfer function. This means that a narrow-band low pass filter eliminates the higher frequency components of the input noise and reduces the impact of the input noise source on the timing jitter. On the other

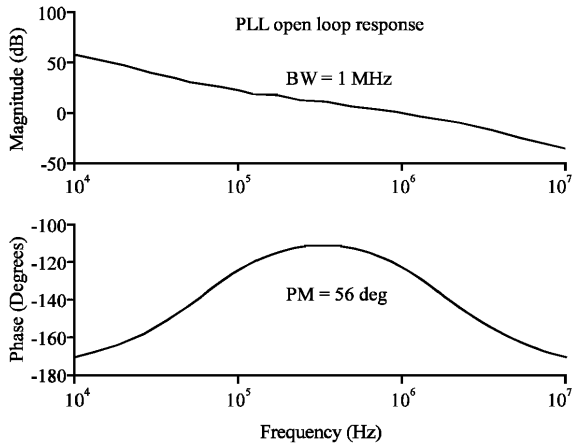

Fig. 16: Simulated bandwidth and phase margin of PLL

hand, the PLL operates as a high pass filter for the VCO noise (Lee *et al*., 2001), meaning that, in contrast to the input noise, a narrow-band loop filter is not a good choice for the VCO phase noise attenuation.

However, the loop bandwidth should be less than the reference input frequency to keep the loop stable (Heydari and Pedram, 2003; Lee *et al*., 2001). So, the selection of optimal bandwidth of PLL is a critical parameter in design process. The simulation begins with investigation of the CPPLL stability in the open loop PLL configuration. The loop filter parameter values and current source values for the required loop width are obtained by loop stability analysis using MATLAB. The simulated stability and bandwidth of the PLL is shown in Fig. 16.

This result shows a good agreement with the hand calculation.

Substrate coupling: In the case of PLLs, the procedure can be simplified since most sub-blocks are digital and insensitive to substrate noise. By contrast, the VCO (and in particular, the ring VCO) is the most noise-sensitive circuit among other sub-blocks in a PLL circuit. The reason is that the ring VCO is a closed-loop oscillator where corrupted zero-crossings of the oscillations due to substrate and supply noise are recirculated in the loop. So, it is assumed that the dominant noise inside the PLL loop is thus contributed by the VCO phase noise (Heydari, 2004; Kim *et al*., 2005).

For realizing the substrate coupling from digital block, we use a five stage inverter chain with each stage loaded by two inverters sized a power of 2 larger than previous stage to increase the noise coupling. The first inverter transistor's dimensions are $\left(\frac{W}{L}\right)_n = \left(\frac{4}{0.35}\right)\mu m$ and $\left(\frac{W}{L}\right)_p = \left(\frac{7}{0.35}\right)\mu m$.

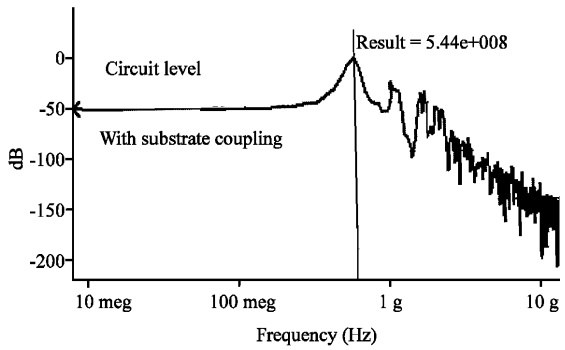

Fig. 17: Output spectral content of the VCO with substrate coupling

At first, we extract the resistance model of substrate using the method mentioned in section II using MATLAB. We assume that the distance between these circuits (digital block and VCO) is far enough so far that the coupling occurs mainly through the direct substrate node. The result is shown in Fig. 17. As shown from this figure, substrate coupling noise couples with the VCO to cause a change in its frequency ($\Delta f = 44$ MHZ).

BEHAVIORAL MODELING FOR PLL NOISE ANALYSIS

The goal of behavioral modeling in higher level building blocks is to ease and accelerate the design of analog circuits, such as reducing PLL simulation time. Since these behavioral simulations show the major characteristics of the PLL system, design errors are detected early and phase noise is predicted. While the behavioral simulation technique has the advantage of faster computational speed, it provides only coarse results. In order to guarantee the accuracy as well as speed of the behavioral simulations, it is critical to carefully abstract the characteristics of each block from the circuit- or device-level analysis for use at the system level model. In this section, we present efficient models using VHDL-AMS (Vhdl-ams, 1999) and also with piecewise linear (PWL) behavioral modeling. The efficiency of the proposed models in analyzing substrate noise will be validated by comparing both speed and accuracy with the full circuit-level simulation results.

Behavioral modeling of PLL Using VHDL-AMS: First, we consider the behavioral modeling of noise-free PLL circuit using VHDL-AMS. The result of voltage control of filter is shown in Fig. 18. Table 3 shows the important parameter values for PLL in the lock condition.

As mentioned earlier, VCO is susceptible to substrate noise. This noise causes a change in its frequency (Δf).

Table 3: Comparison between circuit and behavioral modeling results without substrate coupling

Parameter	Behavior model (VHDL-AMS)	Circuit level (HSPICE)
Run time	280 sec	11500 sec
Lock in time	≈ 7.5 μsec	≈ 7.8 μsec

Table 4: Comparison between circuit and behavioral modeling results with substrate coupling

Parameter	Behavior model (VHDL-AMS)	Circuit level (HSPICE)
Run time	292 sec	12900 sec
Lock in time	≈ 9 μsec	≈ 10 μsec

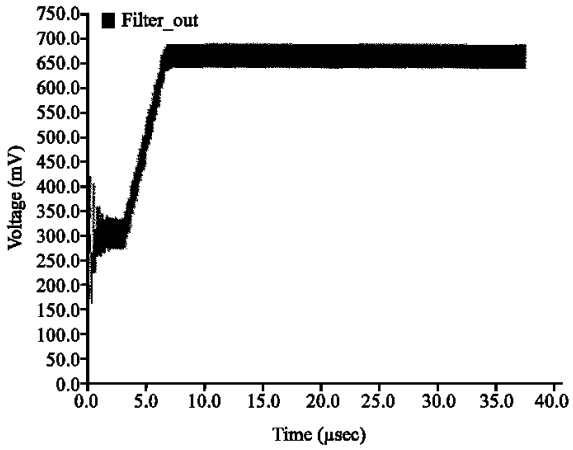

Fig. 18: Simulated control voltage of the filter without applying substrate noise

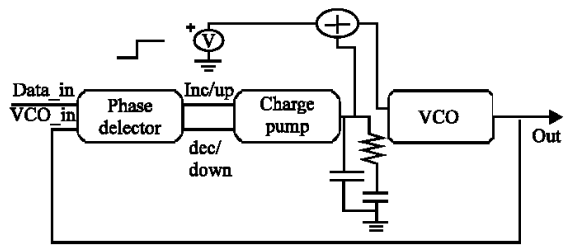

Fig. 19: PLL substrate noise simulation schematic

So, in lock condition, PLL needs a number of clock cycles to correct this phase error. We have used the schematic in Fig. 19 to monitor the transient response of the PLL phase error to power supply noise. The change in VCO frequency due to substrate noise is simulated as a corresponding voltage step at the VCO input. We make the same assumptions as made previously, that the loop is locked. The change in frequency from its value using the circuit level simulation was obtained (from Fig. 16). Then the corresponding input noise voltage required to achieve this frequency step was calculated using the VCO gain K_0.

The PLL was then simulated in the transient domain using behavioral VHD-AMS model for the PLL. The result was investigated by control voltage of filter as shown in Fig. 20. As shown in Fig. 20, the capture time has been increased about 2.5 μsec. Table 4 shows a summary of obtained results.

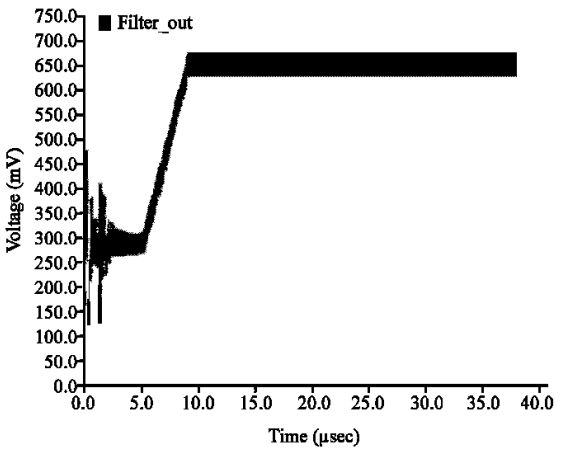

Fig. 20: Simulated control voltage of the filter with applying substrate noise

As shown from these results, the substrate coupling affects the critical parameters and performance of PLL. It is very important to capture higher-order effects earlier on in a top-down design flow. In this paper a methodology has been proposed to use a VHDL-AMS like language to capture and simulate the effect of faults on the jitter and power supply coupling in a mixed-signal PLL. This methodology is very attractive because the simulation time using a mixed-signal HDL was significantly low and characteristics such as the phase error were easily monitored. The use of a mixed-signal HDL enables us to capture the circuit at all levels of abstraction in the analog and digital domain. Thus, any block amongst the entire circuit can be captured at a desired level of abstraction. Also, the use of a VHDL-AMS like language allows a natural integration of design and test for mixed-signal circuits, at the behavioral level.

Piecewise linear (PWL) behavioral modeling of PLL: The HSPICE simulator suffers from DC convergence problems since it uses a Newton-Raphson iteration algorithm (Vhdl-ams, 1999; Star-Hspice). In small circuits, it may be possible to solve the convergence problem by setting initial node voltages. However, in a large mixed mode analog and digital circuit, it is not easy to find the DC operating point for starting the simulation. The process of riding non-convergence errors in circuit simulation results in long simulation times. To overcome long simulation times at the circuit level and to solve the

difficulty of nonlinear operation modes, precise behavioral modeling Like a real circuit simulation is required for quick estimation of PLL performance. Furthermore, all PLL performance parameters are simulated in the domain like a circuit level simulation, after extracting critical parameters from each of functional blocks of the PLL. Because PWL elements do not use Newton-Raphson iteration algorithms to solve the nonlinear equations, using this behavioral modeling is a good case for mixed-signal circuit modeling. Another advantage of using PWL modeling is that, this approach significantly reduces the simulation time. Digital gates such as AND, OR, NAND, NOR and INVERTER are simulated by one command with a few PWL segments. Finally, other analog circuits such as comparators and operational amplifiers can be modeled for slew rate, gain and bandwidth, with inclusion of nonlinear effects with a few PWL segments. Bottom-up verification (circuit level simulation) for behavioral modeling is done by the characterization of each block. The simulation results (using HSPICE) from a transistor level description of components are compared with the result of the behavioral simulation. In this part, we model the PLL blocks with this technique.

- **PFD circuit:** As mentioned previously, there are several types of phase detectors such as analog multiplier, exclusive-OR, JK-type and transmission gate PD. Most of them suffer from the nonlinear characteristic of dead zone. Thus, we use the PFD in Fig. 9 to minimize the dead zone and improve jitter performance. Each basic element such as INV, NAND and OR is first simulated in a transistor level circuit using a dc sweep of the input and measuring the output current. Next, a lookup table element is defined. The dc characteristics and transient characteristics of CMOS inverter circuit and its behavioral model are compared in Fig. 21. The other multi-input logic gates (AND, OR, NAND and NOR) in HSPICE also use only one output current source which represents the PWL variation of output as a function of input. All logic elements for the PFD are built up using the subcircuit command, based on the PFD block diagram. A comparison of simulation results obtained at circuit level and by behavioral model is shown in Fig. 22.

- **Charge pump circuit:** The non-ideal effect of CP i.e., current mismatch, can cause a small charge or discharge of voltage control of filter even when the PLL is locked. These noises generate sidebands in the output spectrum or modulate the VCO with periodic changes in the control voltage. This effect can be modeled using the voltage-controlled current source value.

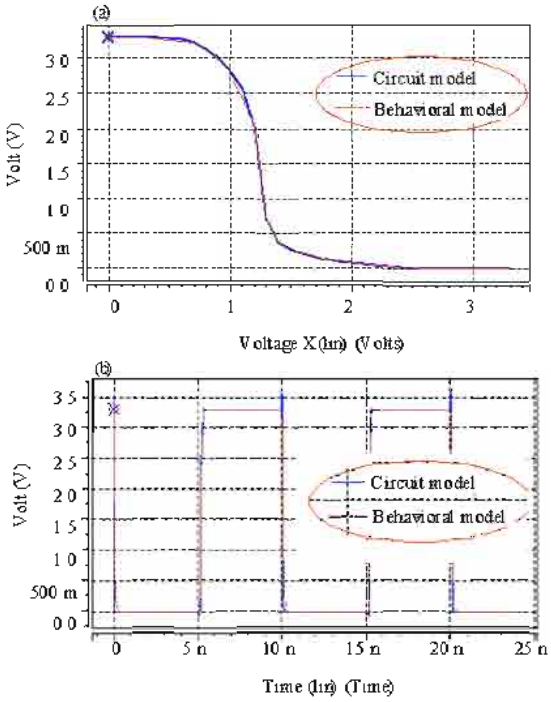

Fig. 21: DC and transient of the CMOS inverter (a) DC sweep and (b) transient response

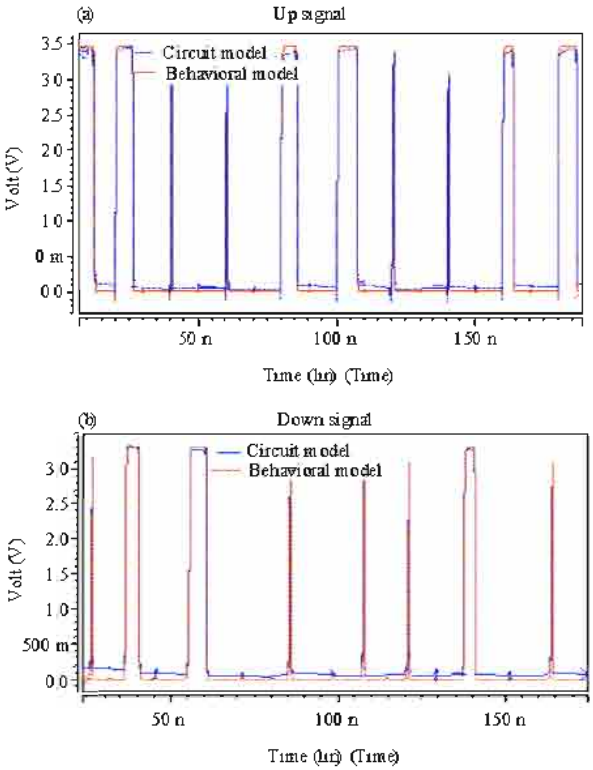

Fig. 22: Output signals of PFD in circuit and behavioral modeling (a) up signal and (b) down signal

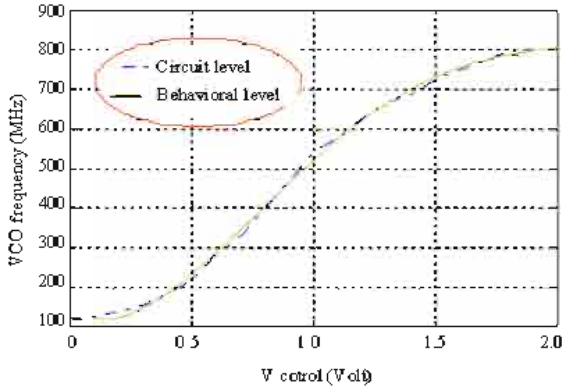

Fig. 23: VCO gain curve of VCO circuit and its behavioral model

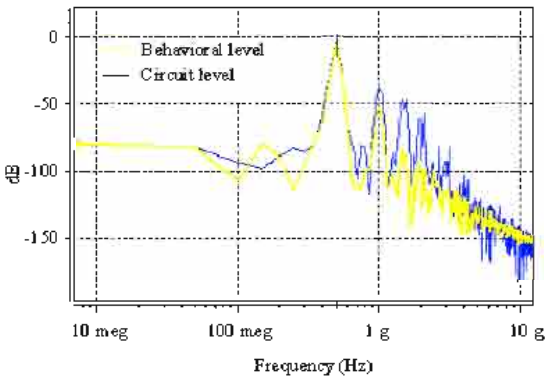

Fig. 24: Output frequency of VCO circuit with its behaviorual model

Substrate coupling model: To investigate the effect of substrate coupling on PLL performance, we use a five stage inverter chain with each stage loaded by two inverters sized a power of 2 larger than previously stage to increase the noise coupling. Similarly, we assume that the distance between these circuits (digital block and VCO) is so far that the coupling occurs mainly through the direct substrate node (Fig. 23, 24).

Simulation results: An important characteristic of PLL performance is the capture time by which the PLL acquires locking with reference clock signal, starting from a free-running condition. At first, we start the simulation when the substrate coupling is not considered. Figure 25 represents the simulated control voltage of the PLL circuit and behavioral modeling during locking, without applying substrate coupling, respectively. A good agreement is shown between the results, whereas the time of the simulation is reduced appreciably.

In this situation, Table 5 shows the simulation results.

Table 5 Result summary

Parameter	Behavioral model	Circuit model
Run time simulation	490 sec	11500 sec
Cycle jitter	10 psec	6.5 psec
Lock in time	= 7.5 sec	= 7.8 sec

Table 6 Result summary (with substrate coupling)

Parameter	Behavioral model	Circuit model
Run time simulation	630 sec	12900 sec
Cycle jitter	29 psec	22.5 psec
Lock in time	= 9.2 sec	= 10 sec

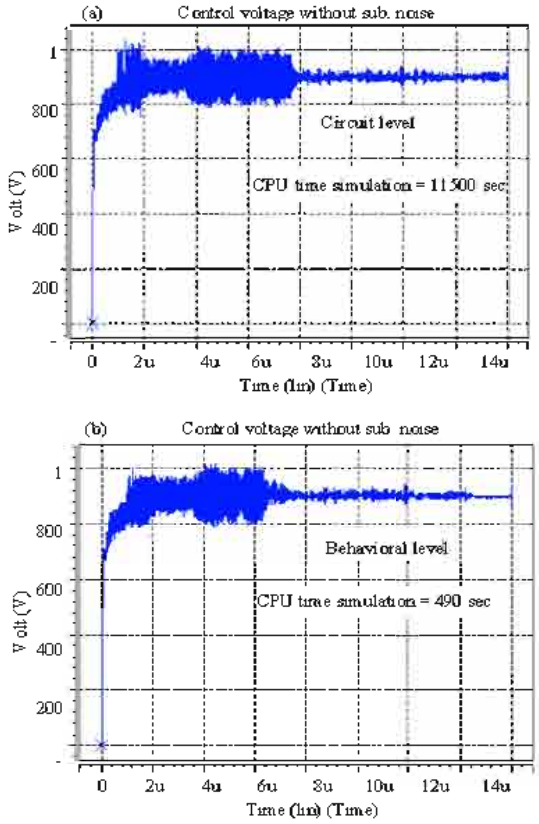

Fig. 25: Lock in time (a) circuit model and (b) behavioral model

Now, we considered the substrate coupling in circuit design. Figure 26 shows the simulated result for control voltage with substrate coupling consideration. As can be seen, the run time for behavioral modeling is 4-5% of that in circuit model simulation.

Table 6 summarizes the simulation result in this situation. The values in this table indicate that the circuit-level simulation and behavioral simulation have yield in much closed results, however, the run time is greatly reduced in the second method. So, the behavioral model simulation technique using PWL elements can be extended to characterize all PLL performances in time domain.

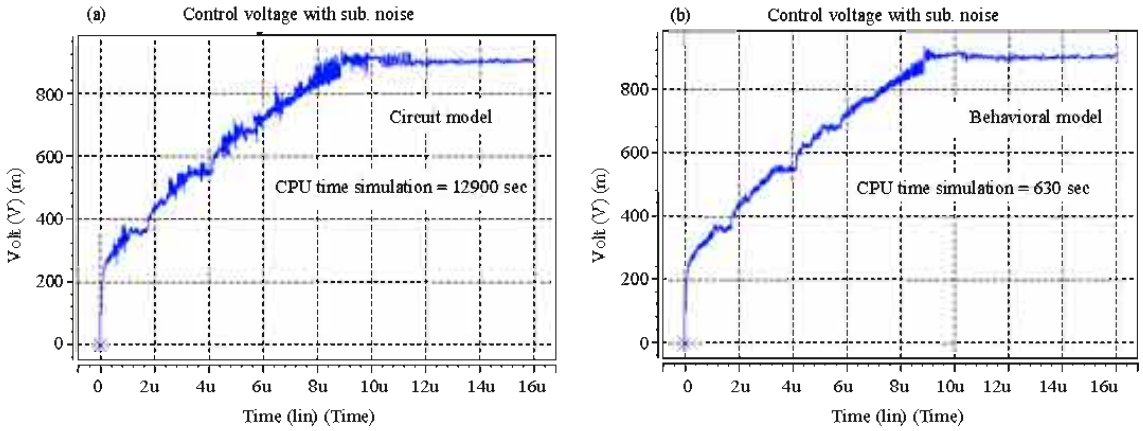

Fig. 26: Lock in time (a) circuit model (b) behavioral model

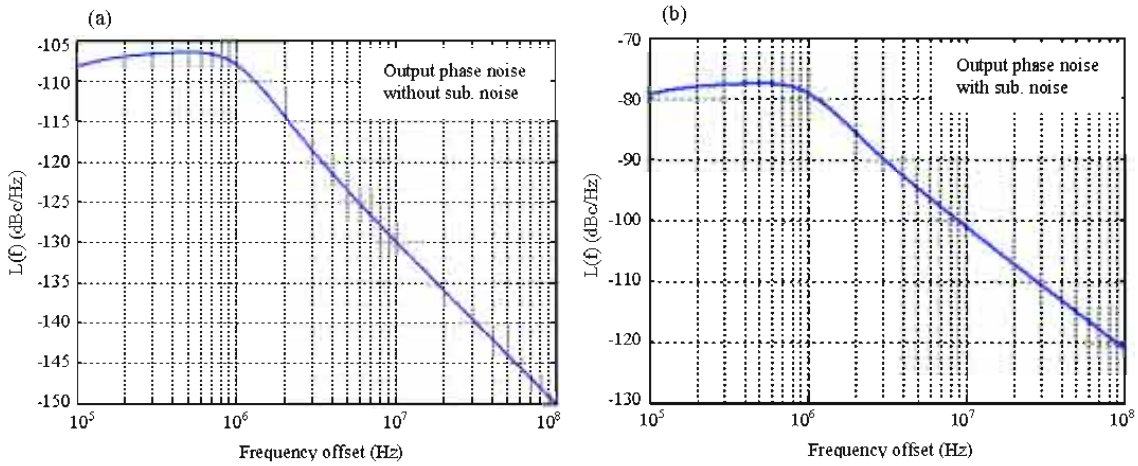

Fig. 27: Phase noise of the PLL output (a) without substrate coupling (b) with substrate coupling

To gain a better insight of effect of substrate noise coupling, the PLL's phase noise is shown without and with the influence of substrate noise in Fig. 27a,b, respectively. It can be seen from these two figures that the phase noise has increased by around 30 dB in the latter case.

CONCLUSION

In this research, we described a method to quickly and accurately estimate substrate coupling effects based on a Green's function formulation and the integral solution for substrate parasitic extraction. For verification, several examples were presented. Simulation results verified the accuracy and the efficiency of the proposed technique. A very good speedup factor was obtained when comparing our technique with other methods in the literature. In another part of this work, an investigation of the PLL performance due to substrate coupling noise from digital block was presented. Thus, modeling and simulation was done using a behavioral modeling by VHDL-AMS and with piecewise linear (PWL) behavioral modeling. A comparison between the results obtained by our models and those obtained by HSPICE simulation prove the accuracy of the predicted models. Also, to obtain the extra useful information, we have analyzed the results in frequency domain. This information helps the designer with optimal selection of RF and IF frequencies and also in using an efficient methodology to mitigate the substrate coupling in mixed-signal IC's.

ACKNOWLEDGMENT

This research is sponsored in part by Razi University.

REFERENCES

Badaroglu, M., M.V. Heijningen, V. Gravot, J. Compiet, S. Donnay, G.G.E. Gielen and H.J. De Man, 2002. Methodology and experimental verifications for substrate noise reduction in CMOS mixed-signal ICs with synchronous digital circuits. IEEE J. Solid-State Circuits, 37 (11): 1383-1395.

Chang, H. *et al*., 1992. Top-down constraint-driven design methodology based for analog integrated circuits. In: Proceeding Custom Integrated Circuits Conference.

Costa, J.P., M. Chou and L.M. Silveira, 1999. Efficient techniques for accurate modeling and simulation of substrate coupling in mixed-signal IC's. IEEE Trans. Computer-Aided Des., 18 (5): 597-607.

Donnay, S. *et al*., 1996. Using Top-Down CAD Tools for Mixed Analog/Digital ASICs: A Practical Design Case. Norwell, MA: Kluwer.

Gharpurey, R. and R.G. Meyer, 1996. Modeling and analysis of substrate coupling in integrated circuits. IEEE J. Solid-State Circuits, 31 (3): 344-353.

Hajimiri, A., 2001. Noise in phase-locked loops. In: Proceedings of IEEE Southwest Sympoisury Mixed-Signal Design.

Heydari, P., 2003. Characterizing the effects of clock jitter due to substrate noise in discrete-time Δ/Σ modulators. In: Proceedings IEEE/ACM Design Automation Conference.

Heydari, P. and M. Pedram, 2003. Ground bounce in digital VLSI circuits. IEEE Trans. VLSI Syst., 11 (2): 180-193.

Heydari, P., 2004. Analysis of the PLL jitter due to power/ground and substrate noise power/ground and substrate noise. IEEE Trans. Circuits Syst., 51 (12): 2404-2416.

Kim, J.W., Y.C. Lu and R.W. Dutton, 2005. Modeling and simulation of jitter in phase-locked loops due to substrate noise. In: Proceedings of the IEEE International Conference of BMAS, pp: 25-30.

Koukab, A., K. Banerjee and M. Declercq, 2004. Modeling techniques and verification methodologies for substrate coupling effects in mixed-signal system-on-chip designs. IEEE Trans. Computer-Aided Des. Integrated Circuits Syst., 23 (6): 823-836.

Kroupa, V.F., 1982. Noise properties of PLL systems. IEEE Trans. Commun. J., 30 (10): 2244-2252.

Kundert, K., 1997. Modeling and Simulation of Jitter in Phase-Locked Loops in Analog Circuit Design. Norwell, MA: Kluwer Academic Publishers.

Lee, C.H., K.Mc. Clellan and J. Choma, 2001. A supply noise insensitive PLL design through PWL behavioral modeling and simulation. IEEE Trans. Circuits Syst., 48 (12): 1137-1144.

Liu, E. and A. Sangiovanni-Vincentelli, 1992. Behavioral representations for VCO and detectors in phase-lock systems. In: Proceedings Custom Integrated Circuits Conference.

Maneatis, J.G., 1996. Low-jitter process-independent DLL and PLL based on self-biased techniques. IEEE J. Solid-State Circuits, 31 (11): 1723-1732.

Masoumi, N., S. Safavi-Naeini and M.I. Elmasry, 2001a. Efficient Green's Function for Substrate Coupling Modeling in VLSI Circuits. In: Processing of International Conference on VLSI-SOC: Systems on A Chip, Kluwer Academic Publications.

Masoumi, N., M.I. Elmasry, S. Safavi-Naeini and S.J. Kovacic, 2001b. Substrate-coupling noise analysis of a mixed-signal RF IC using an efficient technique for substrate paprasitic extraction. In: International Conference on Circuits, System, Communications and Computers.

Masoumi, N., M.I. Elmasry, S. Safavi-Naeini and H. Hadi, 2002. A novel analytical model for evaluation of substrate crosstalk in vlsi circuits. In: Proceedings IEEE International Workshop on Electronic Design, Test and Applications.

Miguel, S.L. and N. Vargas, 2000. Characterizing substrate coupling in deep-submicron designs. IEEE J. Des. Test Comput., 19 (2): 4-15.

Perrott, M.H., 2002. Fast and accurate behavioral simulation of fractional-n frequency synthesizers and other PLL/DLL circuits. In: Proceeding of the 39th Design Automation Conference (DAC), Anaheim, Calif.

Razavi, B., 1996. Monolithic Phase-Locked Loops and Clock Recovery Circuits. Piscataway, NJ: IEEE Press.

Razavi, B., 2001. Design of Analog CMOS Integrated Circuits. McGraw-Hill, New York.

Stanisic, B.R., N.K. Verghese, R.A. Rutenbar, R.L. Carley and D.J. Allstot, 1994. Addressing substrate coupling in mixed-mode IC's and power distribution synthesis. IEEE J. Solid-State Circuits, 29 (3): 226-237.

Su, D.K., M.J. Loinaz, S. Masui and B.A. Wooley, 1993. Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits. IEEE J. Solid-State Circuits, 28 (4): 420-430.

Star-Hspice, avant!, www.synopsys.com.

Vhdl-ams, 1999. com.http://www.vhdl-ms.com/.

Wemple, I.L. and A.T. Yang, 1995. Mixed-signal switching noise analysis using voronoi-tesselation substrate macromodels. In: Proceedings 32nd ACM/IEEE Design Automation Conference San Francisco, CA.